Si8920

Isolated Amplifier for Current Shunt Measurement

Features

- Low voltage differential input
  - ±100 mV and ±200 mV options
- Low signal delay: 0.75 µs
- Input offset: 0.2 mV
- Gain error: <0.5%
- Excellent drift specifications
  - 1 µV/°C offset drift
  - 60 ppm/°C gain drift
- Nonlinearity: 0.1% full-scale
- Low noise: 0.10 mVrms over 100 kHz bandwidth
- High common-mode transient immunity: 75 kV/µs
- Compact packages
  - 16-pin wide body SOIC
  - 8-pin surface mount DIP
- –40 to 125 °C
- AEC-Q100

Applications

- Industrial, HEV and renewable energy inverters
- AC, Brushless, and DC motor controls and drives
- Variable speed motor control in consumer white goods
- Isolated switch mode and UPS power supplies

Safety Approvals

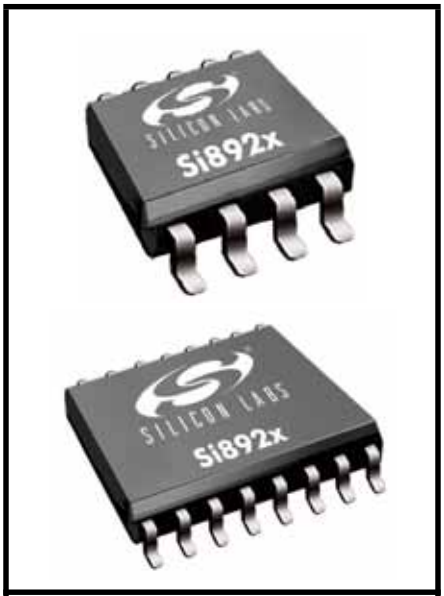
- UL 1577 recognized
  - Up to 5000 Vrms for 1 minute
- CSA component notice 5A approval
- VDE certification conformity
  - VDE0884 Part 10 (basic/reinforced insulation)
- CQC certification approval
  - GB4943.1

Description

The Si8920 is a galvanically isolated analog amplifier. The low-voltage differential input is ideal for measuring voltage across a current shunt resistor or for any place where a sensor must be isolated from the control system. The output is a differential analog signal amplified by either 8.1x or 16.2x.

The very low signal delay of the Si8920 allows control systems to respond quickly to fault conditions or changes in load. Low offset and gain drift ensure that accuracy is maintained over the entire operating temperature range. Exceptionally high common-mode transient immunity means that the Si8920 delivers accurate measurements even in the presence of high-power switching as is found in motor drive systems and inverters.

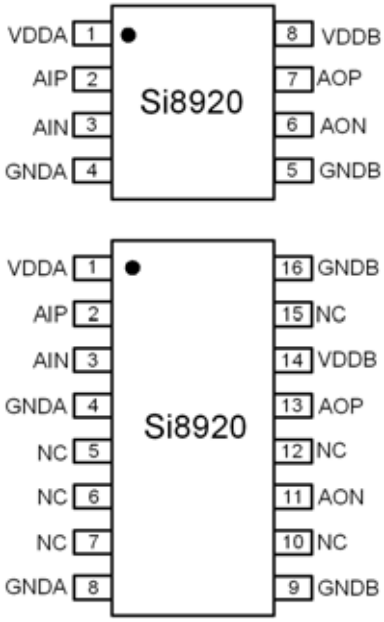
The Si8920 isolated amplifier utilizes Silicon Labs' proprietary isolation technology. It supports up to 5.0 kVrms withstand voltage per UL1577. This technology enables higher performance, reduced variation with temperature and age, tighter part-to-part matching, and longer lifetimes compared to other isolation technologies.



Ordering Information:

See page 15.

Pin Assignments



Patents pending

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1. Functional Block Diagram

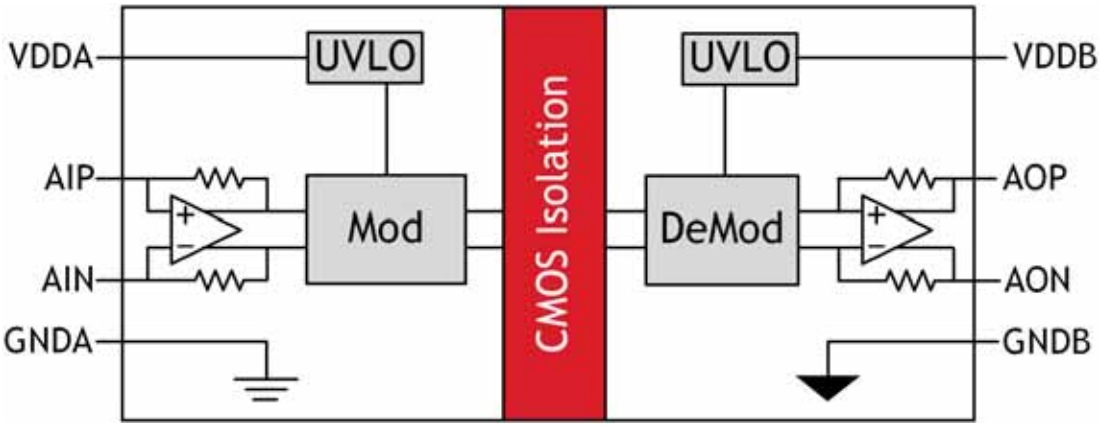


Figure 1. Si8920 Block Diagram

2. Electrical Specifications

Table 1. Electrical Specifications

V_{DDA}, V_{DDB} = 5 V, T_A = –40 to +125 °C; typical specs at 25 °C

Parameter		Symbol	Test Condition	Min	Typ	Max	Units
Input Side Supply Voltage		VDDA		3.0		5.5	V
Input Supply Current		IVDDA	V_{AIP} = V_{AIN} @ 3.3 V	3.2	4.2	5.5	mA
Output Side Supply Voltage		VDDB		3.0		5.5	V
Output Supply Current		IVDDB	V_{AIP} = V_{AIN} @ 3.3 V	2.3	3.2	4.1	mA
VDD Undervoltage Threshold		VDDUV+	VDDA, VDDB rising		2.7		V
VDD Undervoltage Threshold		VDDUV–	VDDA, VDDB falling		2.6		V
VDD Undervoltage Hysteresis		VDD_{HYS}			100		mV
Amplifier Bandwidth					750		kHz
Amplifier Input							
Specified Full Scale Input Amplitude	Si8920A	VAIP – VAIN		–100		100	mV
	Si8920B			–200		200	mV
Maximum Input Voltage Before Clipping	Si8920A	VAIP – VAIN			±125		mV
	Si8920B				±250		mV
Common-Mode Operating Range		VCM		–0.2		1	V
Input Referred Offset		VOS			0.2	1.5	mV
Input Offset Drift		VOS_T			1.0		µV/°C
Differential Input impedance	Si8920A	RIN			20		kΩ
	Si8920B				37.2		kΩ
Differential Input Impedance Drift		RIN_T			850		ppm/°C
Amplifier Output							
Full-scale Output		VAOP – VAON		1.58	1.62	1.65	Vpk
Gain	Si8920A				16.2		
	Si8920B				8.1		
Gain Error			T_A = 25 °C	–0.5		0.5	%
Gain Error Drift					60		ppm/°C
Output Common Mode Voltage		(VAOP + VAON)/2		1.02	1.1	1.17	V
Output Noise	Si8920A		100 kHz bandwidth		0.14	0.28	mVrms
	Si8920B		100 kHz bandwidth		0.10	0.20	mVrms
Nonlinearity	Si8920A				0.15	0.50	%
	Si8920B				0.10	0.30	%
Output Resistive Load		RLOAD		5			kΩ
Output Capacitive Load		CLOAD				100	pF

Table 1. Electrical Specifications (Continued)

V_{DDA}, V_{DDB} = 5 V, T_A = –40 to +125 °C; typical specs at 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Timing						
Signal Delay	tPD	50% to 50% 50% to 99%		0.75 1.85		µs
Rise Time	tR	10% to 90%		0.42		µs
Common-Mode Transient Immunity*	CMTI	AIP = AIN = AGND, VCM = 1500 V	50	75		kV/µs
***Note:** An analog CMTI failure is defined as an output error of more than 100 mV persisting for at least 1 µs.						

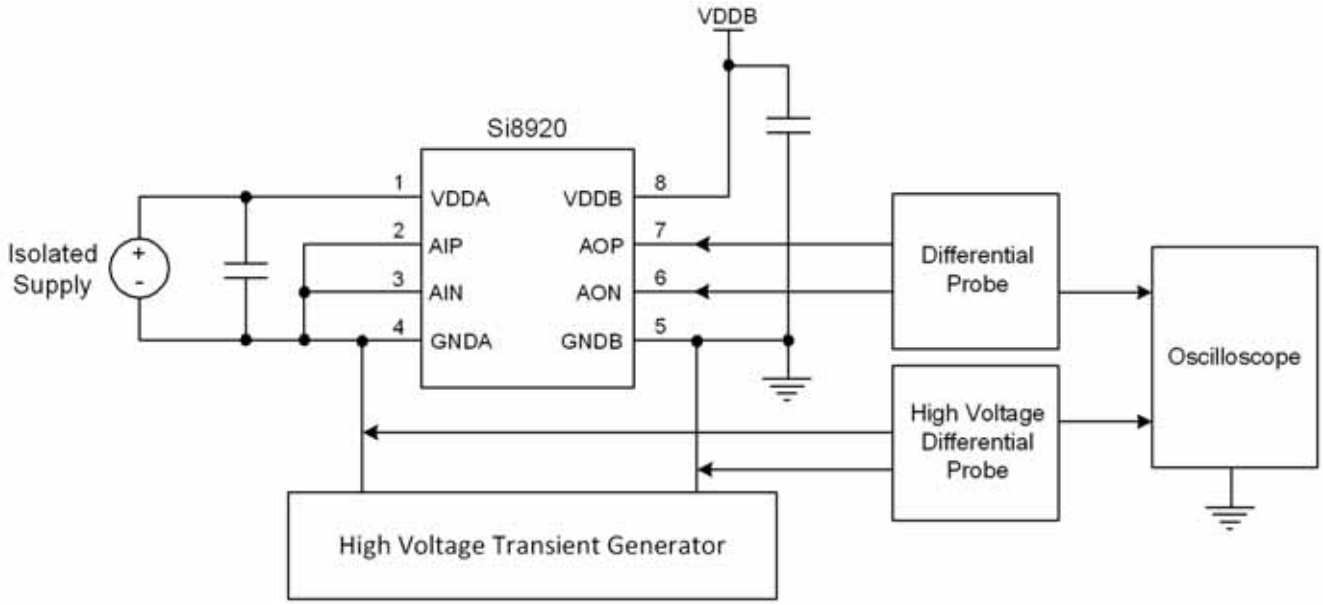


Figure 2. Common Mode Transient Immunity Characterization Circuit

2.1. Regulatory Information

Table 2. Regulatory Information[1,2]

CSA
The Si8920 is certified under CSA Component Acceptance Notice 5A. For more details, see File 232873.
60950-1: Up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
VDE
The Si8920 is certified according to VDE 0884-10. For more details, see File 5006301-4880-0001.
VDE 0884-10: Up to 1200 V_{peak} for reinforced insulation working voltage.
UL
The Si8920 is certified under UL1577 component recognition program. For more details, see File E257455.
Rated up to 5000 V_{RMS} isolation voltage for basic protection.
CQC
The Si8920 is certified under GB4943.1-2011.
Rated up to 600 V_{RMS} reinforced insulation working voltage; up to 1000 V_{RMS} basic insulation working voltage.
Notes: **1.** Regulatory Certifications apply to 5 kV_{RMS} rated devices which are production tested to 6.0 kVRMS for 1 sec. **2.** Regulatory Certifications apply to 3.75 kV_{RMS} rated devices which are production tested to 4.5 kVRMS for 1 sec.

Table 3. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value		Unit
			GW DIP-8	WB SOIC-16	
Nominal Air Gap (Clearance)	L(IO1)		7.2	8.0[1]	mm
Nominal External Tracking (Creepage)	L(IO2)		7.0	8.0[1]	mm
Minimum Internal Gap (Internal Clearance)			0.016	0.016	mm
Tracking Resistance (Proof Tracking Index)	PTI	IEC60112	600	600	V
Erosion Depth	ED		0.031	0.019	mm
Resistance (Input-Output)[2]	R_{IO}		10^{12}	10^{12}	Ω
Capacitance (Input-Output)[2]	C_{IO}	f = 1 MHz	1	1	pF

Notes:

1. The values in this table correspond to the nominal creepage and clearance values. VDE certifies the clearance and creepage limits as 8.5 mm minimum for the WB SOIC-16 package. UL does not impose a clearance and creepage minimum for component-level certifications. CSA certifies the clearance and creepage limits as 7.6 mm minimum for the WB SOIC-16 package.
2. To determine resistance and capacitance, the Si8920 is converted into a 2-terminal device. Pins 1–8 (1–4 DIP8) are shorted together to form the first terminal, and pins 9–16 (5–8 DIP8) are shorted together to form the second terminal. The parameters are then measured between these two terminals.

Table 4. IEC 60664-1 (VDE 0884) Ratings

Parameter	Test Conditions	Specification	
		GW DIP-8	WB SOIC-16
Basic Isolation Group	Material Group	I	I
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-IV	I-IV
	Rated Mains Voltages ≤ 450 V_{RMS}	I-III	I-III
	Rated Mains Voltages ≤ 600 V_{RMS}	I-III	I-III

Table 5. VDE 0884-10 Insulation Characteristics*

Parameter	Symbol	Test Condition	Characteristic		Unit
			GW DIP-8	WB SOIC-16	
Maximum Working Insulation Voltage	V_{IORM}		891	1200	V peak
Input to Output Test Voltage	V_{PR}	Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1671	2250	V peak
Transient Overvoltage	V_{IOTM}	t = 60 sec	6000	8000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	$>10^9$	Ω

***Note:** This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si8920 provides a climate classification of 40/125/21.

Table 6. Absolute Maximum Ratings*

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{STG}	-65	150	°C
Ambient Temperature Under Bias	T_A	-40	125	°C
Junction Temperature	T_J	—	150	°C
Supply Voltage	VDDA, VDDB	–0.5	6.0	V
Input Voltage respect to GNDA	VAIP, VAIN	–0.5	VDD*x*+0.5	V
Output Sink or Source Current	$\|I_O\|$	—	5	mA
Total Power Dissipation	P_T	—	212	mW
Lead Solder Termperature (10 s)		—	260	°C
Human Body Model ESD Rating		4000	—	V
Capacitive Discharge Model ESD Rating PDIP		2000	—	V
Capacitive Discharge Model ESD Rating SOIC		2000	—	V
Maximum Isolation (Input to Output) (1 s) PDIP		—	6500	V_{RMS}
Maximum Isolation (Input to Output) (1 s) SOIC		—	6500	V_{RMS}

***Note:** Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of the data sheet.

3. Typical Operating Characteristics

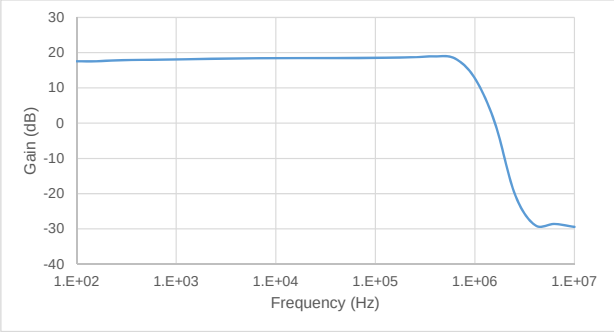


Figure 3. Amplifier Bandwidth

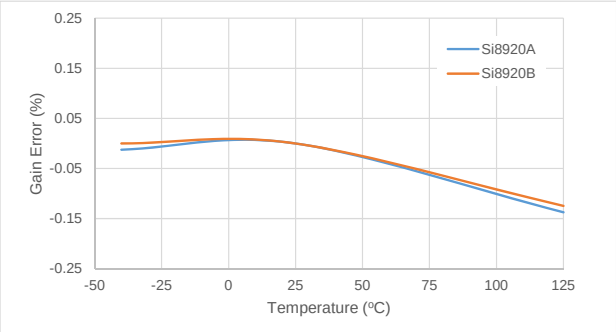


Figure 4. Gain Error vs. Temperature

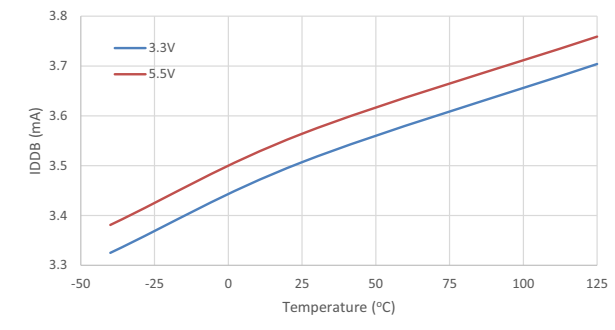


Figure 5. IDDB vs. Temperature

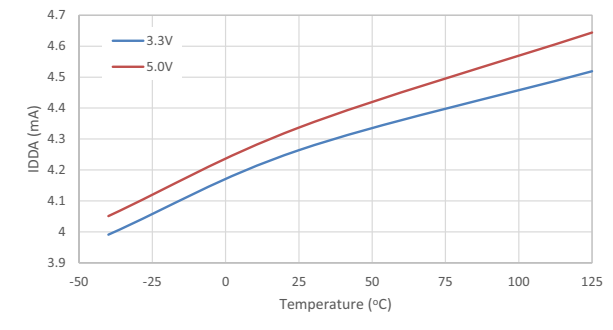


Figure 6. IDDA vs. Temperature

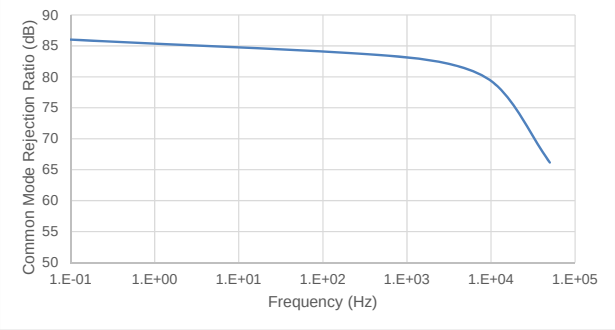


Figure 7. CMRR vs. Frequency

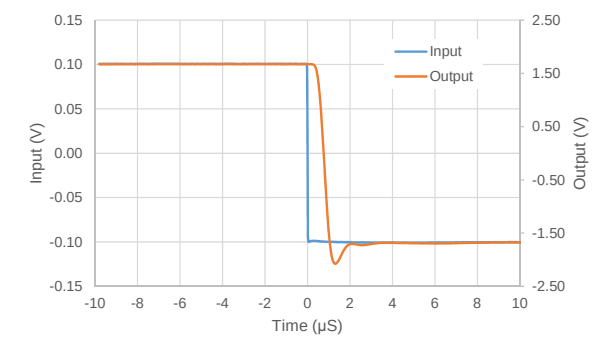


Figure 8. Step Response High to Low

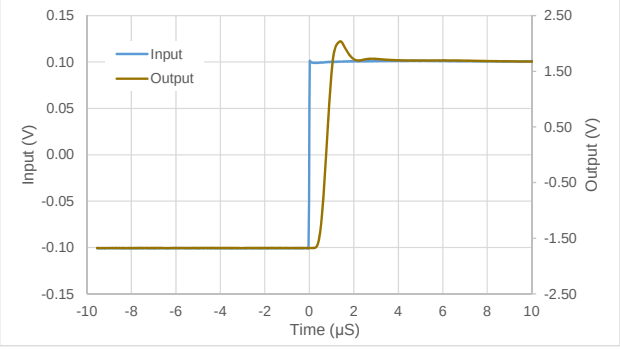


Figure 9. Step Response Low to High

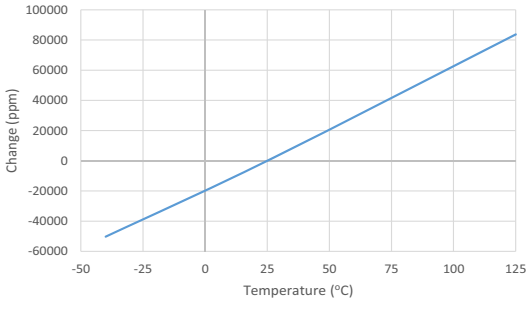


Figure 10. Normalized Differential Input Resistance vs. Temperature

4. Functional Description

The input to the Si8920 is tuned for low-voltage, differential signals. This is ideal for connection to low resistance current shunt measurement resistors. The Si8920A has a full scale input of ±100 mV, and the Si8920B has a full scale input of ±200 mV. In both cases, the internal gain is set so that the full scale output is 1.6 V.

The Si8920 modulates the analog signal in a unique way for transmission across the semiconductor based isolation barrier. The input signal is first converted to a pulse-width modulated digital signal. For transmission across the isolation barrier, the signal is further modulated with a high frequency carrier. On the other side of the isolation barrier, the signal is demodulated and the carrier portion is removed. The resulting PWM signal is then used to faithfully reproduce the analog signal. This solution provides exceptional signal bandwidth and accuracy.

5. Current Sense Application

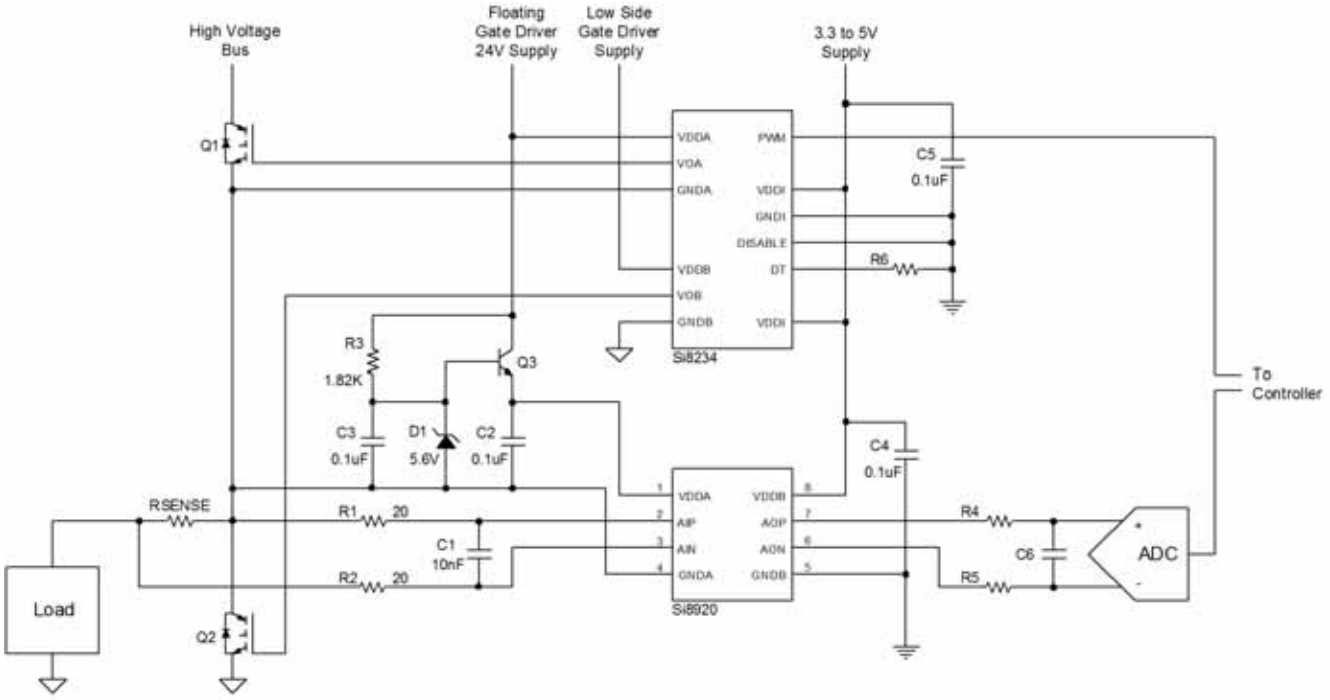


Figure 11. Current Sense Application

In the driver circuit presented in Figure 11, the Si8920 is used to amplify the voltage across the sense resistor, RSENSE, and transmit the analog signal to the low voltage domain across an isolation barrier. Isolation is needed as the voltage of RSENSE with respect to ground will swing between 0 V and the high voltage rail connected to the drain of Q1.

The load in this application can be a motor winding or a similar inductive winding. In a three phase motor drive application, this circuit would be repeated three times, one for each phase. RSENSE should be a small resistor value to reduce power loss. However, too low a resistance will reduce the signal-to-noise of the measurement. Si8920 offers two specified full scale input options, ±100 mV (Si8920A) and ±200 mV (Si8920B) for optimizing the value of RSENSE.

AIP and AIN connections to the RSENSE resistor should be made as close as possible to each end of the RSENSE resistor as trace resistance will add error to the measurement. The input to the Si8920 is differential, and the PCB traces back to the input pins should run in parallel. This ensures that any large noise transients that occur on the high voltage side are coupled equally to the AIP and AIN pins and will be rejected by the Si8920 as a common-mode signal.

The amplifier bandwidth of the Si8920 is approximately 750 kHz. If further input filtering is required, a passive, differential RC low pass filter can be placed between RSENSE and the inputs pins. Values of R1 = R2 = 20 Ω and C1 = 10 nF, as shown in Figure 9, provides a cutoff at approximately 400 kHz. For best gain error, R1 and R2 should always be less than 33 Ω to keep the source impedance sufficiently low compared to the Si8920 input impedance.

The common mode voltage of AIN and AIP must be greater than –0.2 V but less than 1 V with respect to GNDA. To meet this requirement, connect GNDA of the Si8920 to one side RSENSE resistor. In this example GNDA, RSENSE, the source of Q1 and drain of Q2 are connected together. The ground of the gate driver, Silicon Labs' Si8234 in this circuit, is also commonly connected to the same node.

The Q1 gate driver has a floating supply, 24 V in this example. Since the input and output of the Si8920 are galvanically isolated from each other, separate power supplies are necessary on each side. Q3, R3, C3, and D1 make a regulator circuit for powering the input side of the Si8920 from this floating supply. D1 establishes a voltage of 5.6 V at the base of Q3. R3 is selected to provide a zener current of 10 mA for D1. C3 provides filtering at the base of Q3 and the emitter output of Q3 provides approximately 5 V to VDDA. C2 is a bypass capacitor for the supply and should be placed at the VDDA pin with its return trace connecting to the GNDA connection at RSENSE.

C4, the local bypass capacitor for the B-side of Si8920, should be placed closed to VDDB supply pin with its return close to GNDB. The output signal at AOP and AON is differential with a nominal gain of 8.1 (Si8920B) or 16.2 (Si8920A) and common mode of 1.1 V. The outputs are sampled by a differential input ADC. Depending on the sample rate of the ADC, an anti-aliasing filter may be required. R4, C6, and R5 make a simple anti-aliasing filter from passive components. The characteristics of this filter will be dictated by the input topology and sampling frequency of the ADC. However, to ensure the Si8920 outputs are not overloaded, R4 = R5 ≥ 5 kΩ, and C6 can be calculated by the following equation:

$$C6 = \frac{1}{2 \times \pi \times (R4 + R5) \times f_{3dB}}$$

6. Pin Descriptions

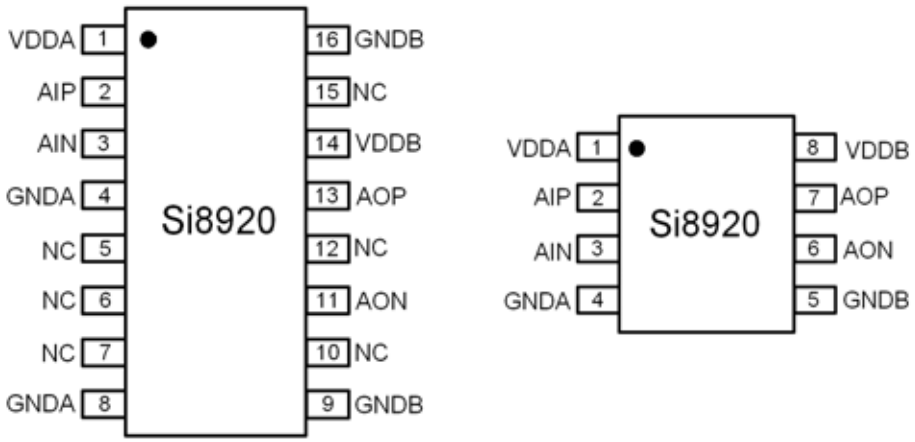


Figure 12. Si8920 Pin Configurations

Table 7. Si8920 Pin Descriptions

Name	WB SOIC-16 Pin #	GW DIP-8 Pin #	Description
VDDA	1	1	Input side power supply
AIP	2	2	Analog input high
AIN	3	3	Analog input low
GNDA	4, 8	4	Input side ground
GNDB	9, 16	5	Output side ground
AON	11	6	Analog output low
AOP	13	7	Analog output high
VDDB	14	8	Output power supply
NC	5, 6, 7, 10, 12, 15	—	No Connect
***Note:** No Connect. These pins are not internally connected. To maximize CMTI performance, these pins should be connected to the ground plane.			

7. Ordering Guide

Table 8. Si8920 Ordering Guide[1,2,3]

New Ordering Part Number (OPN)	Ordering Options		
	Specified Input Range	Isolation Rating	Package Type
Si8920AC-IP	±100 mV	3.75 kVrms	Gull-wing DIP-8
Si8920BC-IP	±200 mV	3.75 kVrms	Gull-wing DIP-8
Si8920AD-IS	±100 mV	5.0 kVrms	WB SOIC-16
Si8920BD-IS	±200 mV	5.0 kVrms	WB SOIC-16

Notes:
1. All packages are RoHS-compliant.
2. “Si” and “SI” are used interchangeably.
3. AEC-Q100 qualified.

8. Package Outline: DIP8

Figure 13 illustrates the package details for the Si8920 in a DIP8 package. Table 9 lists the values for the dimensions shown in the illustration.

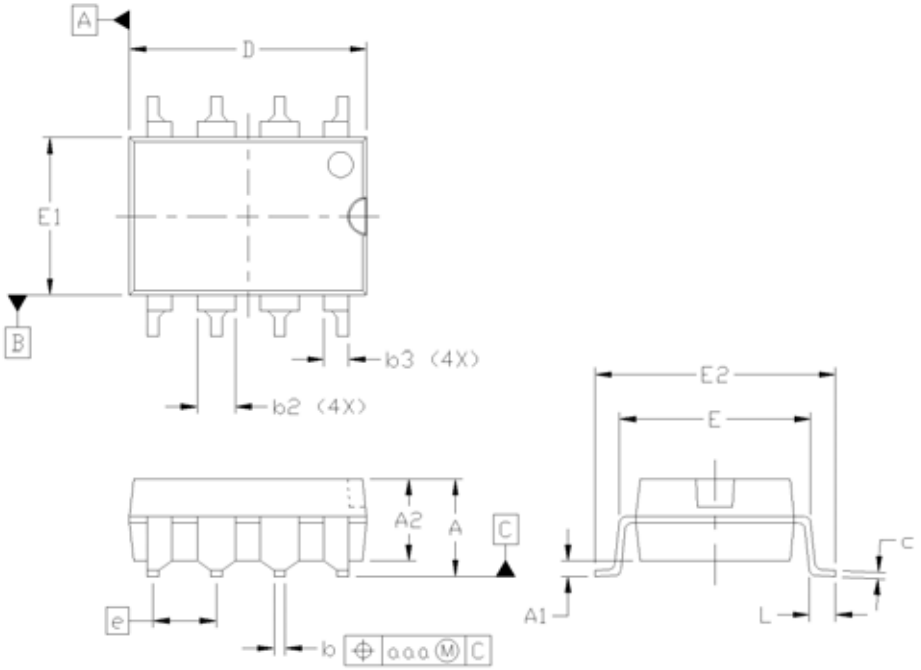


Figure 13. DIP8 Package

Table 9. DIP8 Package Diagram Dimensions

Dimension	Min	Max
A	—	4.19
A1	0.55	0.75
A2	3.17	3.43
b	0.35	0.55
b2	1.14	1.78
b3	0.76	1.14
c	0.20	0.33
D	9.40	9.90
E	7.37	7.87
E1	6.10	6.60
E2	9.40	9.90
e	2.54 BSC.	
L	0.38	0.89
aaa	—	0.25

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

9. Land Pattern: DIP8

Figure 14 illustrates the recommended land pattern details for the Si8920 in a DIP8 package. Table 10 lists the values for the dimensions shown in the illustration.

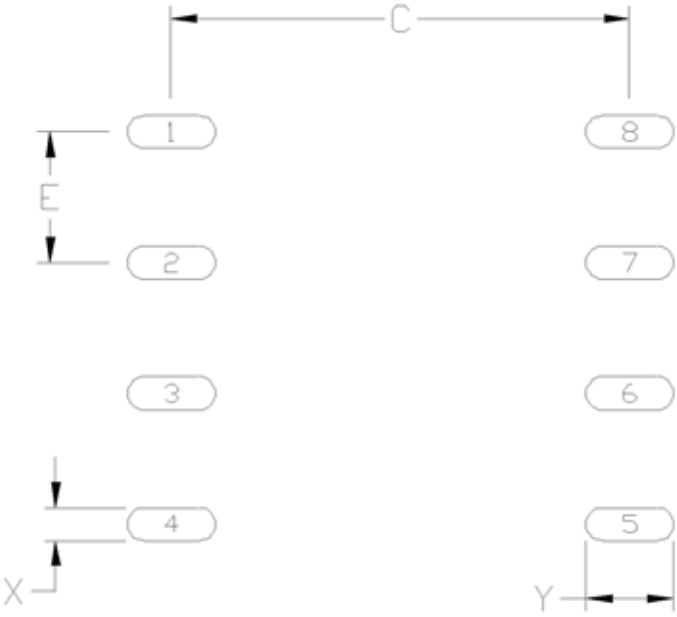


Figure 14. DIP8 Land Pattern

Table 10. DIP8 Land Pattern Dimensions*

Dimension	Min	Max
C	8.85	8.90
E	2.54 BSC	
X	0.60	0.65
Y	1.65	1.70
***Note:** This Land Pattern Design is based on the IPC-7351 specification.		

10. Package Outline: 16-Pin Wide Body SOIC

Figure 15 illustrates the package details for the Si8920 in a 16-Pin Wide Body SOIC. Table 11 lists the values for the dimensions shown in the illustration.

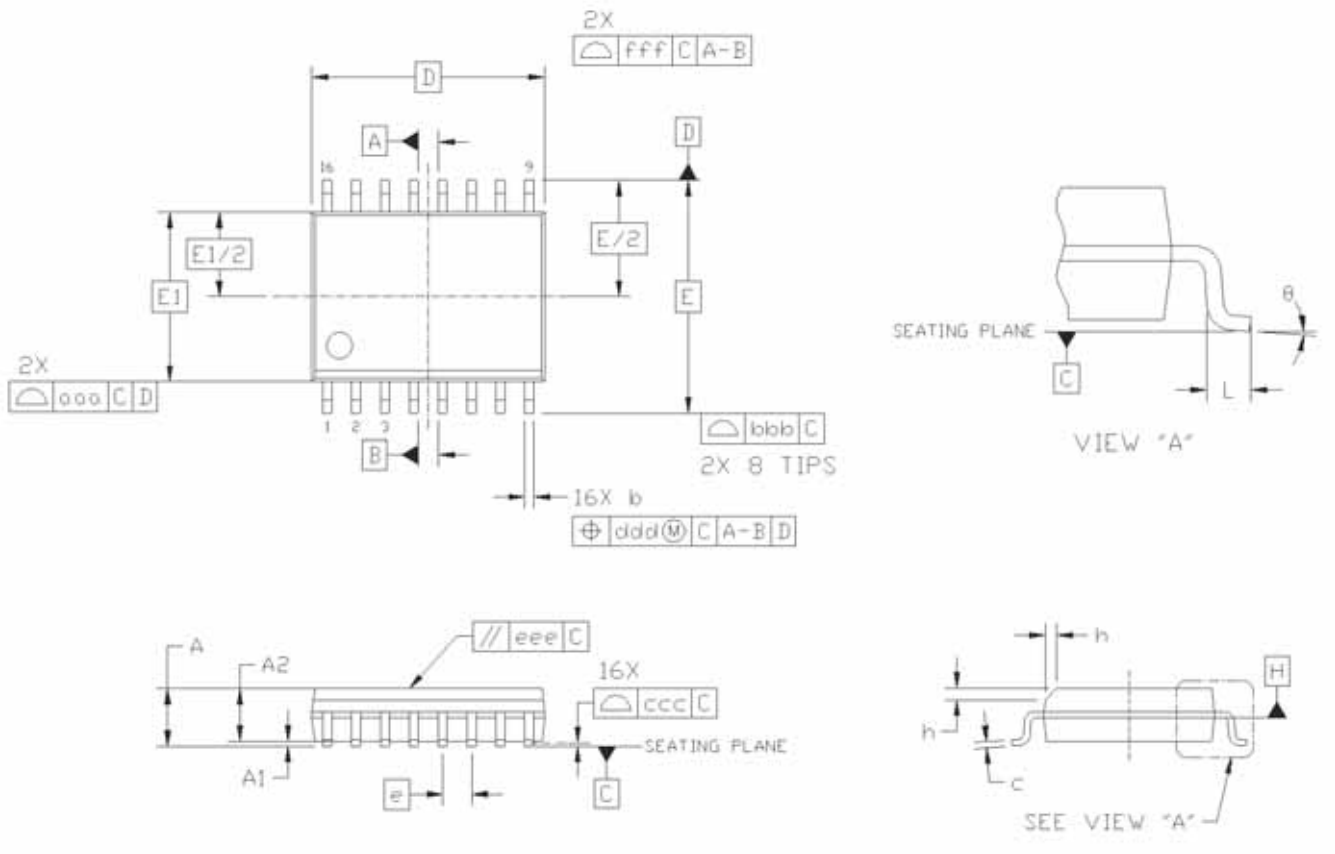


Figure 15. 16-Pin Wide Body SOIC

Table 11. Package Diagram Dimensions

Symbol	Millimeters	
	Min	Max
A	—	2.65
A1	0.10	0.30
A2	2.05	—
b	0.31	0.51
c	0.20	0.33
D	10.30 BSC	
E	10.30 BSC	
E1	7.50 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.75
θ	0°	8°
aaa	—	0.10
bbb	—	0.33
ccc	—	0.10
ddd	—	0.25
eee	—	0.10
fff	—	0.20

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Outline MS-013, Variation AA.
4. Recommended reflow profile per JEDEC J-STD-020C specification for small body, lead-free components.

11. Land Pattern: 16-Pin Wide Body SOIC

Figure 16 illustrates the recommended land pattern details for the Si8920 in a 16-pin wide-body SOIC. Table 12 lists the values for the dimensions shown in the illustration.

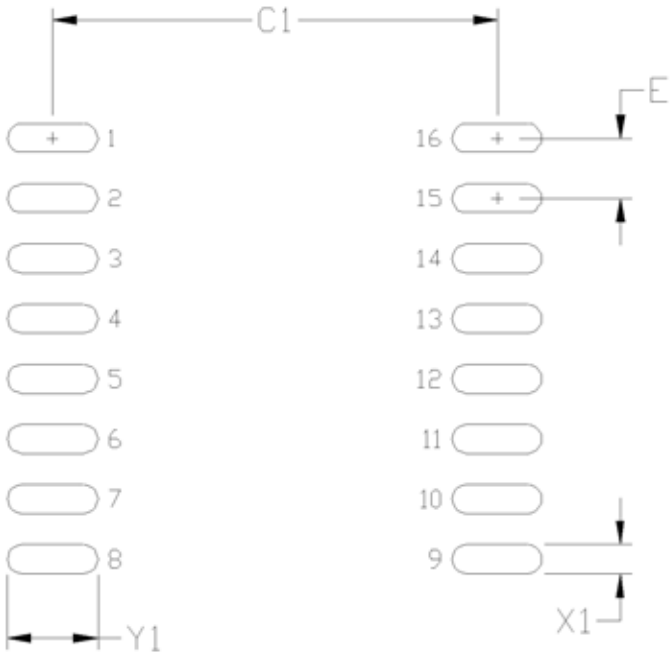


Figure 16. 16-Pin SOIC Land Pattern

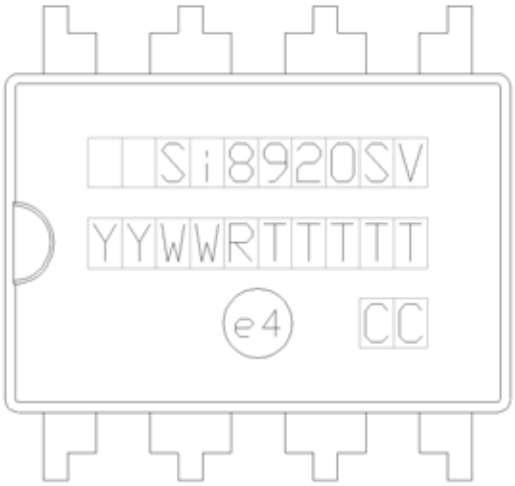
Table 12. 16-Pin Wide Body SOIC Land Pattern Dimensions

Dimension	Feature	(mm)
C1	Pad Column Spacing	9.40
E	Pad Row Pitch	1.27
X1	Pad Width	0.60
Y1	Pad Length	1.90

Notes:
1. This Land Pattern Design is based on IPC-7351 pattern SOIC127P1032X265-16AN for Density Level B (Median Land Protrusion).
2. All feature sizes shown are at Maximum Material Condition (MMC) and a card fabrication tolerance of 0.05 mm is assumed.

12. Top Markings

12.1. Si8920 Top Marking (DIP8)



12.2. Top Marking Explanation (DIP8)

Line 1 Marking:	Customer Part Number	Si8920 = Isolator Amplifier Series S = Input Range: A = ±100 mV B = ±200 mV V = Insulation rating C = 3.75 kV D = 5.0 ,kV
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision.
Line 3 Marking:	Circle = 51 mils Diameter Center-Justified	“e4” Pb-Free Symbol
	Country of Origin (Iso-Code Abbreviation)	CC

12.3. Si8920 Top Marking (SOIC-16)

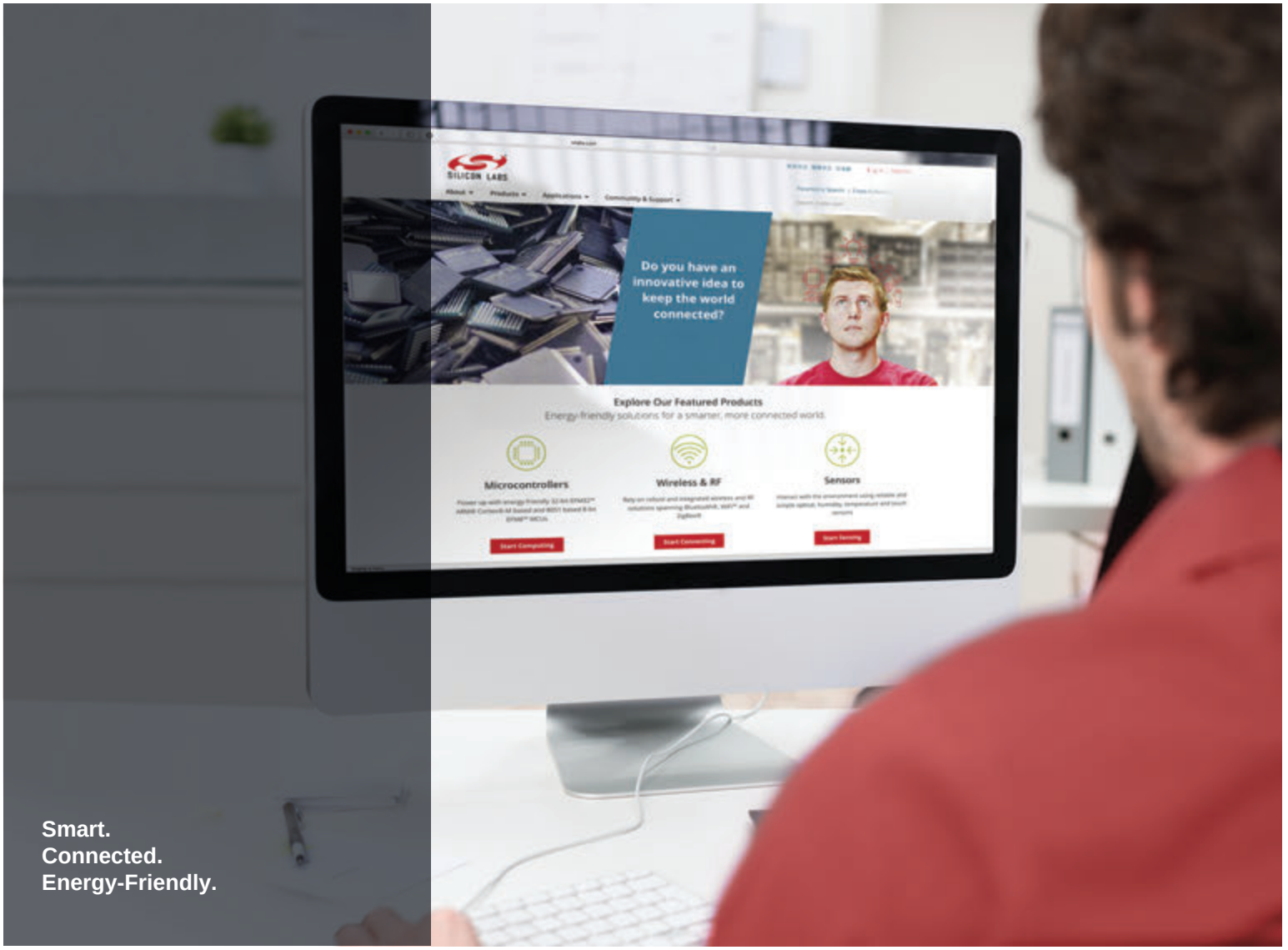
12.4. Top Marking Explanation

Line 1 Marking:	Customer Part Number	Si8920 = Isolator Amplifier Series S = Input Range: A = ±100 mV B = ±200 mV V = Insulation rating C = 3.75 kV D = 5.0 ,kV
Line 2 Marking:	YY = Year WW = Work Week	Assigned by the Assembly House. Corresponds to the year and work week of the mold date.
	RTTTTT = Mfg Code	Manufacturing Code from the Assembly Purchase Order form. “R” indicates revision.
Line 3 Marking:	Circle = 43 mils Diameter Left-Justified	“e4” Pb-Free Symbol

DOCUMENT CHANGE LIST

Revision 0.6 to Revision 0.7

- Updated Figure 13, “DIP8 Package,” on page 16.



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