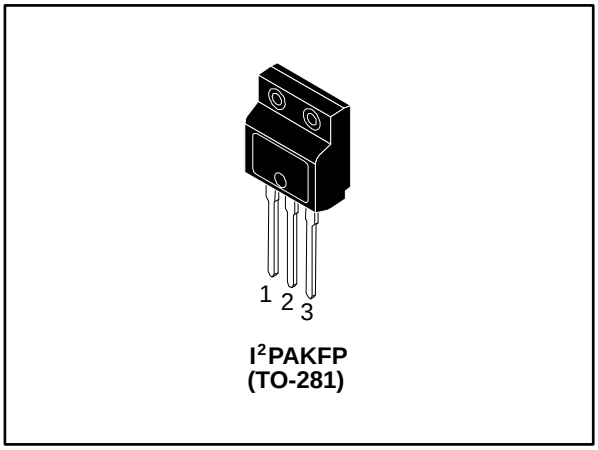
STFI26NM60N

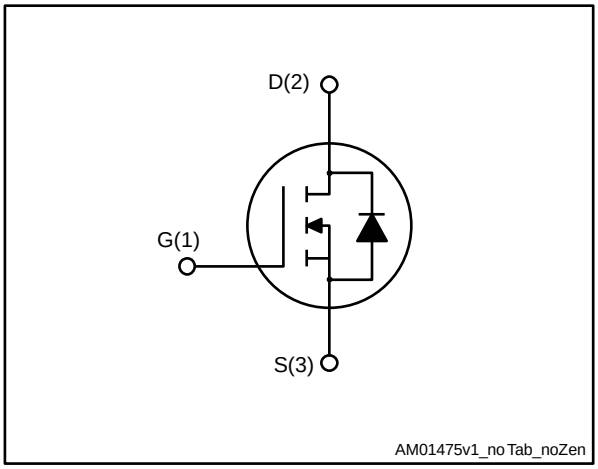
N-channel 600 V, 0.135 Ω typ., 20 A MDmesh™ II Power MOSFET in an I²PAKFP package

Datasheet - production data



I²PAKFP (TO-281)

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max	I_D
STFI26NM60N	600 V	0.165 Ω	20 A

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STFI26NM60N	26NM60N	I²PAKFP (TO-281)	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±30	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	20	A
I_D (1)	Drain current (continuous) at T_C = 100 °C	12.6	A
I_{DM} (1)(2)	Drain current (pulsed)	80	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
dv/dt (3)	Peak diode recovery voltage slope	15	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T_C = 25 °C)	2500	V
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1)Limited by package.

(2)Pulse width limited by safe operating area.

(3)$I_{SD} \le 20$ A, di/dt ≤ 400 A/µs, $V_{DS(peak)} \le V_{(BR)DSS}$, $V_{DD} \le 80\%\ V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	3.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Single pulse avalanche current (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting T_J=25 °C, I_D=I_{AS}, V_{DD}=50 V)	610	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C= 125 °C (1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±0.1	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10 A		0.135	0.165	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0 V	-	1800	-	pF
C_{oss}	Output capacitance		-	115	-	pF
C_{rss}	Reverse transfer capacitance		-	6	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 480 V	-	310	-	pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 20 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	60	-	nC
Q_{gs}	Gate-source charge		-	8.5	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC
R_G	Gate input resistance	f=1 MHz, I_D=0 A	-	2.8	-	Ω

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 10 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	13	-	ns
t_r	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
t_f	Fall time		-	50	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (1)	Source-drain current		-		20	A
I_{SDM} (2)	Source-drain current (pulsed)		-		80	A
V_{SD} (3)	Forward on voltage	I_{SD} = 20 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	370		ns
Q_{rr}	Reverse recovery charge		-	5.8		µC
I_{RRM}	Reverse recovery current		-	31.6		A
t_{rr}	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	450		ns
Q_{rr}	Reverse recovery charge		-	7.5		µC
I_{RRM}	Reverse recovery current		-	32.5		A

Notes:

(1)Limited by package.

(2)Pulse width limited by safe operating area.

(3)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

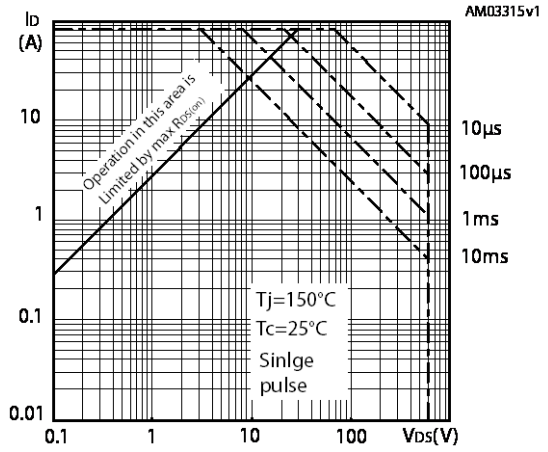


Figure 3: Thermal impedance

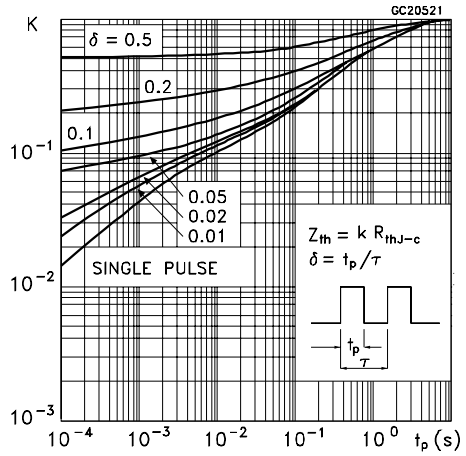


Figure 4: Output characteristics

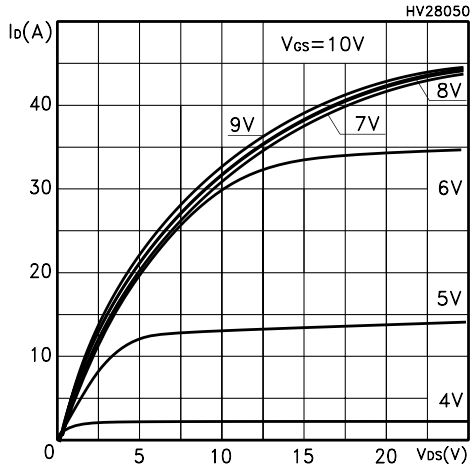


Figure 5: Transfer characteristics

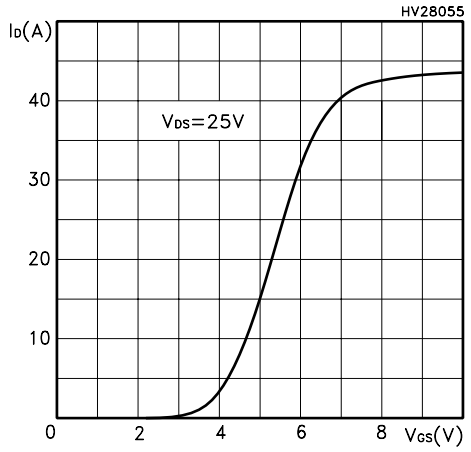


Figure 6: Gate charge vs gate-source voltage

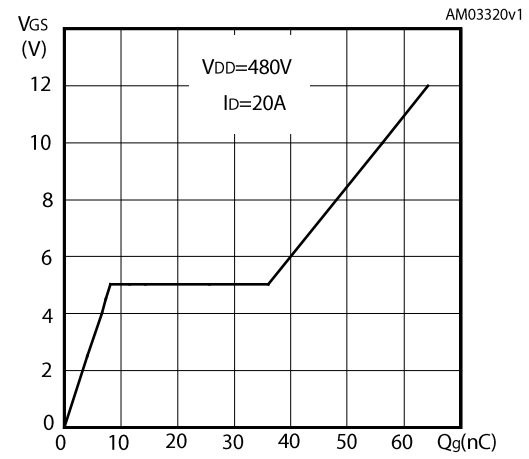


Figure 7: Static drain-source on-resistance

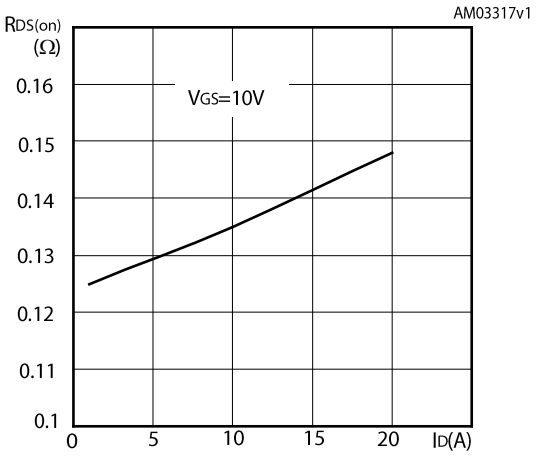


Figure 8: Capacitance variations

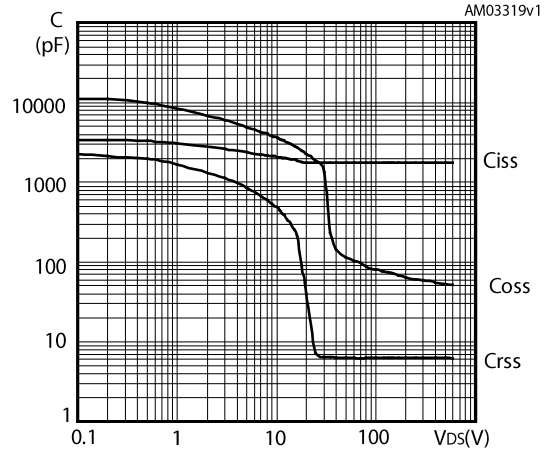


Figure 9: Source-drain diode forward characteristics

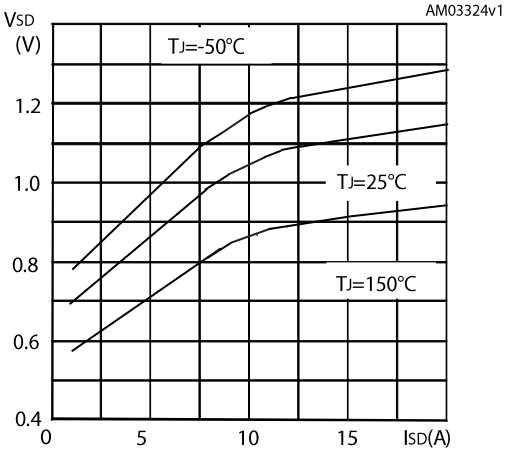


Figure 10: Normalized gate threshold voltage vs temperature

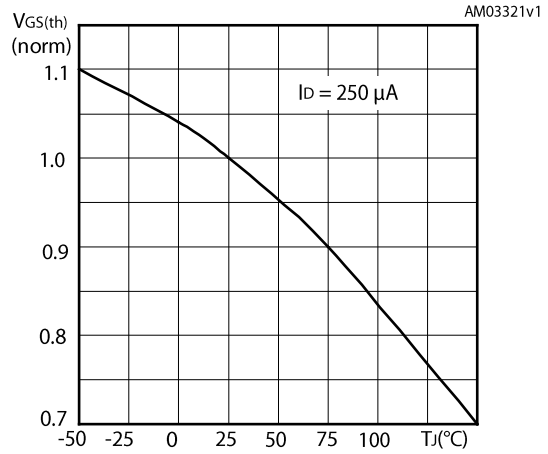


Figure 11: Normalized on-resistance vs temperature

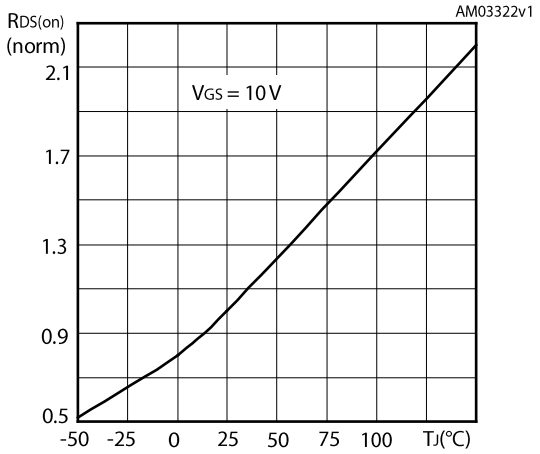
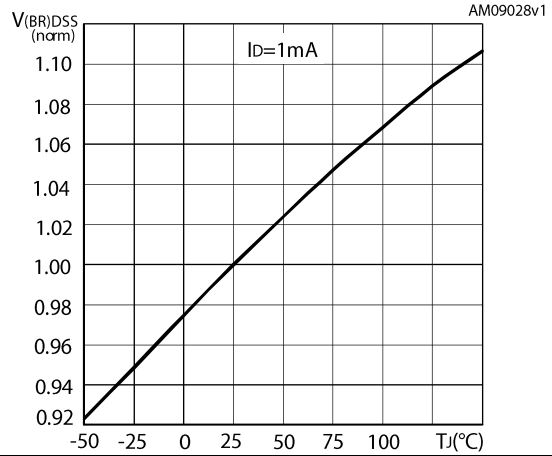


Figure 12: Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13: Test circuit for resistive load switching times

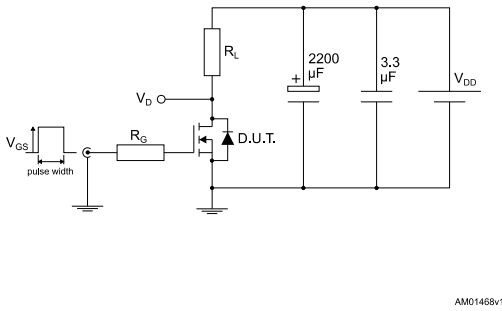


Figure 14: Test circuit for gate charge behavior

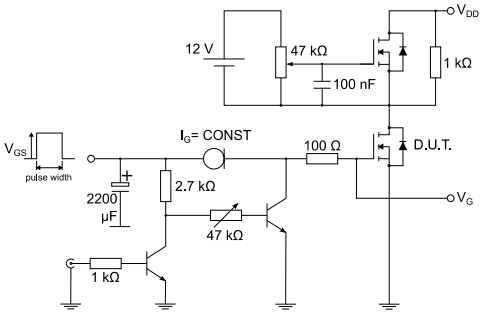


Figure 15: Test circuit for inductive load switching and diode recovery times

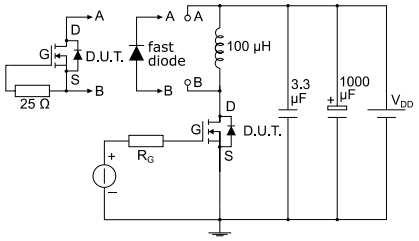


Figure 16: Unclamped inductive load test circuit

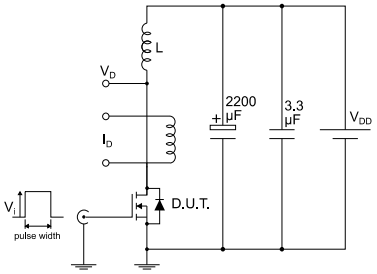


Figure 17: Unclamped inductive waveform

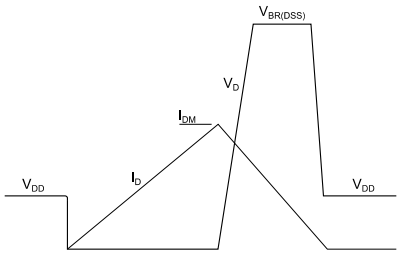
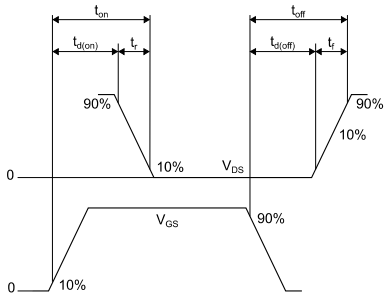


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 I²PAKFP package information

Figure 19: I²PAKFP (TO-281) package outline

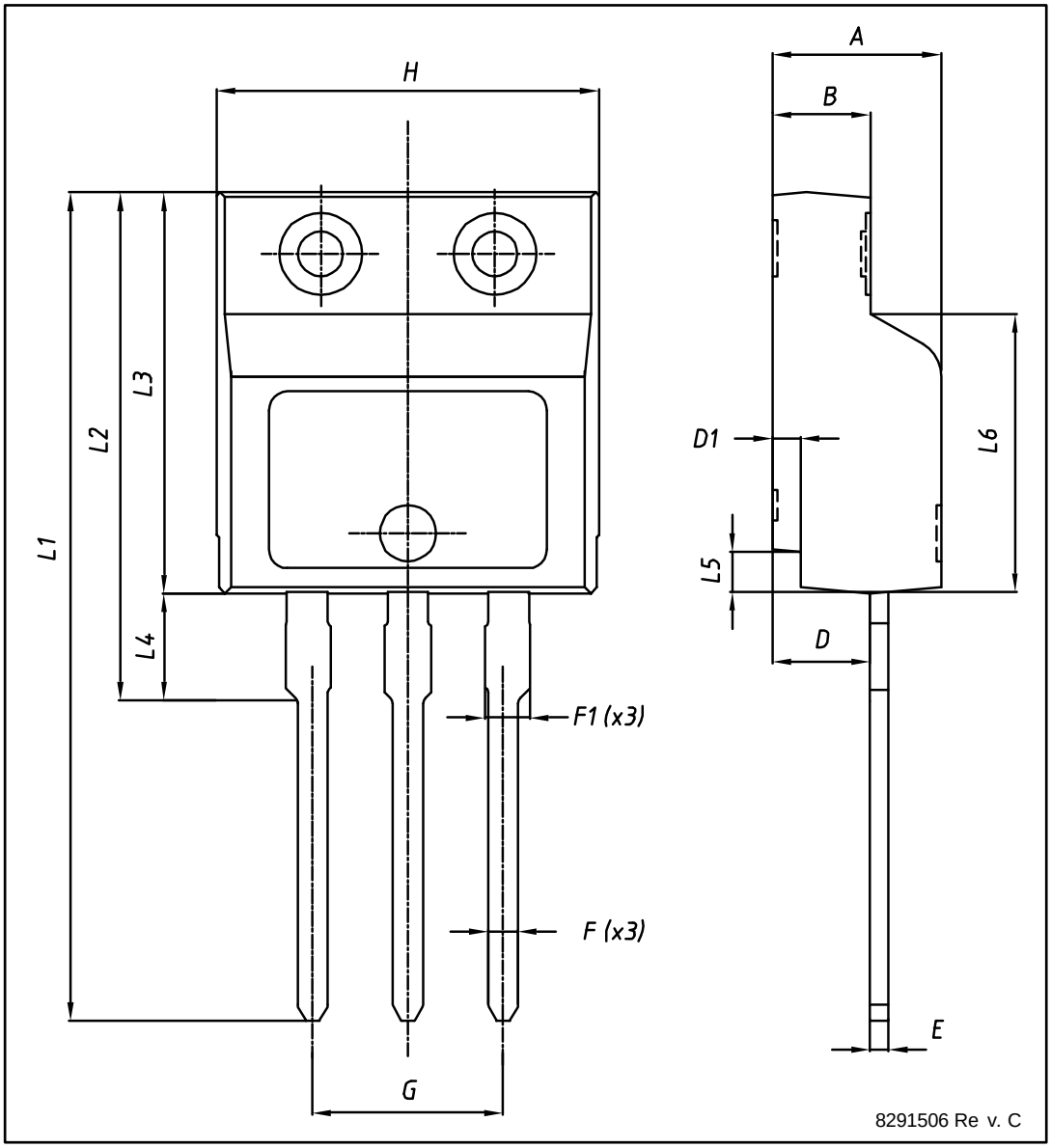


Table 9: I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
15-Nov-2011	1	First release.
04-Jun-2012	2	Document status promoted from preliminary data to production data. Updated P_{TOT} and Derating factor values in *Table 2: Absolute maximum ratings*, $R_{th\text{-}case}$ value in *Table 3: Thermal data* Package name has been updated.
10-Jun-2015	3	Updated *Section 4: Package information.*Minor text changes.
13-Dec-2016	4	Modified *Table 2: "Absolute maximum ratings"*, *Table 5: "On/off states"*, *Table 6: "Dynamic"* and *Table 8: "Source-drain diode"* Modified *Section 2.1: "Electrical characteristics (curves)"* Minor text changes

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