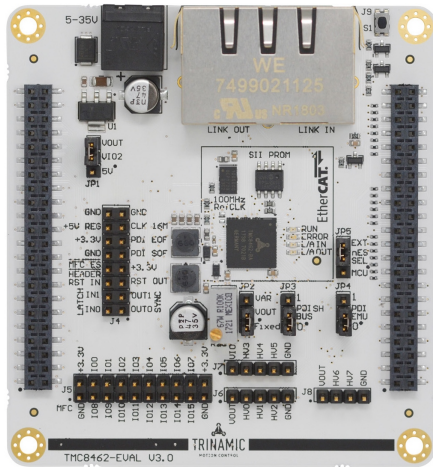


TMC8462-EVAL

Document Revision V1.00 • 2018-June-15

The TMC8462-EVAL is designed for evaluating all features of the TMC8462-BA EtherCAT Slave Controller. It can be used as bus interface module for EtherCAT applications.



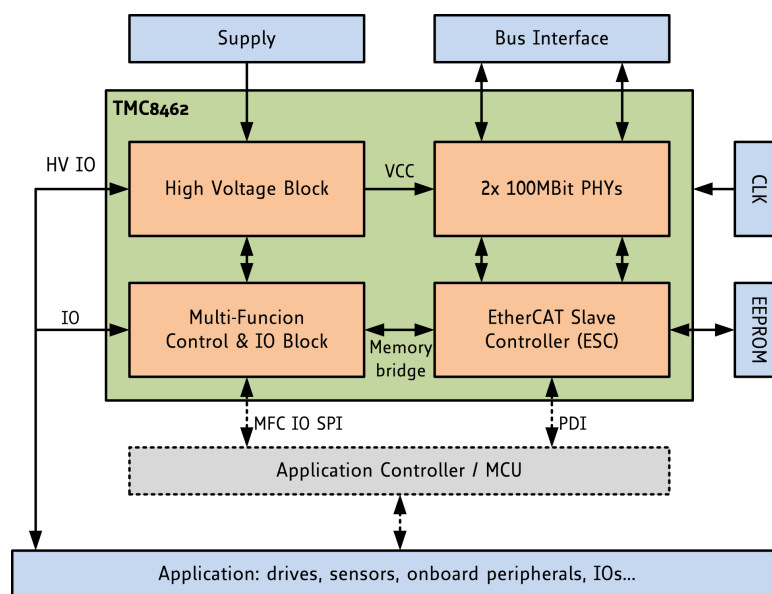
Features

- TMC8462-BA EtherCAT Slave Controller
- Board supply voltage: 5V to 35V
- Dual RJ45 TPC connector
- SPI PDI interface
- SPI interface for TRINAMIC's Multi-Function and Control IO Block (MFC IO)
- Access to all chip functions via pin headers and connectors
- Interface to TRINAMIC's evaluation board concept
- CAD design files available for download on www.trinamic.com

Applications

- Laboratory Automation
- Semiconductor Handling
- Factory Automation
- Drives
- Robotics
- Connected Sensors

Simplified Block Diagram



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1 Getting Started

You need

- TMC8462-EVAL
- TRINAMIC's [Landungsbruecke](#) or [Startrampe](#)
- Firmware for [Landungsbruecke](#) or [Startrampe](#) with simple implementation of the ESM (EtherCAT State Machine)
- Eselsbruecke connector board
- Power Supply 5V-35V for the evaluation board itself
- Latest [TMCL-IDE](#)
- RJ45 TPC cable
- EtherCAT master system (Beckhoff TwinCAT, SOEM, Omron, Ancosys...)
- Additional cables you need for your setup

Precautions

- Do not mix up connections or short-circuit pins.
- Do not exceed the maximum rated supply supply voltage!
- START WITH POWER SUPPLY OFF!

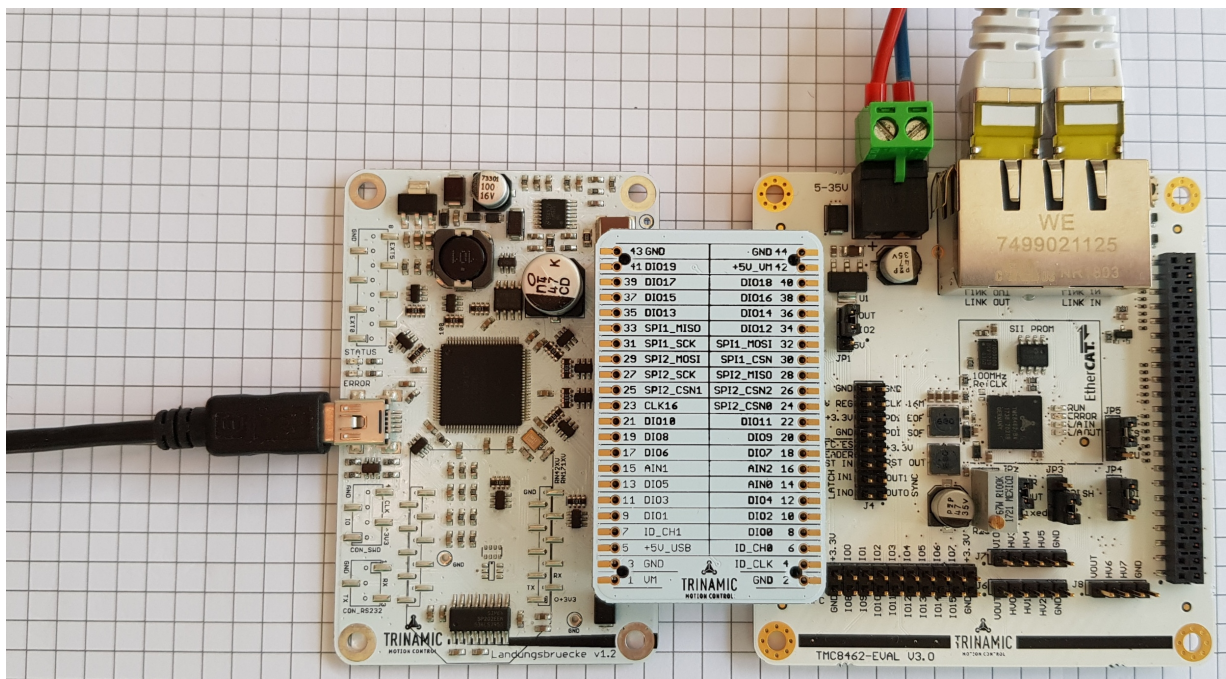


Figure 1: TMC8462-EVAL kit with Landungsbruecke, Eselsbruecke and TMC8462-EVAL

NOTICE

The Landungsbruecke operates on USB Power Supply. All other voltages are generated from the evaluation board supply 5V-35V. The kit works only when both supplies are connected.



1.1 First Start-Up

1. Make sure that the latest version of the TMCL-IDE is installed. The TMCL-IDE can be downloaded from www.trinamic.com/support/software/tmcl-ide/.
2. Open the TMCL-IDE and connect the Landungsbruecke or Startrampe via USB to the computer. For Windows 10 no extra USB driver needed. On Windows 7 and 8 machines the TMCL-IDE can install the driver automatically.
3. Verify that the Landungsbruecke or Startrampe is using the latest firmware version. The firmware version is shown in the connected device tree. The latest firmware is always available online at <https://www.trinamic.com/support/eval-kits/details/landungsbruecke/> or <https://www.trinamic.com/support/eval-kits/details/startrampe/>

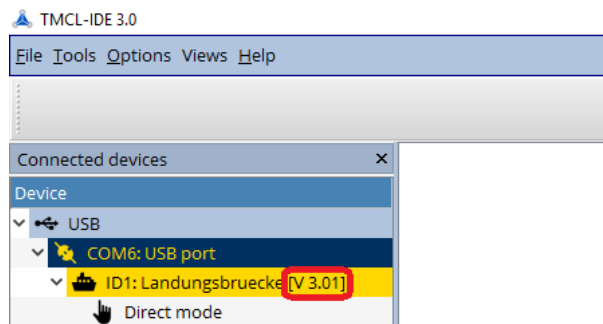


Figure 2: Firmware Version

4. The TMCL-IDE needs room to show all important information and to provide a good overview. Therefore, arrange the main window related to your needs. We recommend using full screen.

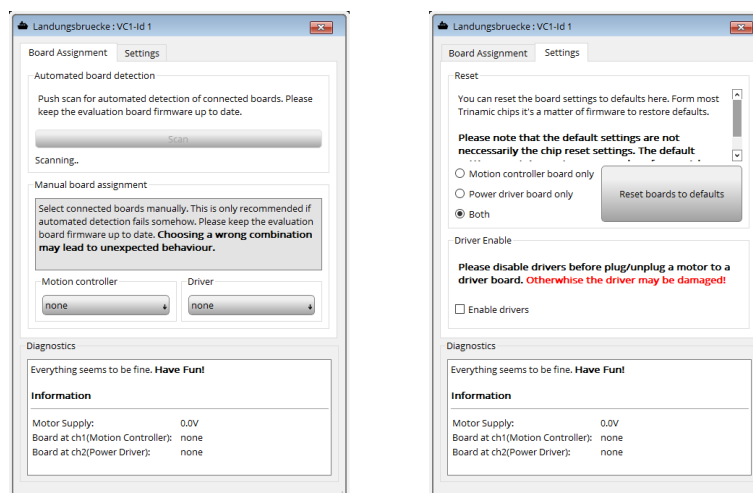


Figure 3: Landungsbruecke Dialogue

5. The TMCL-IDE includes a dialogue for diagnostic tasks for the controller board. Further, the dialogue provides an overview of the connected evaluation board (controller and/or driver). The TMC8462-EVAL should appear under "controller" by automatic detection. In case it does not appear, the evaluation board can also be selected manually. A window should pop up immediately after connecting the



evaluation kit the first time. The window shows the general status of the connected evaluation board. The second tab of the dialogue offers the possibility to choose basic settings or to reset the module.

NOTICE

With TMC8462-EVAL of version V3.0 the automatic detection is not possible. The board must be manually selected in "Motion Controller" drop down list. With TMC8462-EVAL of version V3.1 or higher, the automatic detection of the evaluation board is working properly.

6. If not yet done also connect your Ethernet TPC cables into the RJ45 bus connections of the TMC8462-EVAL to connect to other EtherCAT slaves and your EtherCAT master system.
7. For operation with the Landungsbruecke and the TMCL-IDE please make sure that JP3 on the evaluation board is set on positions 1-2. This should basically be the default factory setting. It configures the SPI channels mode. Setting 1-2 is required for the Landungsbruecke.



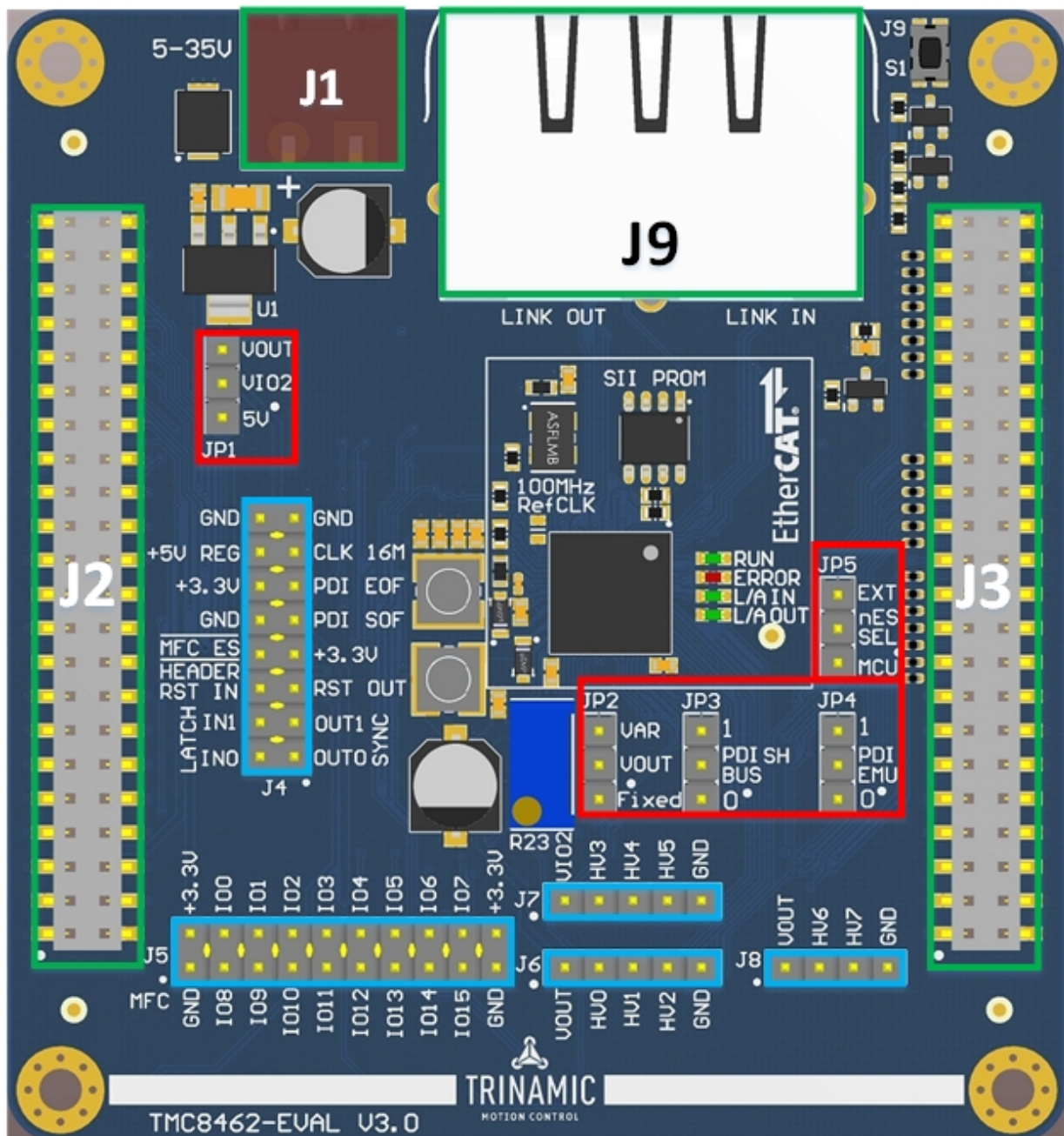


Figure 4: Top view of TMC8462-EVAL

2 Evaluation Board Sections and Components

Figure 4 top view of the TMC8462-EVAL shows the main connectors (green), signal pin headers (light blue), and jumper options (red).

The on-chip reset circuit takes care for proper power-on reset.

The tactile switch S1 in the upper right corner triggers a manual reset of the ESC and the PHYs.



2.1 Evaluation Board Connectors

| Connector ID | Description |
|--------------|--|
| J1 | Power supply connector for the evaluation board. Connect Ground and Supply here (5V-35V). Type: AKL320-02 by RIA |
| J2 | Left side 44-pin connector with control signals going to TRINAMIC's Landungsbruecke or Startrampe controller board or a users own controller board. The Eselsbruecke connector board fits onto this connector. Type: HLE-122-02-F-DV by Samtec |
| J3 | Right side 44-pin connector with configurable MFC IO signals of TMC8462-BA. Type: HLE-122-02-F-DV by Samtec |
| J9 | Double RJ45 twisted pair copper (TPC) connector to connect the TMC8462-EVAL to the EtherCAT bus. 10/100BaseT with integrated transformers. Type: 7499021125 by Wuerth Elektronik |

Table 1: Board connectors

Please check the online available design files and schematic data for the connectors' signal connections and pinning.

2.2 Evaluation Board Pin Headers

There are 5 pin header groups on the TMC8462-EVAL- J4 to J8.

| Pin Header ID | Description |
|---------------|--|
| J4 | General control signals |
| J5 | MFC IO 16x low-voltage/digital IOs |
| J6 | MFC IO 3x high-voltage IOs, pin group 1 using VIO1 |
| J7 | MFC IO 3x high-voltage IOs, pin group 2 using VIO2 |
| J7 | MFC IO 2x high-voltage IOs, pin group 3 using VIO3 |

Table 2: Pin header groups

J4 contains various control and debug signals.

The distributed clocks synchronization output trigger signals and input latch signals are available along with some PDI debug signals.

Using a 2-pin jumper bridge across pin 5 and pin 6 (RESET_OUT to RST_IN) enables using the internal reset signal of the ESC. Thereby, the EtherCAT master or the local host can issue a TMC8462-BA device reset by writing a special character sequence into ESC registers 0x0040 or 0x0041.

| Pin # | Description | Pin # | Description |
|-------|---------------------------------|-------|-------------|
| 1 | SYNC_OUT0 | 2 | LATCH_IN0 |
| 3 | SYNC_OUT1 | 4 | LATCH_IN1 |
| 5 | RESET_OUT | 6 | RST_IN |
| 7 | +3.3V (= TMC8462-BA SW0 output) | 8 | MFC_NES_EXT |



| Pin # | Description | Pin # | Description |
|-------|---------------|-------|---------------------------------|
| 9 | PDI_SOF | 10 | GND |
| 11 | PDI_EOF | 12 | +3.3V (= TMC8462-BA SW0 output) |
| 13 | CLK_16MHZ_OUT | 14 | +5V (from LDO U1) |
| 15 | GND | 16 | GND |

Table 3: Pin header J4 pinning – general control signals

J5 allows access to all 16 low-voltage MFC IOs. They are using VCCIO = +3.3V. The actual function of these 16 MFC IOs is defined by the configuration of the MFC IO block's crossbar matrix and functional sub-blocks.

| Pin # | Description | Pin # | Description |
|-------|-------------|-------|---------------------------------|
| 1 | GND | 2 | +3.3V (= TMC8462-BA SW0 output) |
| 3 | MFCIO08 | 4 | MFCIO00 |
| 5 | MFCIO09 | 6 | MFCIO01 |
| 7 | MFCIO10 | 8 | MFCIO02 |
| 9 | MFCIO11 | 10 | MFCIO03 |
| 11 | MFCIO12 | 12 | MFCIO04 |
| 13 | MFCIO13 | 14 | MFCIO05 |
| 15 | MFCIO14 | 16 | MFCIO06 |
| 17 | MFCIO15 | 18 | MFCIO07 |
| 19 | GND | 20 | +3.3V (= TMC8462-BA SW0 output) |

Table 4: Pin header J5 pinning – MFC IO 16x low-voltage/digital IOs

J6, J7, and J8 allow access to all 8 high-voltage MFC IOs. The voltage at these pins is configurable and can be up to the supply voltage. The 8 high-voltage MFC IOs are divided into three groups where each group has its own supply voltage. On the TMC8462-EVAL VIO1 and VIO2 are the same and directly driven by VOUT. VIO2 can be selected using The actual function of these 8 MFC IOs is defined by the configuration of the MFC IO block's crossbar matrix and functional sub-blocks.

| Pin # | Description |
|-------|--|
| 1 | VOUT (= TMC8462-BA SW1 output, configurable) |
| 2 | MFCHVIO00 |
| 3 | MFCHVIO01 |
| 4 | MFCHVIO02 |
| 5 | GND |

Table 5: Pin header J6 pinning – MFC IO 3x high-voltage IOs, pin group 1 using VIO1



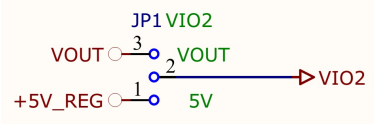
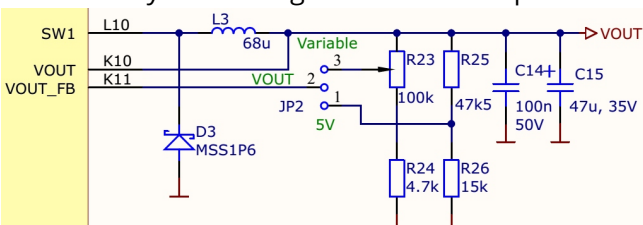
| Pin # | Description |
|-------|--------------------------------------|
| 1 | VIO2 (= selectable and configurable) |
| 2 | MFCHVIO03 |
| 3 | MFCHVIO04 |
| 4 | MFCHVIO05 |
| 5 | GND |

Table 6: Pin header J7 pinning – MFC IO 3x high-voltage IOs, pin group 2 using VIO2

| Pin # | Description |
|-------|--|
| 1 | VOUT (= TMC8462-BA SW1 output, configurable) |
| 2 | MFCHVIO06 |
| 3 | MFCHVIO07 |
| 4 | GND |

Table 7: Pin header J8 pinning – MFC IO 2x high-voltage IOs, pin group 3 using VIO3

2.3 Evaluation Board Jumper Settings

| Jumper ID | Default Connection Pins | Description |
|-----------|-------------------------|--|
| JP1 | 2-3 | <p>JP1 selects the voltage used for bank 2 of the high voltage IOs VIO2. The default setting selects VOUT of the configurable buck regulator of TMC8462-BA. The VOUT itself can further be selected with JP2. The second option of JP1 is to use a dedicated fixed 5V voltage regulator output.</p>  |
| JP2 | 1-2 | <p>JP2 selects the configuration for the output voltage of the configurable internal buck regulator of TMC8462-BA. The default setting ("fixed") uses a voltage divider configuration for VOUT = 5V. The second option ("VAR") allows directly controlling VOUT with the potentiometer R23.</p>  |



| Jumper ID | Default Connection Pins | Description |
|-----------|-------------------------|--|
| JP3 | 1-2 | <p>JP3 selects the configuration of the two SPI control interfaces of TMC8462-BA (PDI SPI interface and MFC IO SPI interface). The default setting configures the interfaces to be two separate SPI buses with individual control and data signals. The second option is to physically share the PDI SPI bus and also allow access to the MFC IO SPI via the second chip select line.</p> |
| JP4 | 1-2 | <p>JP4 selects the EtherCAT operation mode of TMC8462-BA. With the default setting, the EtherCAT slave controller operates in standard mode. TMC8462-BA thereby expects a controller including an EtherCAT State Machine (ESM) implementation at the PDI interface. The second option is to start-up the ESC in so-called PDI- or device-emulation mode, which allows operation without an external controller. State changes are then directly executed in hardware in the ESC.</p> |
| JP5 | 2-3 | <p>JP5 selects the actual source of the low active (not) emergency switch input MFC_NES. MFC_NES has a weak internal pull down and must be driven high for normal operation. The default setting of JP5 configures the source of MFC_NES coming from pin header J4 at pin 8. The second option is that MFC_NES is driven by pin 23 of the 44-pin connector J2, for example by a connected TRINAMIC Landungsbruecke controller board.</p> |

Table 8: Board jumper options and defaults




```
</ImageData16x14>  
87 </Device>  
</Devices>  
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</EtherCATInfo>
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5 Revision History

5.1 Document Revision

| Version | Date | Author | Description |
|---------|------------|--------|------------------------------------|
| 1.00 | 2018-02-26 | SK | Initial release. |
| 1.10 | 2018-06-15 | SK | Update of getting started section. |

Table 9: Document Revision

