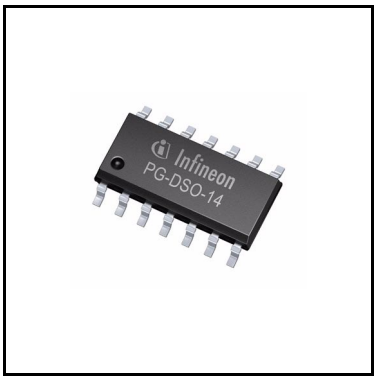
TLE6251-2G

High Speed CAN Transceiver with Wake and Failure Detection

AEC Qualified RoHS



1 Overview

Features

- HS CAN Transceiver with data transmission rate up to 1 MBaud
- Compliant to ISO 11898-5
- Very low power consumption in Sleep mode
- Bus Wake-Up and local Wake-Up
- Inhibit output to control external circuitry
- Split termination to stabilize the recessive level
- Separate V_{IO} input to adapt different micro controller supply voltages
- Separate output for failure diagnosis
- Optimized for low electromagnetic emission (EME)
- Optimized for a high immunity against electromagnetic interference (EMI)
- Very high ESD robustness, ±9 kV according to IEC 61000-4-2
- Protected against automotive transients
- Receive-Only mode for node failure analysis
- TxD time-out function and RxD recessive clamping with failure indication
- TxD to RxD short circuit recognition with failure indication
- CANH and CANL short circuit recognition with failure indication
- Bus dominant clamping diagnosis
- Under-voltage detection at V_{CC}, V_{IO} and V_S
- Power-Up and Wake-Up source recognition
- Short circuit proof and Over-Temperature protection
- Green Product (RoHS compliant)
- AEC Qualified

Applications

- Mixed power supply HS-CAN networks

Description

As a successor of the TLE6251G, the TLE6251-2G is designed to provide an excellent passive behavior in Power Down. This feature makes the TLE6251-2G extremely suitable for mixed power supply HS-CAN networks. The TLE6251-2G provides different operation modes with a very low quiescent current in Sleep mode. Based on the high symmetry of the CANH and CANL signals, the TLE6251-2G provides a very low level of electromagnetic

emission (EME) within a broad frequency range. The TLE6251-2G is integrated in a RoHS compliant PG-DSO-14 package and fulfills or exceeds the requirements of the ISO11898-5. The TLE6251G and the TLE6251-2G are fully pin compatible and function compatible.

Type	Package	Marking
TLE6251-2G	PG-DSO-14	TLE6251-2G

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2 Block Diagram

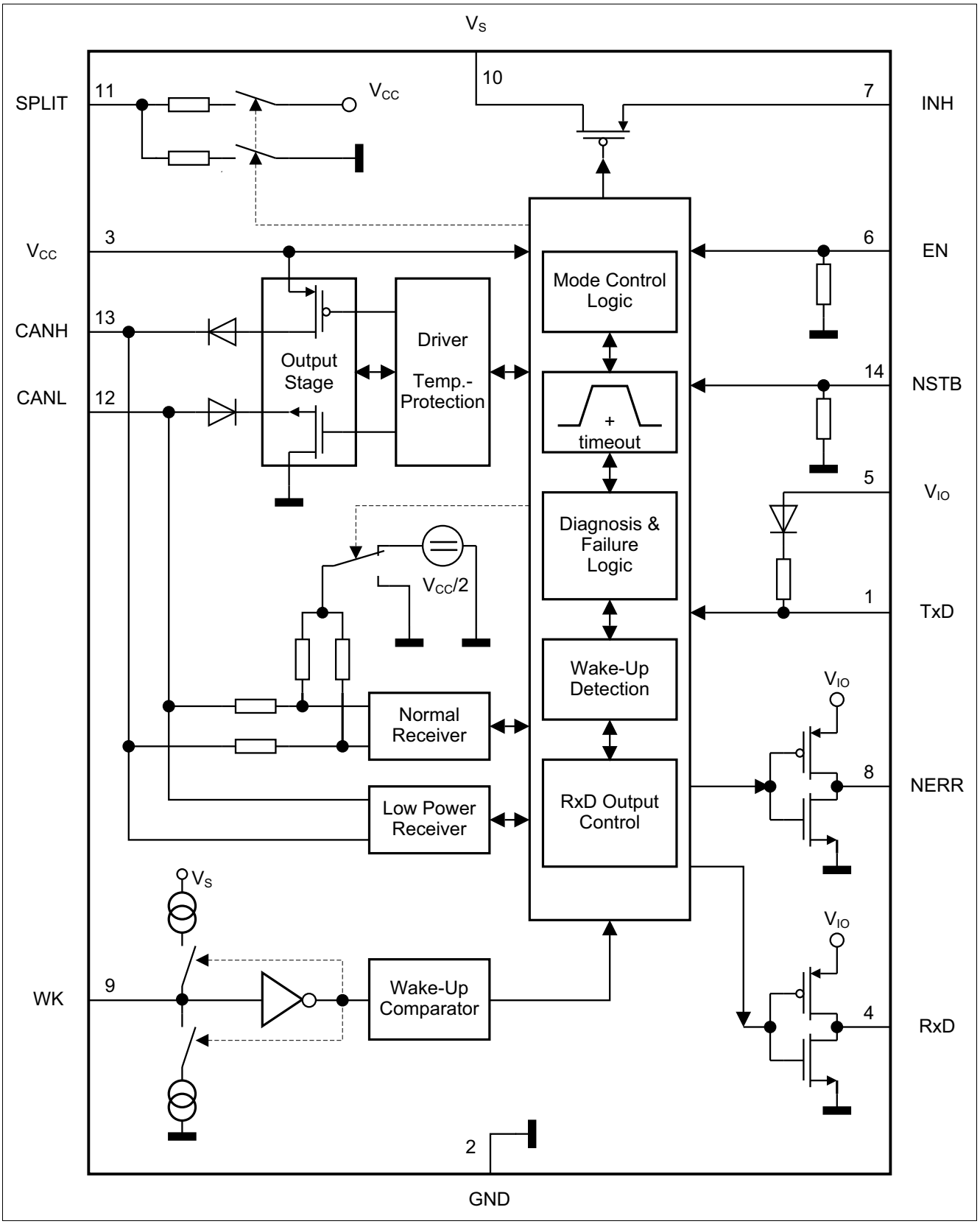


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

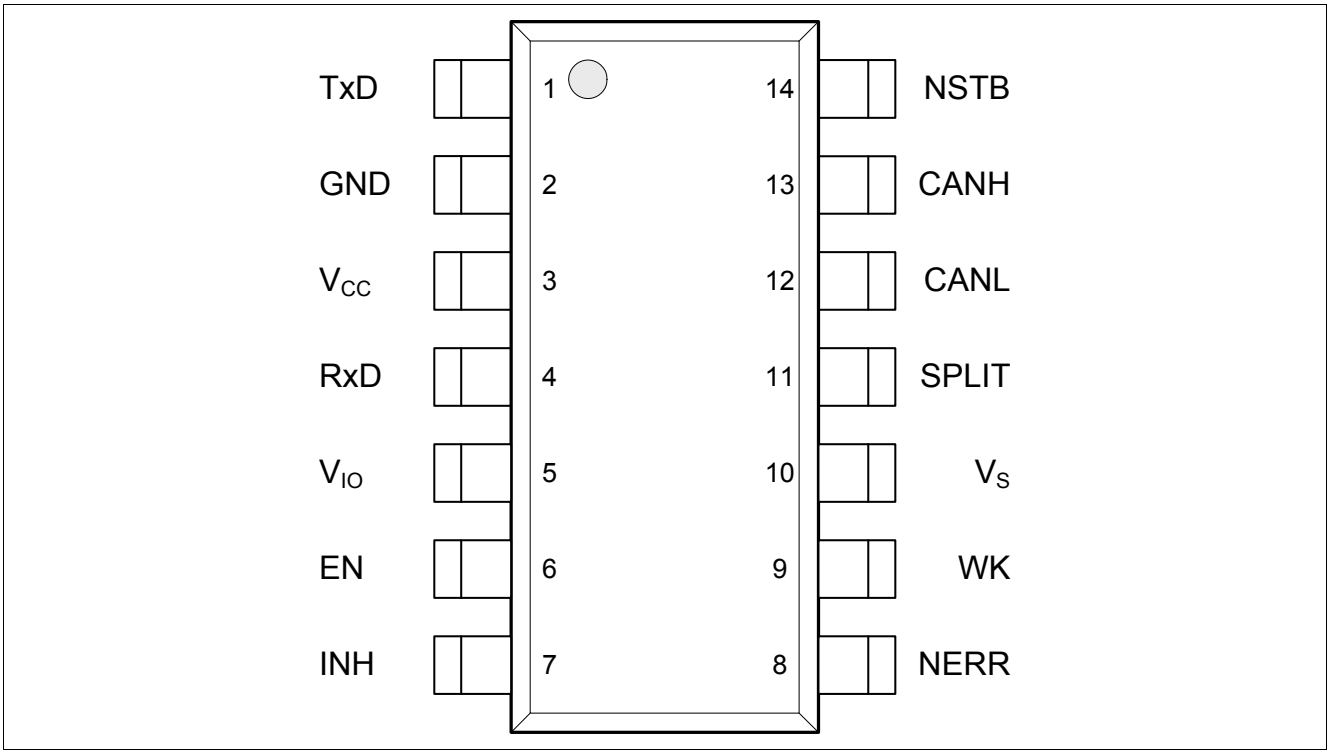


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Table 1 Pin Definitions and Functions

Pin	Symbol	Function
1	TxD	**Transmit Data Input;** integrated pull-up resistor to V_{IO}, “low” for dominant state.
2	GND	**Ground**
3	V_{CC}	**Transceiver Supply Voltage;** 100 nF decoupling capacitor to GND recommend.
4	RxD	**Receive Data Output;** “Low” in dominant state. Output voltage level dependent on the V_{IO} supply
5	V_{IO}	**Logic Supply Voltage;** Digital Supply Voltage for the logic pins TxD, RxD, EN, NERR and NSTB; Usually connected to the supply voltage of the external microcontroller; 100 nF decoupling capacitor to GND recommend.
6	EN	**Mode Control Input;** Integrated pull-down resistor; “High” for Normal Operation mode.

Pin Configuration

Table 1 Pin Definitions and Functions (cont'd)

Pin	Symbol	Function
7	INH	**Inhibit Output;** Open drain output to control external circuitry; High impedance in Sleep mode
8	NERR	**Error Flag Output;** Failure and Wake-Up indication output, active "low" Output voltage level depends on the V_{IO} supply
9	WK	**Wake-Up Input;** Local Wake-Up input; Wake-Up input sensitive to a level change in both directions, "high" to "low" and vice versa.
10	V_S	**Battery Voltage Supply;** 100 nF decoupling capacitor to GND recommend.
11	SPLIT	**Split Termination Output;** Stabilization output to support the recessive voltage level of the CAN bus lines.
12	CANL	**CAN Bus "Low" Level I/O;** "Low" in dominant state
13	CANH	**CAN Bus "High" Level I/O;** "High" in dominant state
14	NSTB	**Stand-By Control input;** Integrated pull-down resistor; "High" for Normal Operation mode.

4 Functional Description

CAN is a serial bus system that connects microcontrollers, sensor and actuators for real-time control applications. The usage of the Control Area Network (abbreviated CAN) within road vehicles is described by the international standard ISO 11898. According to the 7 layer OSI reference model the physical layer of a CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes inside the network. The physical layer specification of a CAN bus system includes all electrical and mechanical specifications of a CAN network. The CAN transceiver is part of the physical layer specification. Several different physical layer standards of CAN networks have been developed over the last years. The TLE6251-2G is a High Speed CAN transceiver with dedicated Wake-Up functions. High Speed CAN Transceivers with Wake-Up functions are defined by the international standard ISO 11898-5.

4.1 High Speed CAN Physical Layer

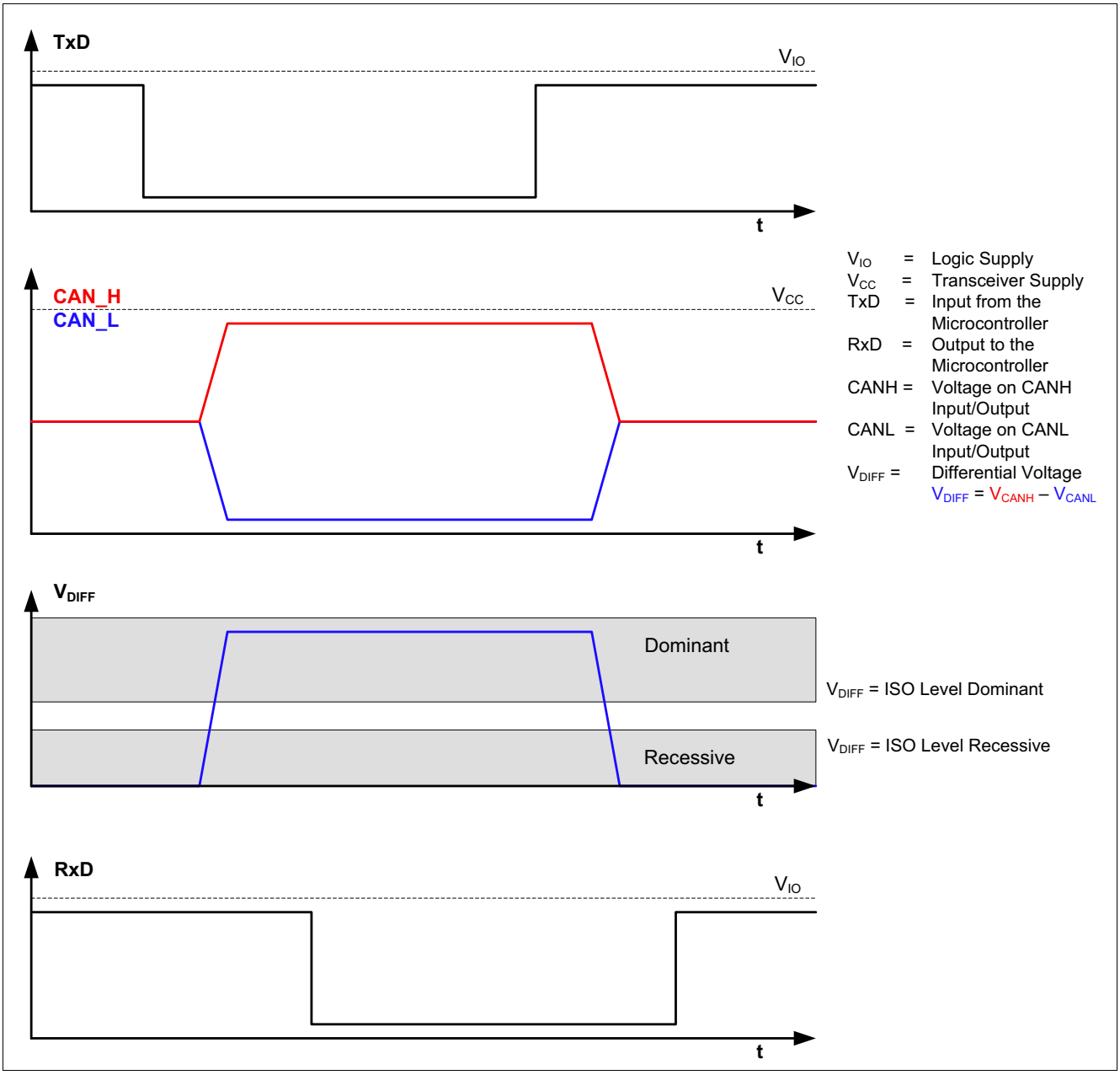


Figure 3 High Speed CAN Bus Signals and Logic Signals

Functional Description

The TLE6251-2G is a High Speed CAN transceiver, operating as an interface between the CAN controller and the physical bus medium. A High Speed CAN network (abbreviated HS CAN) is a two wire differential network which allows data transmission rates up to 1 MBaud. Characteristic for a HS CAN network are the two CAN bus states dominant and recessive (see **Figure 3**).

A HS CAN network is a Carrier Sense Multiple Access network with Collision Detection. This means, every participant of the CAN network is allowed to place its message on the same bus media simultaneously. This can cause data collisions on the bus, which might corrupt the information content of the data stream. In order avoid the loss of any information and to prioritize the messages, it is essential that the dominant bus signal overrules the recessive bus signal.

The input TxD and the output RxD are connected to the microcontroller of the ECU. As shown in **Figure 1**, the HS CAN transceiver TLE6251-2G has a receive unit and a output stage, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time. The HS CAN TLE6251-2G converts the serial data stream available on the transmit data input TxD into a differential output signal on CAN bus. The differential output signal is provided by the pins CANH and CANL. The receiver stage of the TLE6251-2G monitors the data on the CAN bus and converts them to a serial data stream on the RxD pin. A “low” signal on the TxD pin creates a dominant signal on the CAN bus, followed by a “low” signal on the RxD pin (see **Figure 3**). The feature, broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneous is essential to support the bit to bit arbitration on CAN networks.

The voltage levels for a HS CAN on the bus medium are defined by the ISO 11898-2/-5 standards. Whether a data bit is dominant or recessive, depends on the voltage difference between CANH and CANL:

$V_{DIFF} = V_{CANH} - V_{CANL}$

To transmit a dominant signal to the CAN bus the differential signal V_{DIFF} is larger or equal to 1.5 V. To receive a recessive signal from the CAN bus the differential signal V_{DIFF} is smaller or equal to 0.5 V.

The voltage level on the digital input TxD and the digital output RxD is determined by the power supply level at the pin V_{IO}. Depending on voltage level at the V_{IO} pin, the signal levels on the logic pins (EN, NERR, NSTB, TxD and RxD) are compatible to microcontrollers with 5 V or 3.3 V I/O supply. Usually the V_{IO} power supply of the transceiver is connected to same power supply as I/O power supply of the microcontroller.

Partially supplied CAN networks are networks where the participants have a different power supply status. Some nodes are powered up, other nodes are not powered, or some other nodes are in a Low-Power mode, like Sleep mode for example. Regardless on the supply status of the HS CAN node, each participant which is connected to the common bus, shall not disturb the communication on the bus media. The TLE6251-2G is designed to support partially supplied networks. In Power Down condition, the resistors of the Normal Receiver are switched off and the bus input on the pins CANH and CANL is high resistive.

5 Operation Modes

Five different operation modes are available on TLE6251-2G. Each mode with specific characteristics in terms of quiescent current, data transmission or failure diagnostic. For the mode selection the digital input pins EN and NSTB are used. Both digital input pins are event triggered. **Figure 4** illustrates the different mode changes depending on the status of the EN and NSTB pins. A mode change via the mode selections pins EN and NSTB is only possible when the power supplies V_{CC}, V_{IO} and V_S are active.

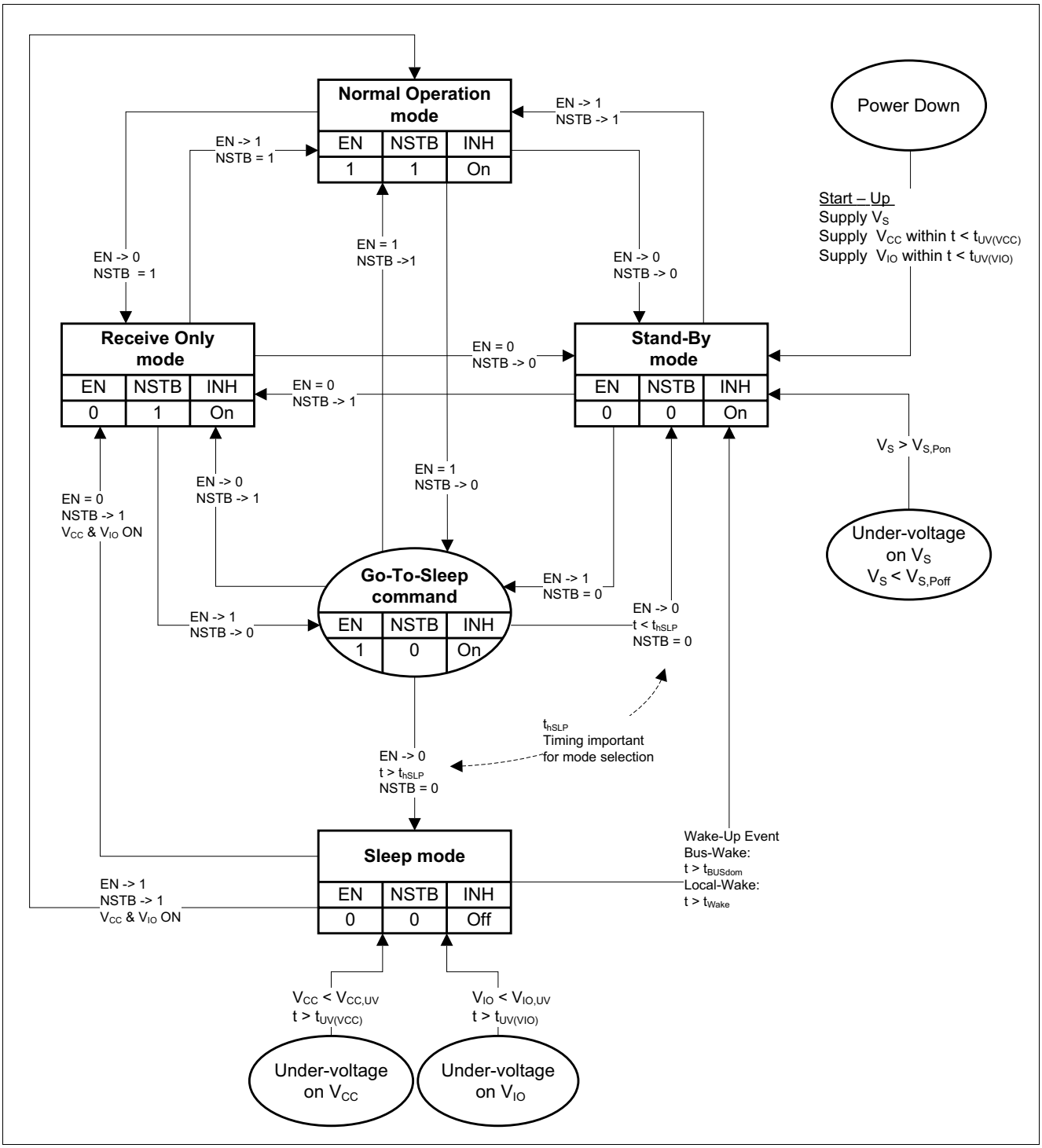


Figure 4 Operation Modes

Operation Modes

In Sleep mode the power supply V_{CC} and the logic power supply V_{IO} are usually turned off. A Wake-Up event, via the CAN bus or the local Wake-Up pin, shifts the device from Sleep mode into Stand-By mode.

The following operation modes are available on the TLE6251-2G:

- Normal Operation mode
- Receive-Only mode
- Stand-By mode
- Sleep mode
- Go-To-Sleep command

Depending on the operation mode, the output driver stage, the receiver stage, the split termination and the bus biasing are active or inactive. **Table 2** shows the different operation modes depending on the logic signal on the pins EN and NSTB with the related status of the INH pin, the SPLIT pin and the bus biasing.

Table 2 Overview Operation Modes

Operation mode	EN	NSTB	INH	Bus Bias	SPLIT
Normal Operation	1	1	V_S	$V_{CC}/2$	$V_{CC}/2$
Receive-Only	0	1	V_S	$V_{CC}/2$	$V_{CC}/2$
Stand-By	0	0	V_S	GND	Floating
Go-To-Sleep	1	0	V_S	GND	Floating
Sleep	0	0	Floating	GND	Floating
Power Down	0	0	Floating	Floating	Floating

5.1 Normal Operation Mode

In Normal Operation mode the HS CAN transceiver TLE6251-2G sends the serial data stream on the TxD pin to the CAN bus while at the same time the data available on the CAN bus is monitored on the RxD output pin. In Normal Operation mode all functions of the TLE6251-2G are active:

- The output stage is active and drives data from the TxD to the CAN bus.
- The normal receiver unit is active and provides the data from the CAN bus to the RxD pin.
- The low power receiver and the bus Wake-Up function is inactive.
- The local Wake-Up pin is disabled.
- The INH pin is connected to V_S.
- The RxD pin is “low” for a dominant bus signal and “high” for a recessive bus signal”
- The SPLIT pin is set to $V_{CC}/2$.
- The bus basing is set to $V_{CC}/2$.
- The failure detection is active and failures are indicated at the NERR pin. (see **Chapter 8**).
- The under-voltage detection on the all 3 power supplies V_{CC}, V_{IO} and V_S is active.

The HS CAN transceiver TLE6251-2G enters Normal Operation mode by setting the mode selection pins EN and NSTB to “high” (see **Table 2** or **Figure 4**).

5.2 Receive-Only Mode

The Receive-Only mode can be used to test the connection of the bus medium. The TLE6251-2G can still receive data from the bus, but the output stage is disabled and therefore no data can be sent to the CAN bus. All other functions are active:

- The output stage is disabled and data which is available on the TxD pin will be blocked and not communicated to the CAN bus.
- The normal receiver unit is active and provides the data which is available on the CAN bus to the RxD pin.
- The INH pin is connected to V_S.
- The RxD pin is “low” for a dominant bus signal and “high” for a recessive bus signal.
- The SPLIT pin is set to $V_{CC}/2$.
- The bus biasing is set to $V_{CC}/2$.
- The low power receiver and the bus Wake-Up function is inactive.
- The local Wake-Up pin WK is disabled.
- The failure diagnostic is active and local failures are indicated at the NERR pin (see **Chapter 8**).
- The under-voltage detection on the all 3 power supplies V_{CC}, V_{IO} and V_S is active.

The HS CAN transceiver TLE6251-2G enters Receive-Only mode by setting the EN pin to “low” and the NSTB to “high” (see **Table 2** or **Figure 4**).

5.3 Stand-By Mode

After the power-up sequence the TLE6251-2G enters automatically into Stand-By mode. Stand-By mode is an idle mode of the TLE6251-2G with optimized power consumption. In Stand-By mode the TLE6251-2G can not send or receive any data. The output driver stage and the normal receiver unit are disabled. Both CAN bus pins, CANH and CANL are connected to GND and the Split termination output is floating. The following functions are available in Stand-By mode:

- The output stage is disabled.
- The normal receiver unit is disabled.
- The low power receiver is active and monitors the CAN bus. In case of a message on the CAN bus the TLE6251-2G sets an internal Wake-Up flag. If the power supplies V_{CC} and V_{IO} are active, the Wake-Up event is indicated by the RxD pin and the NERR pin (see **Chapter 8**). After first power-up or after an undervoltage event on V_S a wake-up is not signaled on RxD and NERR pin.
- The local Wake-Up pin is active and a local Wake-Up event is indicated by the RxD and NERR pin, if the power supplies V_{CC} and V_{IO} are active (see **Chapter 8**).
- The INH output is active and set to V_S.
- Through the internal resistors R_I (see **Figure 1**), the pins CANH and CANL are connected to GND.
- If the power supplies V_{CC} and V_{IO} are active, the RxD pin indicates the Wake-Up events.
- The TxD pin is disabled
- The failure diagnostic is disabled.
- The under-voltage detection on the all 3 power supplies V_{CC}, V_{IO} and V_S is active.
- The TLE6251-2G detects a Power-Up event and indicates it at the NERR pin (see **Chapter 8**).

There are several ways to enter the Stand-By mode (see **Figure 4**):

- After the start-up sequence the device enters per default Stand-By mode. Mode changes are only possible when V_{CC} and V_{IO} are present.
- The device is in Sleep mode and a Wake-Up event occurs.
- The device is in the Go-To-Sleep command and the EN pin goes low before the time $t < t_{hSLP}$ has expired.
- The device is in Normal Operation mode or Receive-Only mode and the EN pin and NSTB pin are set to “low”.

- An under-voltage event occurs on the power supply V_S. In case of an under-voltage event, the TLE6251-2G device always changes to Stand-By mode regardless in which mode the device currently operates.

5.4 Go-To-Sleep Command

The Go-To-Sleep command is a transition mode allowing external circuitry like a microcontroller to prepare the ECU for the Sleep mode. The TLE6251-2G stays in the Go-To-Sleep command for the maximum time t = t_{hSLP}, after exceeding the time t_{hSLP} the device changes into Sleep mode. A mode change into Sleep mode is only possible via the Go-To-Sleep command. During the Go-To-Sleep command the following functions on the TLE6251-2G are available:

- The output driver stage is disabled.
- The normal receiver unit is disabled.
- The low power receiver is active and monitors the CAN bus. In case of a message on the CAN bus the TLE6251-2G sets an internal Wake-Up flag.
- The local Wake-Up pin is active and can detect a local Wake-Up event.
- The INH output is active and set to V_S.
- Through the internal resistors R_I (see **Figure 1**), the pins CANH and CANL are connected to GND.
- The TxD pin is disabled.
- The failure diagnostic is disabled.
- The under-voltage detection on all 3 power supplies V_{CC}, V_{IO} and V_S is active.

Setting the NSTB pin to “low”, while the EN signal remains at “high”, activates the Go-To-Sleep command. The Go-To-Sleep command can be entered from Normal Operation mode, Receive-Only mode and from Stand-By mode.

5.5 Sleep Mode

The Sleep mode is a power save mode. In Sleep mode the current consumption of the TLE6251-2G is reduced to a minimum while the device is still able to Wake-Up by a message on the CAN bus or a local Wake-Up event on the pin WK. Most of the functions of the TLE6251-2G are disabled:

- The output driver stage is disabled.
- The normal receiver unit is disabled.
- The low power receiver is active and monitors the CAN bus. In case of a message on the CAN bus the TLE6251-2G changes from Sleep mode to Stand-By mode and sets an internal Wake-Up flag.
- The local Wake-Up pin is active and in case of a signal change on the WK pin the operation mode changes to Stand-By mode.
- The INH output is floating.
- Through the internal resistors R_I (see **Figure 1**), the pins CANH and CANL are connected to GND.
- If the power supplies V_{CC} and V_{IO} are present, the RxD pin indicates the Wake-Up event.
- The TxD pin is disabled
- The under-voltage detection on the power supply V_S is active and sends the device into Stand-By mode in case of an under-voltage event.

There are only two ways to enter Sleep mode:

- The device can activate the Sleep mode via the mode control pins EN and NSTB.
- An under-voltage event on the power supplies V_{CC} and V_{IO} changes the operation mode to Sleep mode.

In order to enter the Stand-By mode or the Sleep mode, the EN signal needs to be set to “low” a defined time after the NSTB pin was set to “low”. Important for the mode selection is the timing between the falling edge

of the NSTB signal and the EN signal. If the logical signal on the EN pin goes “low” before the transition time t < t_{hSLP} has been reached, the TLE6251-2G enters Stand-By mode and the INH pin remains connected to the V_S supply. In the case the logical signal on the EN pin goes “low” after the transition time t > t_{hSLP}, the TLE6251-2G enters into Sleep mode simultaneous with the expiration of the time window t_{hSLP} and the INH becomes disconnected from the V_S supply and is floating. (see **Figure 5**).

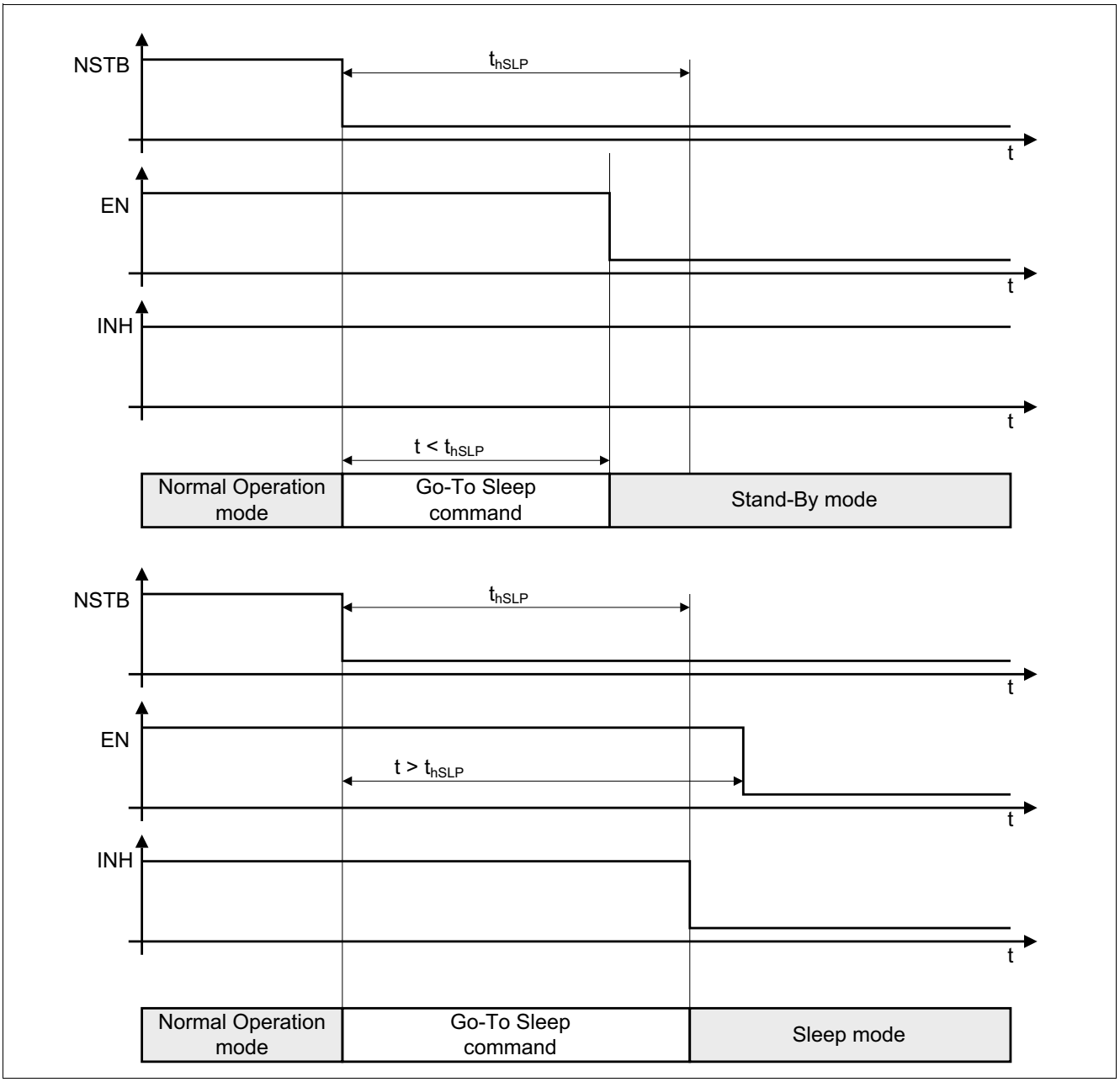


Figure 5 Entering Sleep Mode or Stand-By Mode

The signal on the CAN bus has no impact to mode changes. The operation mode can be changed regardless of the CAN bus being in dominant state or in recessive state.

6 Wake-Up Functions

There are several possibilities for a mode change from Sleep mode to another operation mode.

- Remote Wake-Up via a message on the CAN bus.
- Local Wake-Up via a signal change on the pin WK.
- A status change of the logical signals applied to the mode control pins EN and NSTB.
- An under-voltage detection on the V_S power supply.

In typical applications the power supplies V_{CC} and V_{IO} are turned off in Sleep mode, meaning a mode change can only be caused by an external event, also called Wake-Up. In case the V_{CC} and V_{IO} power supply are available, a mode change can be simple caused by changing the status on the mode control pins EN and NSTB.

6.1 Remote Wake-Up

A remote Wake-Up or also called bus Wake-Up occurs via a CAN bus message and changes the operation mode from Sleep mode to Stand-By mode. A signal change from recessive to dominant, followed by a dominant signal for the time t > t_{Wake} initiates a bus Wake-Up (see **Figure 6**).

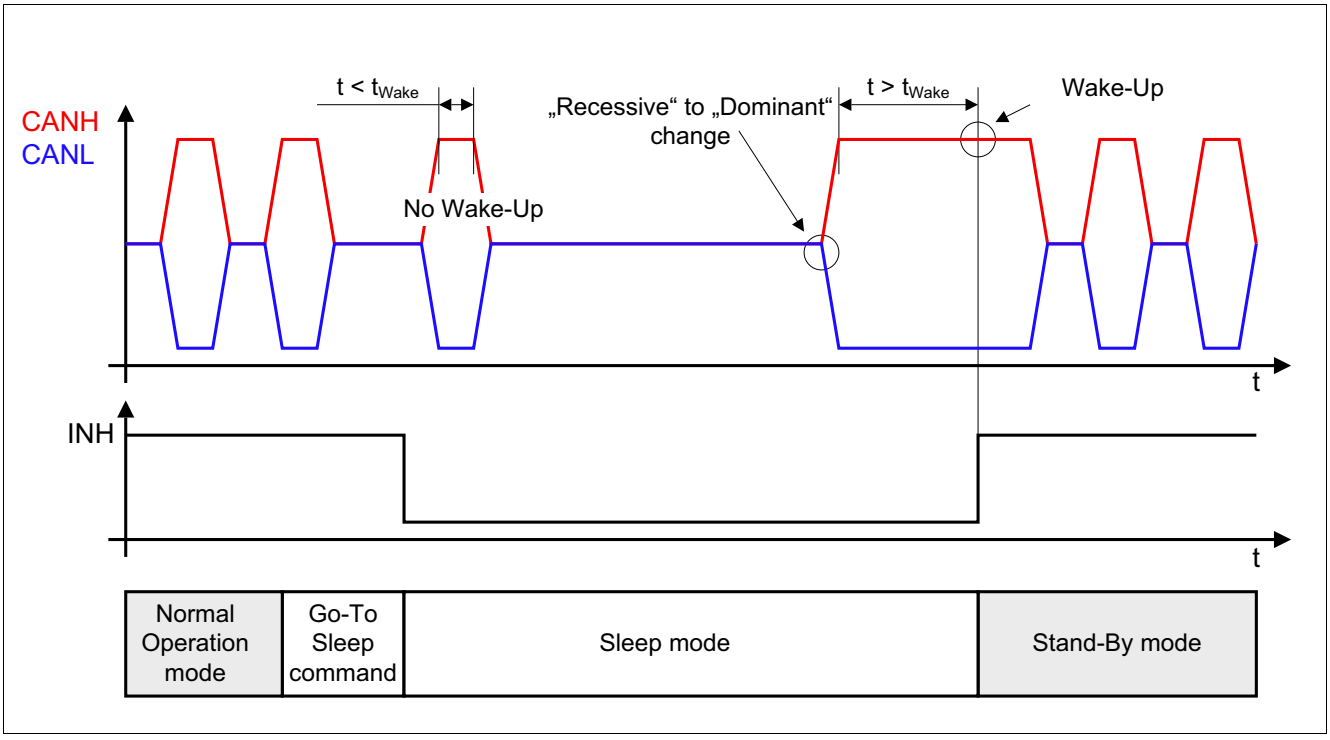


Figure 6 Remote Wake-Up

In case the time of the dominant signal on the CAN bus is shorter than the filtering time t_{Wake}, no bus Wake-Up occurs. The filter time is implemented to protect the HS CAN transceiver TLE6251-2G against unintended bus Wake-Up's, triggered by spikes on the CAN bus. The signal change on the CAN bus from recessive to dominant is mandatory, a permanent dominant signal would not activate any bus Wake-Up.

In Stand-By mode the RxD output pin and the NERR output pin display the CAN bus Wake-Up event by a "low" signal (details see **Chapter 8**). Once the HS CAN Transceiver TLE6251-2G has recognized the Wake-Up event and has changed to Stand-By mode, the INH output pin becomes active and provides the voltage V_S to the external circuitry.

6.2 Local Wake-Up

The TLE6251-2G can be activated from Sleep mode by a signal change on the WK pin, also called local Wake-Up. Designed to withstand voltages up to 40V the WK pin can be directly connected to V_S. The internal logic on the WK pin works bi-sensitive, meaning the Wake-Up logic on the pin WK triggers on a both signal changes, from “high” to “low” and from “low” to “high” (see **Figure 7**).

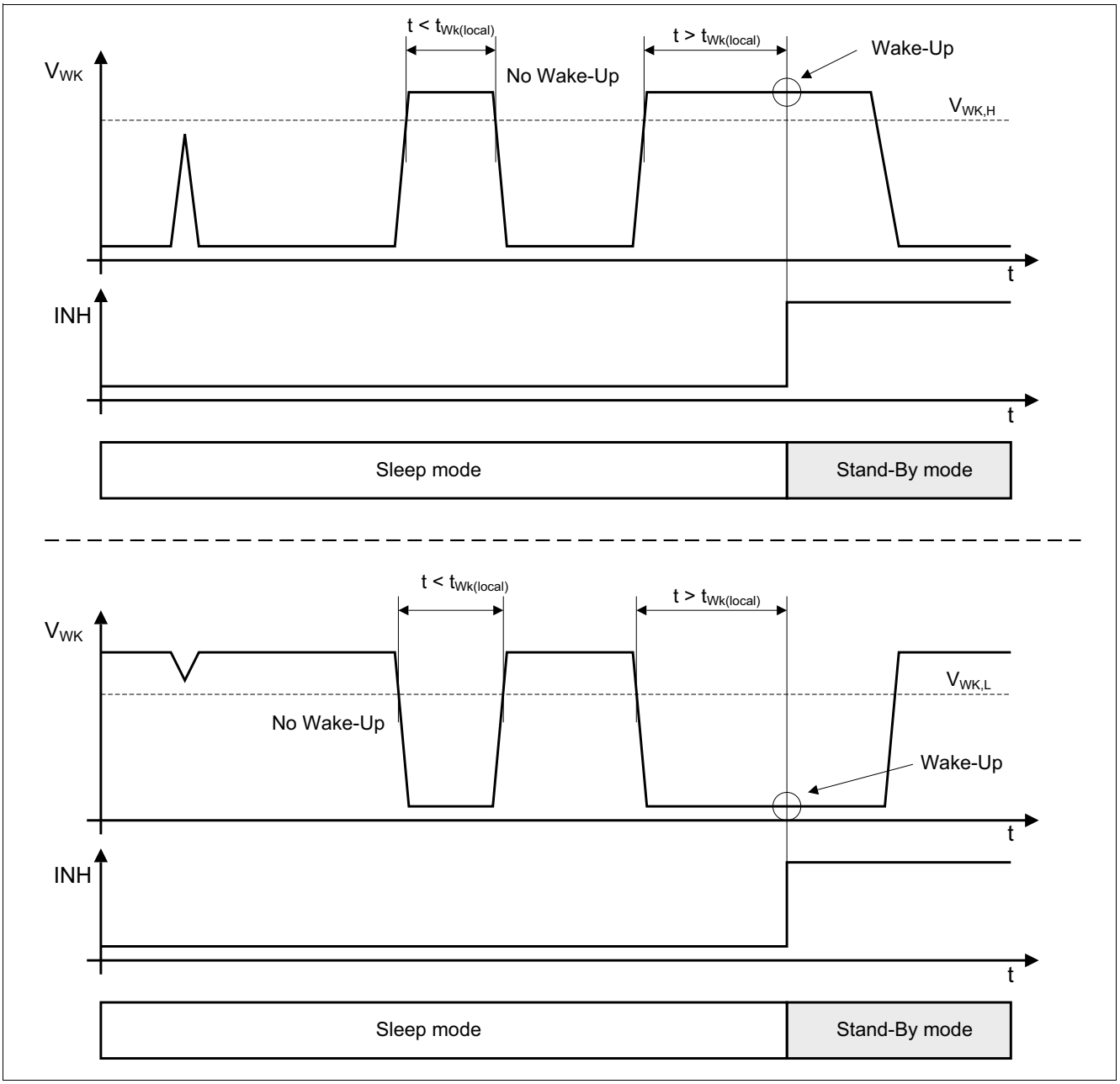


Figure 7 Local Wake - Up

A filter time $t_{WK(local)}$ is implemented to protect the TLE6251-2G against unintended Wake-Up’s, caused by spikes on the pin WK. The threshold values $V_{WK,H}$ and $V_{WK,L}$ depend on the level of the V_S power supply.

In Stand-By mode the RxD output pin and the NERR output pin display the CAN bus Wake-Up event by a logical “low” signal (details see **Chapter 8**). Once the HS CAN Transceiver TLE6251-2G has recognized the Wake-Up event and has changed to Stand-By mode, the INH output pin becomes active and provides the voltage V_S to the external circuitry.

6.3 Mode Change via the EN and NSTB pin

Besides a mode change issued by a Wake-Up event, the operation mode on the TLE6251-2G can be changed by changing the signals on the EN and NSTB pins. Therefore the power supplies V_{CC} and V_{IO} must be active. According to the mode diagram in **Figure 4** the operation mode can be changed directly from Sleep mode to the Receive-Only mode and to the Normal Operation mode. A change from Sleep mode direct to Stand-By mode is only possible via a Wake-Up event. For example by setting the NSTB pin and the EN pin to “high” the TLE6251-2G changes from Sleep mode to Normal Operation mode (see **Figure 8**).

The pins EN and NSTB have a hysteresis between the “low” and the “high” signal in order to avoid any toggling during the operation mode change.

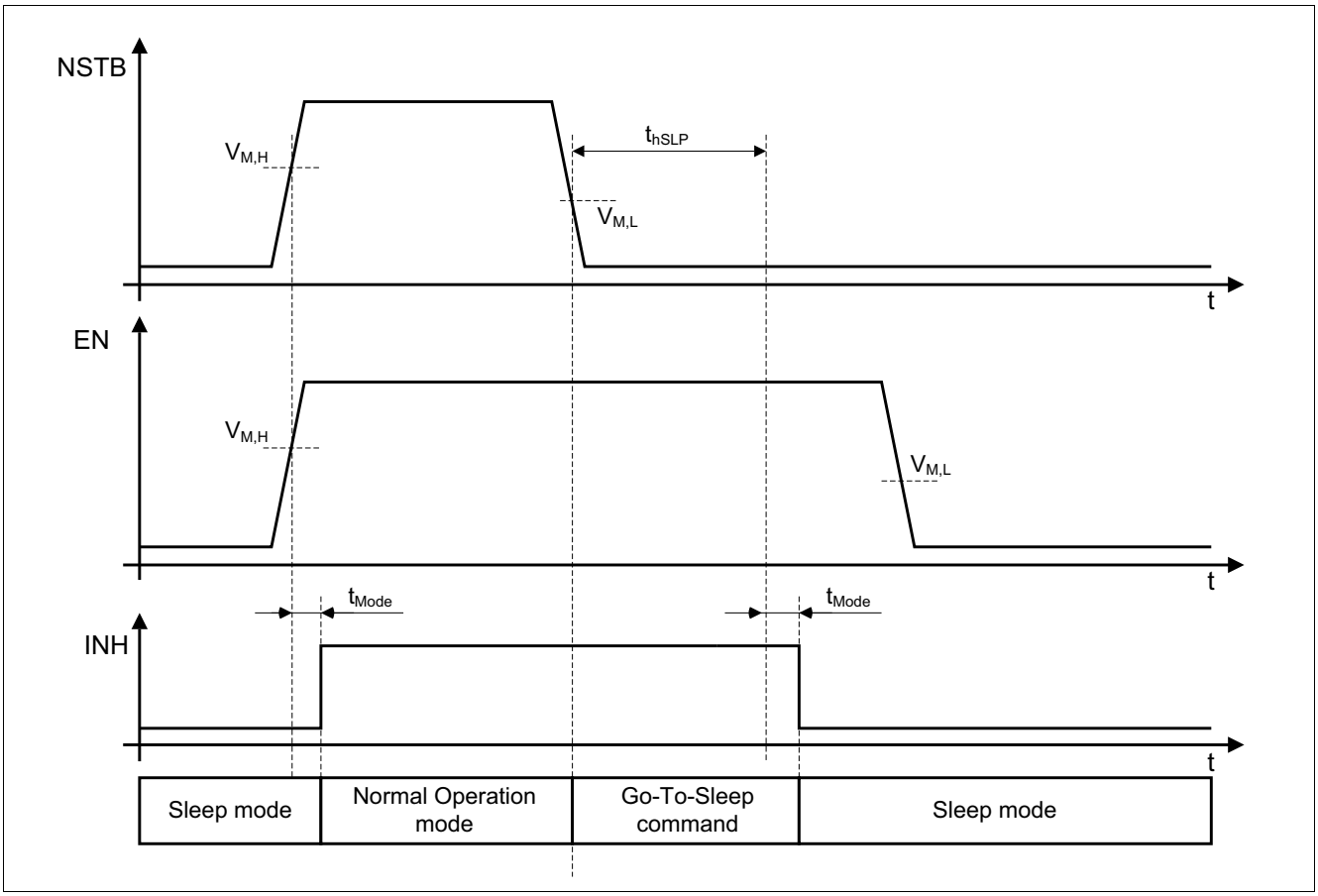


Figure 8 Wake-Up via Mode Change

7 Fail Safe Features

7.1 CAN Bus Failure Detection

The High Speed CAN Transceiver TLE6251-2G is equipped with a bus failure detection unit. In Normal Operation mode the TLE6251-2G can detect the following bus failures:

- CANH shorted to GND
- CANL shorted to GND
- CANH shorted to V_{CC}
- CANL shorted to V_{CC}
- CANH shorted to V_S
- CANL shorted to V_S

The TLE6251-2G can not detect the bus failures:

- CANH open
- CANL open
- CANH short to CANL

The TLE6251-2G detects the bus failures while sending a dominant signal to the CAN bus. After sending four dominant bits to the CAN bus, a “low” on the NERR pins indicates the CAN bus failure. For the failure indication the dominant bits require a minimum pulse width of 4 µs. In case the TLE6251-2G detects an CAN bus failure, the failure is only indicated by the NERR pin, the transceiver doesn’t stop or block the communication, by disabling the output stage for example.

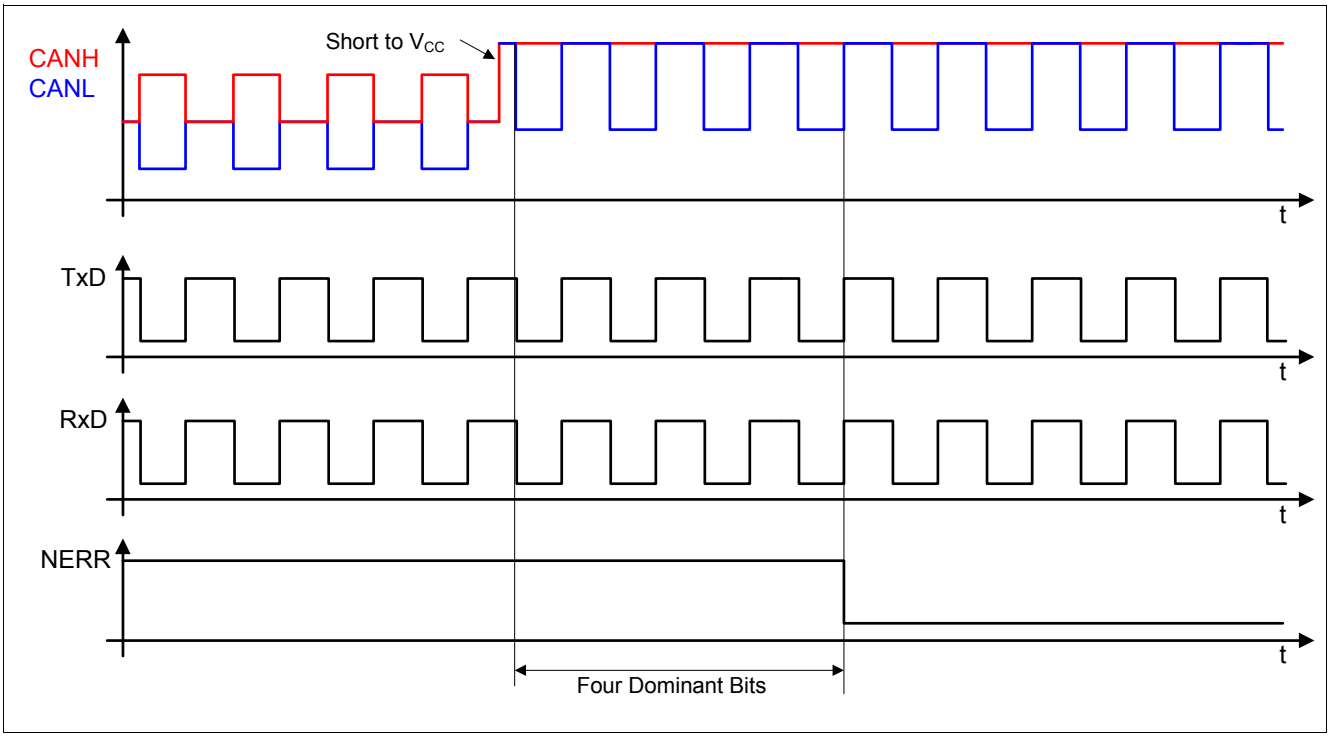


Figure 9 CAN Bus Failure CANH short to V_{CC}

The communication on the CAN bus could still be possible even with a short CANH to V_{CC} or CANH to V_S. Whether the CAN bus communication is possible or not, depends on parameters like the number of

participants inside the CAN network, the network termination, etc. This figure shows a working CAN bus communication as an example and it shall not be considered as a liability that on HS CAN networks the CAN bus communication continues in every CAN bus failure case.

7.2 Local Failures

If a local failure occurs during the operation of the TLE6251-2G, the device sets an internal local failure flag. The local failure flag can be displayed to the microcontroller during the Receive-Only mode and the failures are indicated by a “low” signal on the NERR pin. The following local failures can be detected:

- TxD time-out
- TxD to RxD Short
- RxD permanent Recessive Clamping
- Bus Dominant Clamping
- Over-Temperature Detection

7.2.1 TxD Time-Out Feature

The TxD time-out feature protects the CAN bus against permanent blocking in case the logical signal on the TxD pin is continuously “low”.

In Normal Operation mode, a “low” signal on the TxD input pin for the time $t > t_{TXD}$ enables the TxD time-out feature and the TLE6251-2G disables the output driver stage. In Receive-Only mode the TLE6251-2G indicates the TxD time-out by a “low” signal on the NERR pin (see **Figure 10**). To release the output driver stage after the permanent “low” signal on the TxD input pin disappears, a mode change from Receive-Only mode to Normal Operation mode is required.

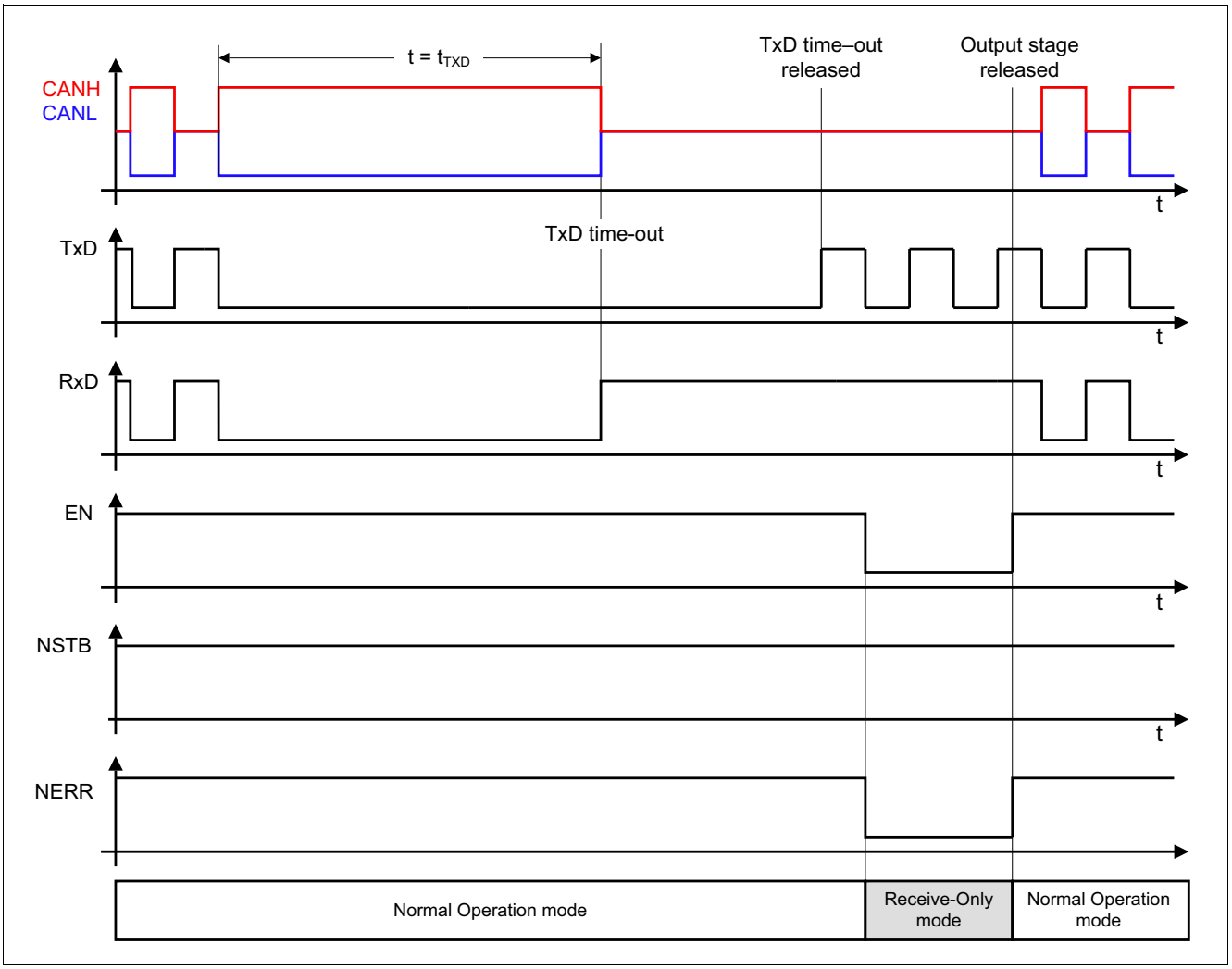


Figure 10 TxD Time-Out Feature

7.2.2 TxD to RxD Short Circuit Feature

A short between the pins TxD and RxD causes permanent blocking of the CAN bus. In the case, that the low side driver capability of the RxD output pin is stronger as the high side driver capability of the external microcontroller output, which is connected to the TxD pin of the TLE6251-2G, the RxD output signal overrides the TxD signal provided by the microcontroller. In this case a continuous dominant signal blocks the CAN bus. The TLE6251-2G detects the short between the TxD and the RxD pin, disables the output driver stage and sets the internal local failure flag. In Receive-Only mode the TLE6251-2G indicates the TxD to RxD short by a “low” signal on the NERR pin. The TLE6251-2G releases the failure flag and the output driver stage by an operation mode change from Receive-Only mode to Normal Operation mode.

7.2.3 RxD Permanent Recessive Clamping

A “High” signal on the RxD pin indicates the external microcontroller, that there is no CAN message on the CAN bus. The microcontroller can transmit a message to the CAN bus only when the bus is recessive. In case the “high” signal on the RxD pin is caused by a failure, like a short from RxD to V_{IO}, the RxD signal doesn’t mirror the signal on the CAN bus. This allows the microcontroller to place a message to the CAN bus at any time and corrupts CAN bus messages on the bus. The TLE6251-2G detects a permanent “high” signal on the RxD pin and set the local error flag. In order to avoid any data collisions on the CAN bus the output driver stage gets disabled. In Receive-Only mode the TLE6251-2G indicates the RxD clamping by a “low” signal on the NERR pin.

The TLE6251-2G releases the failure flag and the output driver stage by an operation mode change or when the RxD clamping failure disappears.

7.2.4 Bus Dominant Clamping

Due to a fail function on one of the CAN bus participants, the CAN bus could be permanent in dominant state. The external microcontroller doesn't transmit any data to the CAN bus as long as the CAN bus remains dominant. Even if the permanent dominant state on the CAN bus is caused by a short from CANH to V_{CC}, or similar, the transceiver can not detect the failure, because the CAN bus failure detection works only when the transceiver is active sending data to the bus. Therefore the TLE6251-2G has a bus dominant clamping detection unit installed. In case the bus signal is dominant for the time $t > t_{Bus,t}$ the TLE6251-2G detects the bus clamping and sets the local failure flag. The output driver stage remains active. In Receive-Only mode the TLE6251-2G indicates the bus dominant clamping by a "low" signal on the NERR pin.

7.2.5 Over-Temperature Detection

The output driver stage is protected against over temperature. Exceeding the shutdown temperature results in deactivation of the output driver stage. To avoid any toggling after the device cools down, the output driver stage is enabled again only after a recessive to dominant signal change on the TxD pin (see **Figure 11**).

An Over-Temperature event only deactivates the output driver stage, the TLE6251-2G doesn't change its operation mode in this failure case. The overtemperature event is indicated by a "low" signal on the NERR pin in Receive-Only mode.

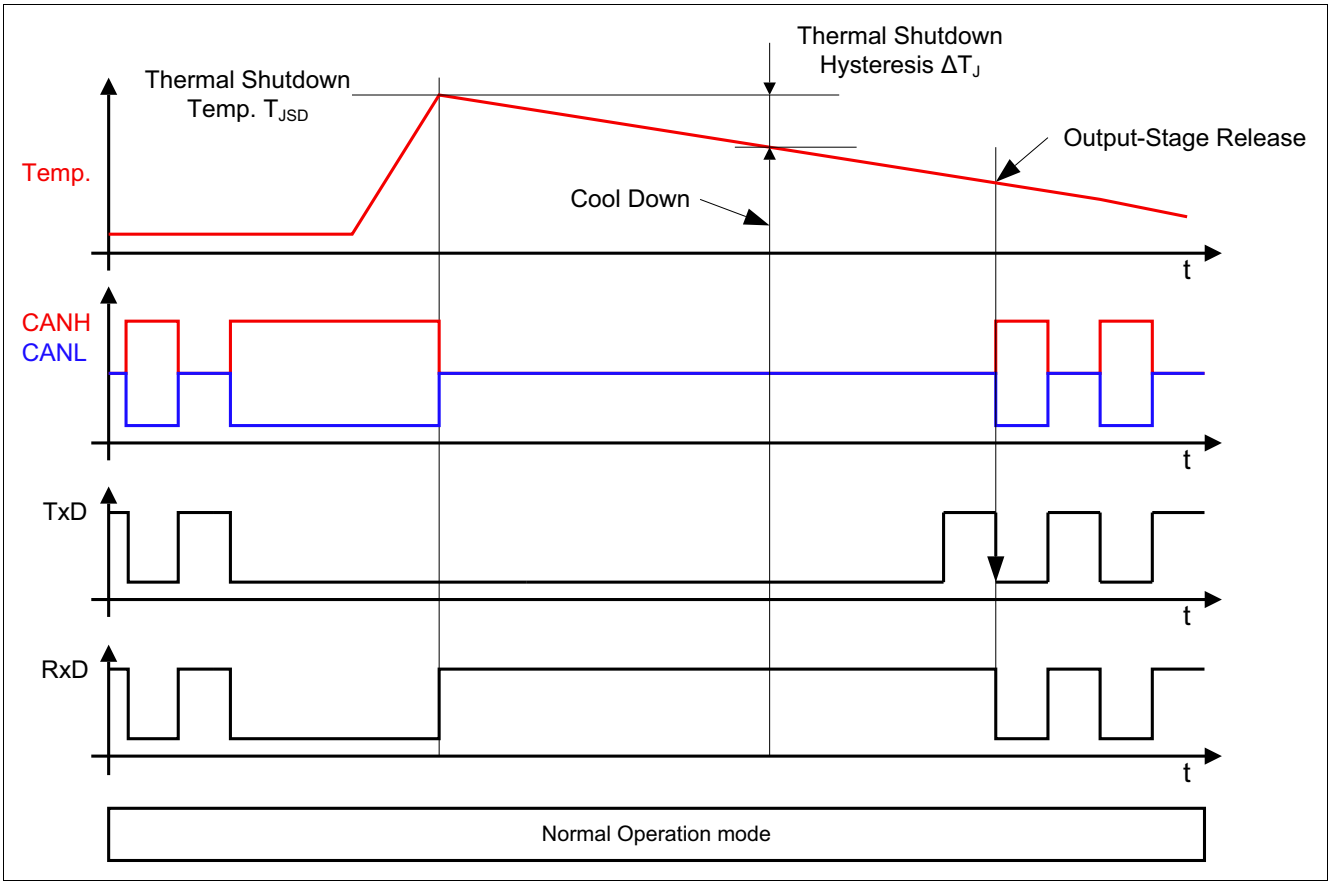


Figure 11 Release of the Transmission after an Over-Temperature event

7.3 Under-Voltage Detection

The TLE6251-2G provides a power supply monitoring on all three power supply pins: V_{CC}, V_{IO} and V_S. In case of an under - voltage event on any of this three power supplies, the TLE6251-2G changes the operation mode and sets an internal failure flag. The internal failure flag is not indicated by the NERR output pin.

7.3.1 Under-Voltage event on V_{CC} and V_{IO}

An under-voltage event on the power supply V_{CC} or the power supply V_{IO} causes the change of the operation mode to Sleep mode, regardless of the operation mode in which the TLE6251-2G might currently operate. The logical signals on the digital input pins EN and NSTB are also disregarded. After the power supplies V_{CC} and V_{IO} are activated again, the operation mode can be changed the usual way. From Sleep mode to Stand-By mode by a Wake-Up event or from Sleep mode direct to Normal Operation mode, Receive-Only mode by the digital input pins EN and NSTB.

The under-voltage monitoring on the power supply V_{CC} and V_{IO} is combined with an internal filter time. Only if the voltage drop on each of these two power supplies is longer present as the time $t_{Drop} > t_{UV(VIO)}$ ($t_{Drop} > t_{UV(VCC)}$) the operation mode change is activated (see **Figure 12**).

Under-voltage events on the power supplies V_{CC} or V_{IO} are not indicated by the NERR pin nor by the RxD pin.

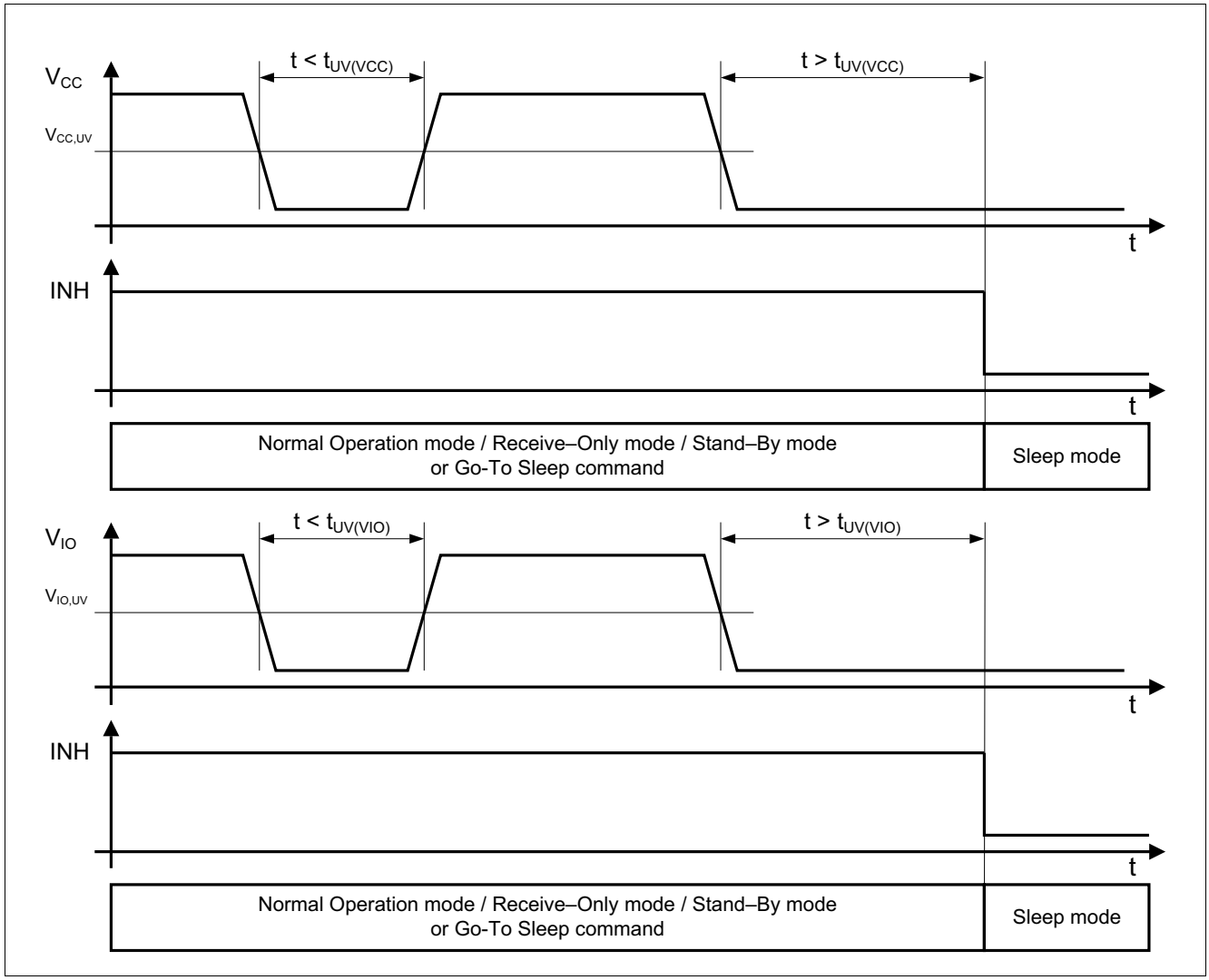


Figure 12 Under-Voltage on V_{IO} or V_{CC}

7.3.2 Under-Voltage Event on V_S

If an under-voltage event is detected at the power supply V_S, the TLE6251-2G immediately enters Stand-By mode, regardless of the operation mode in which the TLE6251-2G operates. After the power supply V_S has been reestablished, the operation mode can be changed by applying a “high” signal to the EN pin or the NSTB pin.

In the case the TLE6251-2G detects an under-voltage event on the V_{CC} or V_{IO} power supply, the TLE6251-2G changes to Sleep mode. If the TLE6251-2G detects in Sleep mode an under-voltage event on the V_S power supply, the device enters Stand-By mode, even when the under-voltage event on the V_{CC} or V_{IO} power supply is still present.

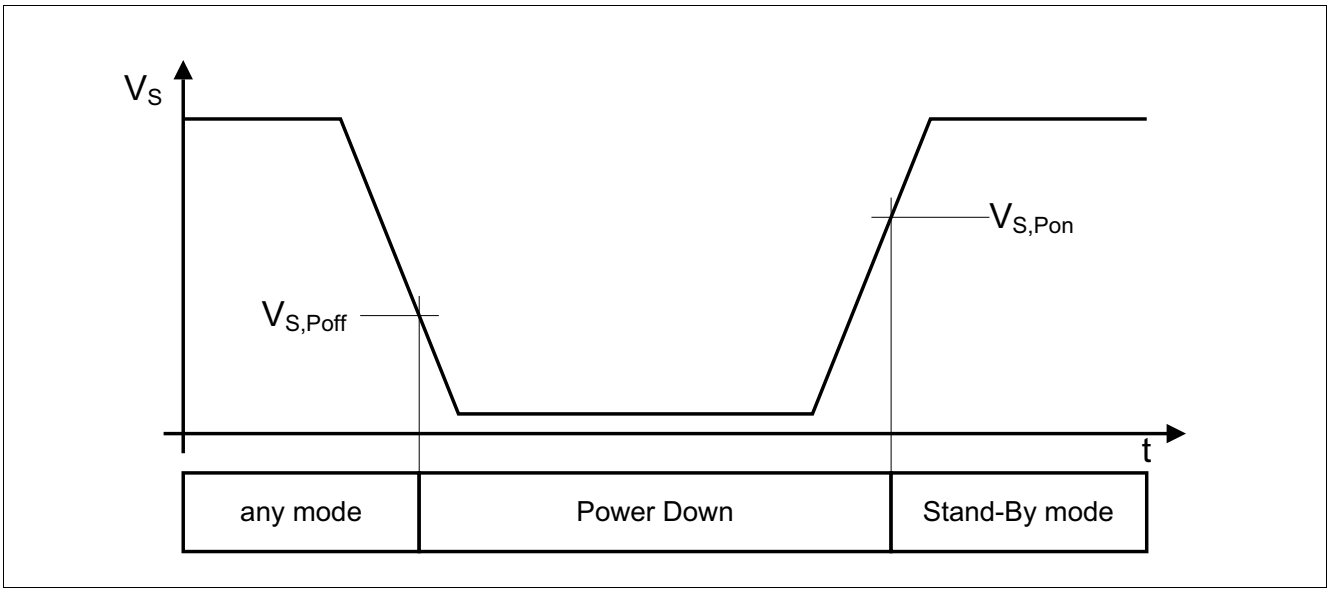


Figure 13 Under-Voltage on V_S

7.4 Voltage Adaptation

The advantage of the adaptive microcontroller logic is the ratio metrical scaling of the I/O levels depending on the input voltage at the V_{IO} pin. Connecting the V_{IO} input to the I/O supply of the microcontroller ensures, that the I/O voltage of the microcontroller fits to the internal logic levels of the TLE6251-2G.

7.5 Split Circuit

The SPLIT output pin is activated during Normal Operation mode and Receive-Only mode and deactivated (SPLIT pin high resistive) during Sleep mode and Stand-By mode. The SPLIT pin is used to stabilize the recessive common mode signal in Normal Operation mode and Receive-Only mode. This is realized with a stabilized voltage of 0.5 x V_{CC} at the SPLIT pin.

8 Diagnosis-Flags at NERR and RxD

Table 3 Truth Table

NSTB	EN	INH	Mode	Event	NERR	RxD	SPLIT
1	1	High	Normal	No CAN bus failure[1)]	1	"low": bus dominant, "high": bus recessive	ON
				CAN bus failure[1)]	0		
				Wake-up via CAN bus/no wake-up request detected	1		
				Wake-up via pin WK[2)]	0		
1	0	High	Receive Only	No V_S fail detected[3)]	1	"low": bus dominant, "high": bus recessive	ON
				V_S fail detected[3)]	0		
				No TxD time-out, Over-Temperature event, RxD recessive clamping or Bus dominant time out detected[4)]	1		
				TxD time-out, Over-Temperature event, RxD recessive clamping or Bus dominant time out detected[4)]	0		
0	0	High	Stand-By	Wake-up request detected[5)6)]	0	0	OFF
				No Wake up request detected[5)]	1	1	
0	0	Floating	Sleep	Wake-up request detected[5)]	0	0	OFF
				No wake-up request detected[5)]	1	1	

1) Only valid after at least four recessive to dominant edges at TxD when entering the Normal Operation mode.
2) Only valid before four recessive to dominant edges at TxD when entering the Normal Operation mode.
3) Power-Up flag only available, when V_{CC} and V_{IO} are active. Power-Up flag will be cleared when entering Normal Operation mode.
4) Valid after a transition from Normal Operation mode.
5) Only valid when V_{CC} and V_{IO} are active.
6) After first power-up or after an undervoltage event on VS, a wake-up is not signaled on the RxD and NERR output pin.

9 General Product Characteristics

9.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings[1)]

All voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	P_9.1.1
Transceiver supply voltage	V_{CC}	-0.3	–	6.0	V	–	P_9.1.2
Logic supply voltage	V_{IO}	-0.3	–	6.0	V	–	P_9.1.3
CANH DC voltage versus GND	V_{CANH}	-40	–	40	V	–	P_9.1.4
CANL DC voltage versus GND	V_{CANL}	-40	–	40	V	–	P_9.1.5
Split DC voltage versus GND	V_{SPLIT}	-40	–	40	V	–	P_9.1.6
Input voltage at WK	V_{WK}	-27	–	40	V	–	P_9.1.7
Input voltage at INH	V_{INH}	-0.3	–	V_S + 0.3	V	–	P_9.1.8
Differential voltage CANH to CANL	$V_{Diff,CAN}$	-40	–	40	V	Max. differential voltage between CAN and CANL	P_9.1.9
Differential voltage SPLIT to CANH and CANL	$V_{Diff,SPLIT}$	-40	–	40	V	Max. differential voltage between SPLIT and CAN	P_9.1.10
Differential voltage WK to SPLIT, CANH and CANL	$V_{Diff,WK}$	-40	–	40	V	Max. differential voltage between WK and SPLIT, CAN	P_9.1.11
Logic voltages at EN, NSTB, NERR, TxD, RxD	V_{Logic}	-0.3	–	V_{IO}	V	0 V < V_{IO} < 6.0 V	P_9.1.12
Currents							
Maximum Output Current INH	$I_{INH(max)}$	-5	–	0	mA	–	P_9.1.13
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_9.1.14
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_9.1.15
ESD Susceptibility							
ESD Resistivity at CANH, CANL, SPLIT and WK versus GND	V_{ESD}	-8	–	8	kV	HBM[2)] (100 pF / 1.5 kΩ)	P_9.1.16
ESD Resistivity all other pins	V_{ESD}	-2	–	2	kV	HBM[2)] (100 pF / 1.5 kΩ)	P_9.1.17

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to AEC-Q100-002D.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

9.2 Functional Range

Table 5 Operating Range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply Voltages							
Supply Voltage Range for Normal Operation	$V_{S(nom)}$	5.5	–	18	V	–	P_9.2.1
Extended Supply Voltage Range for Operation	$V_{S(ext)}$	5.0	–	40	V	Parameter Deviations possible	P_9.2.2
Transceiver Supply Voltage	V_{CC}	4.75	–	5.25	V	–	P_9.2.3
Logic Supply Voltage	V_{IO}	3.0	–	5.25	V	–	P_9.2.4
Thermal Parameters							
Junction temperature	T_J	-40	–	150	°C	1)	P_9.2.5

1) Not subject to production test, specified by design

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

9.3 Thermal Resistance

Table 6 Thermal Characteristics[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal Resistance							
Junction to Soldering Point	R_{thJSP}	–	–	25	K/W	measured to pin 2	P_9.3.1
Junction to Ambient	R_{thJA}	–	130	–	K/W	2)	P_9.3.2
Thermal Shutdown Junction Temperature							
Thermal shutdown temp.	T_{JSD}	150	175	190	°C	–	P_9.3.3
Thermal shutdown hysteresis	ΔT	–	10	–	K	–	P_9.3.4

1) Not subject to production test, specified by design

2) EIA/JESD 52_2, FR4, 80 × 80 × 1.5 mm; 35 µm Cu, 5 µm Sn; 300 mm2

10 Electrical Characteristics

10.1 Functional Device Characteristics

Table 7 Electrical Characteristics

4.75 V < V_{CC} < 5.25 V; 3.0 V < V_{IO} < 5.25 V; 5.5 V < V_S < 18 V; R_L = 60 Ω; normal mode; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption							
Current consumption in Normal Operation mode on V_{CC} and V_{IO}	I_{CC+VIO}	–	6	10	mA	Recessive state; TxD = “high”	P_10.1.1
	I_{CC+VIO}	–	50	80	mA	Dominant state; TxD = “low”	
Current consumption in Receive-Only mode on V_{CC} and V_{IO}	I_{CC+VIO}	–	6	10	mA	–	P_10.1.2
Current consumption in Stand-By mode on V_S	I_{VS}	–	45	70	µA	V_S = WK = 12 V V_{CC} = V_{IO} = 5V	P_10.1.3
Current consumption in Stand-By mode on V_{CC} and V_{IO}	I_{CC+VIO}	–	2.5	10	µA	V_S = V_{WK} = 12 V V_{CC} = V_{IO} = 5V	P_10.1.4
Current consumption in Sleep mode on V_S	I_{VS}	–	20	30	µA	V_S = 12 V, T_j < 85°C, V_{CC} = V_{IO} = 0 V	P_10.1.5
Current consumption in Sleep mode on V_{CC} and V_{IO}	I_{CC+VIO}	–	2.5	10	µA	V_S = 12 V, T_j < 85°C, V_{CC} = $V_{µC}$ = 5V	P_10.1.6
Supply Resets							
V_{CC} under-voltage detection	$V_{CC,UV}$	2	3	4	V	–	P_10.1.7
V_{IO} under-voltage detection	$V_{IO,UV}$	1.5	2.5	2.8	V	–	P_10.1.8
V_S power ON detection level	$V_{S,Pon}$	2	4	5	V	–	P_10.1.9
V_S power OFF detection level	$V_{S,Poff}$	2	3.5	5	V	–	P_10.1.10
Receiver Output RxD							
“High” level output current	$I_{RD,H}$	–	-4	-2	mA	V_{RD} = 0.8 × V_{IO}	P_10.1.11
“Low” level output current	$I_{RD,L}$	2	4	–	mA	V_{RD} = 0.2 × V_{IO}	P_10.1.12

Table 7 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < V_{IO} < 5.25 V; 5.5 V < V_S < 18 V; R_L = 60 Ω; normal mode; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmission Input TxD							
"High" level input range	$V_{TD,H}$	0.7 × V_{IO}	–	V_{IO} + 0.3 V	V	Recessive state	P_10.1.13
"Low" level input range	$V_{TD,L}$	- 0.3	–	0.3 × V_{IO}	V	Dominant state	P_10.1.14
"High" level input current	I_{TD}	-5	0	5	µA	V_{TxD} = V_{IO}	P_10.1.15
TxD pull-up resistance	R_{TD}	10	20	40	kΩ	–	P_10.1.16
Mode Control Inputs EN, NSTB							
"High" level input range	$V_{M,H}$	0.7 × V_{IO}	–	V_{IO} + 0.3 V	V	Recessive state	P_10.1.17
"Low" level input range	$V_{M,L}$	- 0.3	–	0.3 × V_{IO}	V	Dominant state	P_10.1.18
"Low" level input current	I_{MD}	-5	0	5	µA	V_{EN} and V_{NSTB} = 0V	P_10.1.19
Pull-down resistance	R_M	50	100	200	kΩ	–	P_10.1.20
Diagnostic Output NERR							
"High" level output voltage	$V_{NERR,H}$	0.8 × V_{IO}	–	–	V	I_{NERR} = -100 µA	P_10.1.21
"Low" level output voltage	$V_{NERR,L}$	–	–	0.2 × V_{IO}	V	I_{NERR} = 1.25 mA	P_10.1.22
Termination Output SPLIT							
Split output voltage	V_{SPLIT}	0.3 × V_{CC}	0.5 × V_{CC}	0.7 × V_{CC}	V	Normal Operation mode; -500 µA < I_{SPLIT} < 500 µA	P_10.1.23
Split output voltage no load	V_{SPLIT}	0.45 × V_{CC}	0.5 × V_{CC}	0.55 × V_{CC}	V	Normal Operation mode; no load	P_10.1.24
Leakage current	I_{SPLIT}	-5	0	5	µA	Sleep mode V_{CC} = V_{IO} = 0 V	P_10.1.25
Output resistance	R_{SPLIT}	–	600	–	Ω	R_{SPLIT} = (V_{SPLIT}(500 µA) - V_{SPLIT}(-500 µA)) / 1 mA	P_10.1.26

Table 7 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < V_{IO} < 5.25 V; 5.5 V < V_S < 18 V; R_L = 60 Ω; normal mode; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake Input WK							
"High" Level voltage range at WK	$V_{WK,H}$	V_S - 2 V	–	V_S + 3 V	V	V_{EN} = V_{NSTB} = 0 V, rising edge	P_10.1.27
"Low" Level voltage range at WK	$V_{WK,L}$	- 27	–	V_S - 4 V	V	V_{EN} = V_{NSTB} = 0 V, falling edge	P_10.1.28
"High" level input current	I_{WKH}	-10	-5	–	µA	V_{WK} = V_s - 2 V	P_10.1.29
"Low" level current	I_{WKL}	–	5	10	µA	V_{WK} = V_s - 4 V	P_10.1.30
Inhibit Output INH							
"High" level voltage drop $\Delta V_H = V_S - V_{INH}$	ΔV_H	–	0.4	0.8	V	I_{INH} = -1 mA	P_10.1.31
		–	0.8	1.6	–	[1] I_{INH} = -5 mA	
Leakage current	$I_{INH,lk}$	–	–	5	µA	Sleep mode; V_{INH} = 0 V	P_10.1.32
Bus Transmitter							
CANL and CANH recessive output voltage	$V_{CANL/H}$	2.0	–	3.0	V	Normal Operation mode no load	P_10.1.33
CANL and CANH recessive output voltage	$V_{CANL/H}$	-0.1	–	0.1	V	Sleep or Stand-By mode no load	P_10.1.34
CANH to CANL recessive output voltage difference	V_{diff}	-500	–	50	mV	V_{TxD} = V_{IO}; no load	P_10.1.35
CANL dominant output voltage	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V; – 50 Ω < R_L < 65 Ω	P_10.1.36
CANH dominant output voltage	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω	P_10.1.37
CANH, CANL dominant output voltage difference	V_{diff}	1.5	–	3.0	V	V_{TxD} = 0 V; – 50 Ω< R_L < 65 Ω	P_10.1.38
CANL short circuit current	I_{CANLsc}	50	80	200	mA	$V_{CANLshort}$ = 18 V	P_10.1.39
CANH short circuit current	I_{CANHsc}	-200	-80	-50	mA	$V_{CANHshort}$ = 0 V	P_10.1.40
Leakage current	$I_{CANHL,lk}$	-5	0	5	µA	V_S = $V_{µC}$ = V_{CC} = 0 V; 0 V < $V_{CANH,L}$ < 5 V	P_10.1.41

Table 7 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < V_{IO} < 5.25 V; 5.5 V < V_S < 18 V; R_L = 60 Ω; normal mode; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver							
Differential receiver input range - dominant	$V_{diff,rdN}$	0.9	–	5.0	V	Normal Operation mode, In respect to CMR	P_10.1.42
Differential receiver input range - recessive	$V_{diff,drN}$	-1.0	–	0.5	V	Normal Operation mode, In respect to CMR	P_10.1.43
Differential receiver input range - dominant	$V_{diff,rdL}$	1.15	–	5.0	V	Sleep mode, Stand-By mode In respect to CMR	P_10.1.44
Differential receiver input range - recessive	$V_{diff,drL}$	-1.0	–	0.4	V	Sleep mode, Stand-By mode In respect to CMR	P_10.1.45
Common Mode Range	CMR	-12	–	12	V	V_{CC} = 5 V	P_10.1.46
Differential receiver hysteresis	$V_{diff,hys}$	–	100	–	mV	–	P_10.1.47
CANH, CANL input resistance	R_i	10	20	30	kΩ	Recessive state	P_10.1.48
Differential input resistance	R_{diff}	20	40	60	kΩ	Recessive state	P_10.1.49
Dynamic CAN-Transceiver Characteristics							
Propagation delay TxD-to-RxD "low" (recessive to dominant)	$t_{d(L),TR}$	–	150	255	ns	C_L = 100 pF; V_{CC} = V_{IO} = 5 V; C_{RxD} = 15 pF	P_10.1.50
Propagation delay TxD-to-RxD "high" (dominant to recessive)	$t_{d(H),TR}$	–	150	255	ns	C_L = 100 pF; V_{CC} = V_{IO} = 5 V; C_{RxD} = 15 pF	P_10.1.51
Propagation delay TxD"low" to bus dominant	$t_{d(L),T}$	–	50	120	ns	C_L = 100 pF; V_{CC} = V_{IO} = 5 V; C_{RxD} = 15 pF	P_10.1.52
Propagation delay TxD "high" to bus recessive	$t_{d(H),T}$	–	50	120	ns	C_L = 100 pF; V_{CC} = V_{IO} = 5 V; C_{RxD} = 15 pF	P_10.1.53
Propagation delay bus dominant to RxD "low"	$t_{d(L),R}$	–	100	135	ns	C_L = 100 pF; V_{CC} = V_{IO} = 5 V; C_{RxD} = 15 pF	P_10.1.54
Propagation delay bus recessive to RxD "high"	$t_{d(H),R}$	–	100	135	ns	C_L = 100 pF; V_{CC} = V_{IO} = 5 V; C_{RxD} = 15 pF	P_10.1.55
Min. hold time go to sleep command	t_{hSLP}	8	25	50	µs	–	P_10.1.56
Min. wake-up time on pin WK	$t_{WK(local)}$	5	10	20	µs	–	P_10.1.57
Min. dominant time for bus wake-up	t_{Wake}	0.75	3	5	µs	–	P_10.1.58
TxD permanent dominant disable time	t_{TxD}	0.3	0.6	1.0	ms	–	P_10.1.59
Bus permanent time-out	$t_{Bus,t}$	0.3	0.6	1.0	ms	–	P_10.1.60

Table 7 Electrical Characteristics (cont'd)

4.75 V < V_{CC} < 5.25 V; 3.0 V < V_{IO} < 5.25 V; 5.5 V < V_S < 18 V; R_L = 60 Ω; normal mode; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
V_{CC}, $V_{\mu C}$ undervoltage filter time	$t_{UV(VIO)}$ $t_{UV(VCC)}$	200	320	480	ms	–	P_10.1.61
Time for mode change	t_{Mode}	–	20	–	µs	1)	P_10.1.62

1) Not subject to production test, specified by design.

10.2 Diagrams

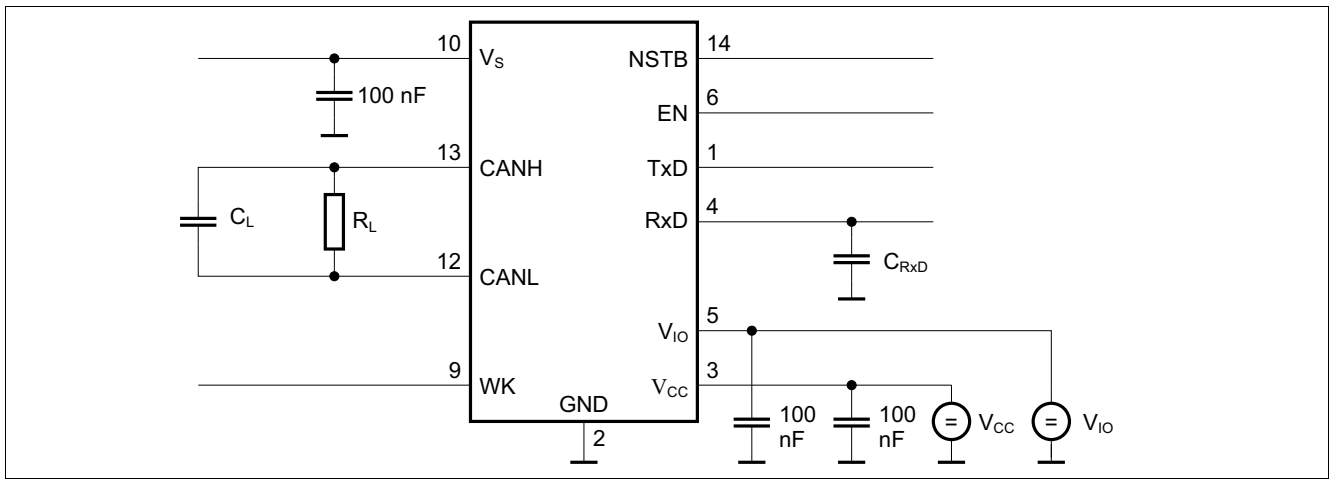


Figure 14 Test Circuit for Dynamic Characteristics

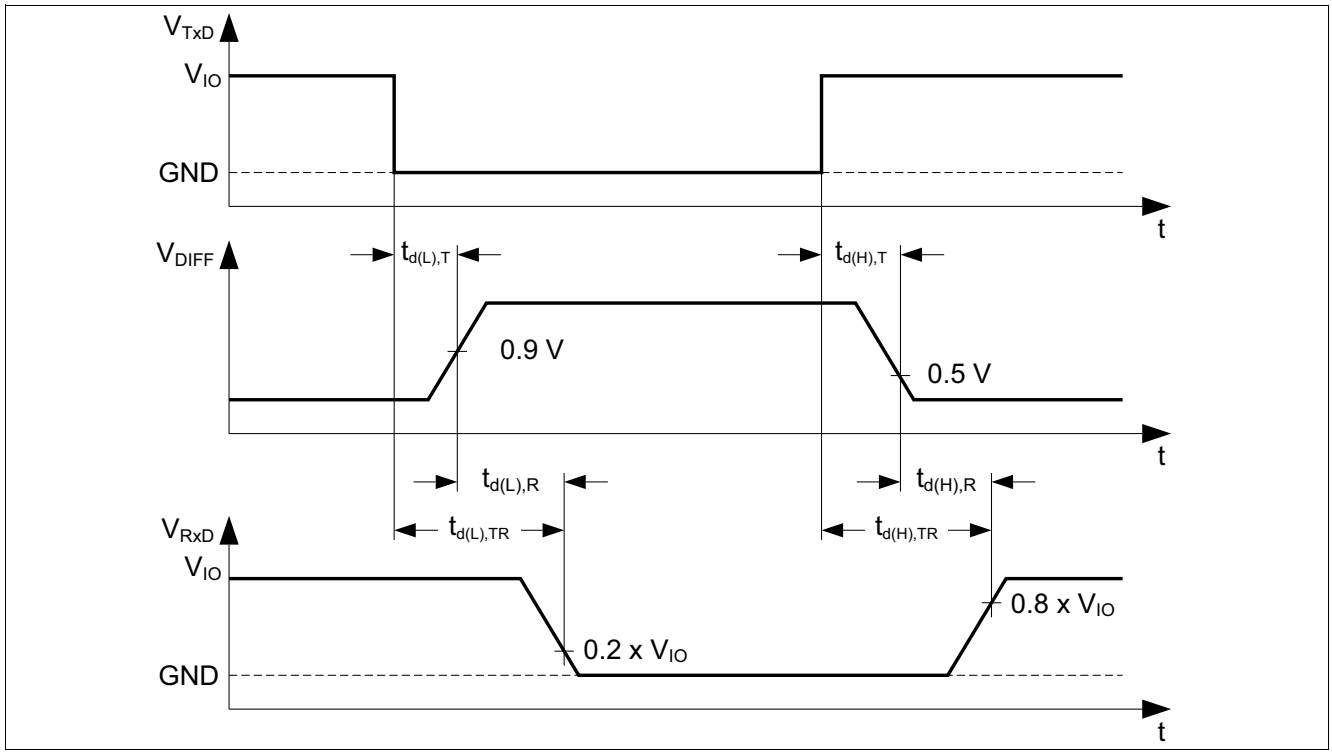


Figure 15 Timing Diagrams for Dynamic Characteristics

11 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

11.1 Application Example

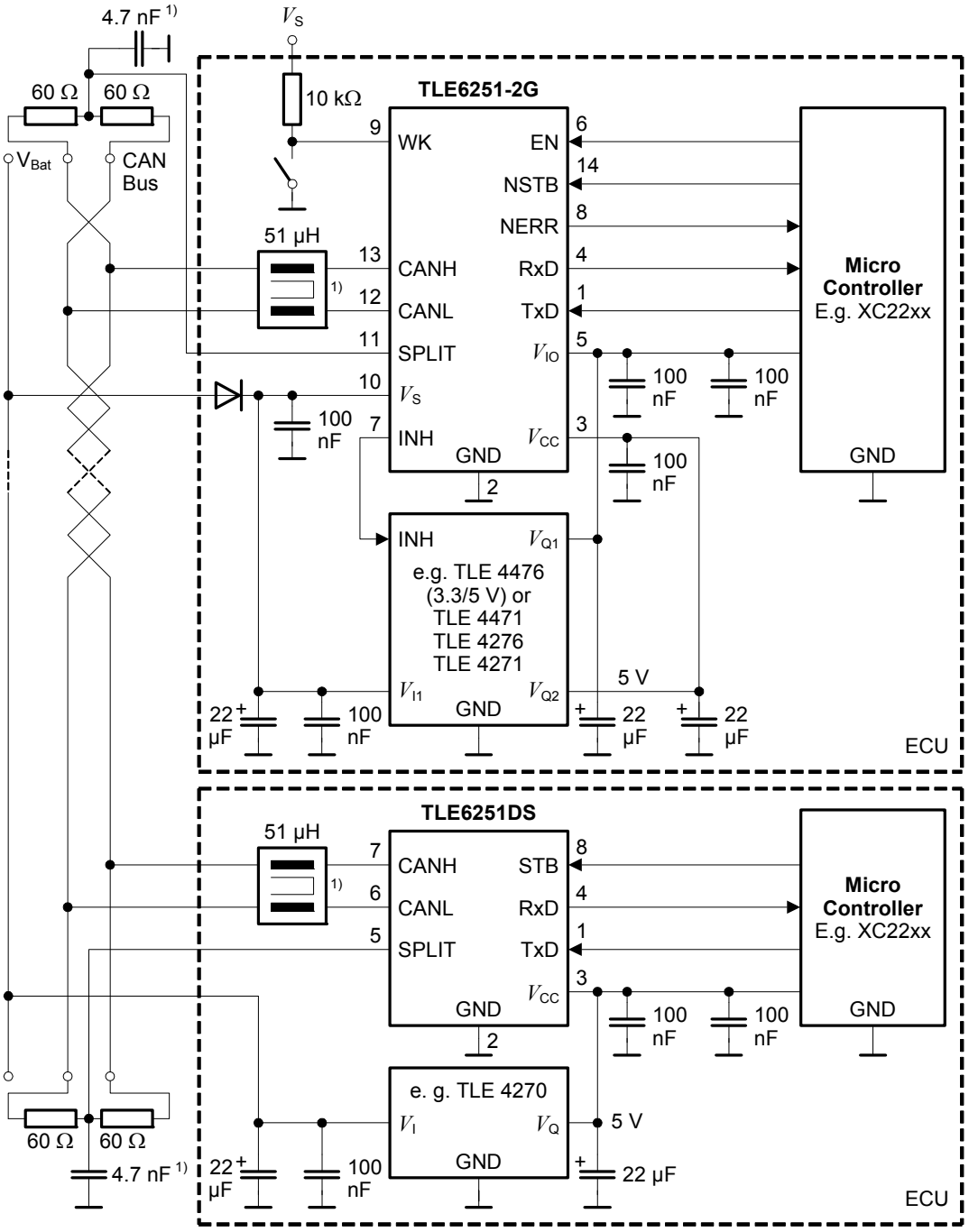


Figure 16 Application Circuit Example

11.2 ESD Robustness according to IEC61000-4-2

Test for ESD robustness according to IEC61000-4-2 “Gun test” (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 8 ESD Robustness according to IEC61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin V_S, CANH, CANL and WK versus GND	≥ 9	kV	[1)]Positive pulse
Electrostatic discharge voltage at pin V_S, CANH, CANL and WK versus GND	≤ -9	kV	[1)]Negative pulse

1) ESD susceptibility “ESD GUN” according to “Gift ICT Evaluation of CAN Transceiver “Section 4.3. (IEC 61000-4-2: 2001-12) -Tested by external test house (IBEE Zwickau, EMC Testreport Nr. 07a-04-09 referenced to the TLE6251-2G).

11.3 Voltage Drop over the INH Output

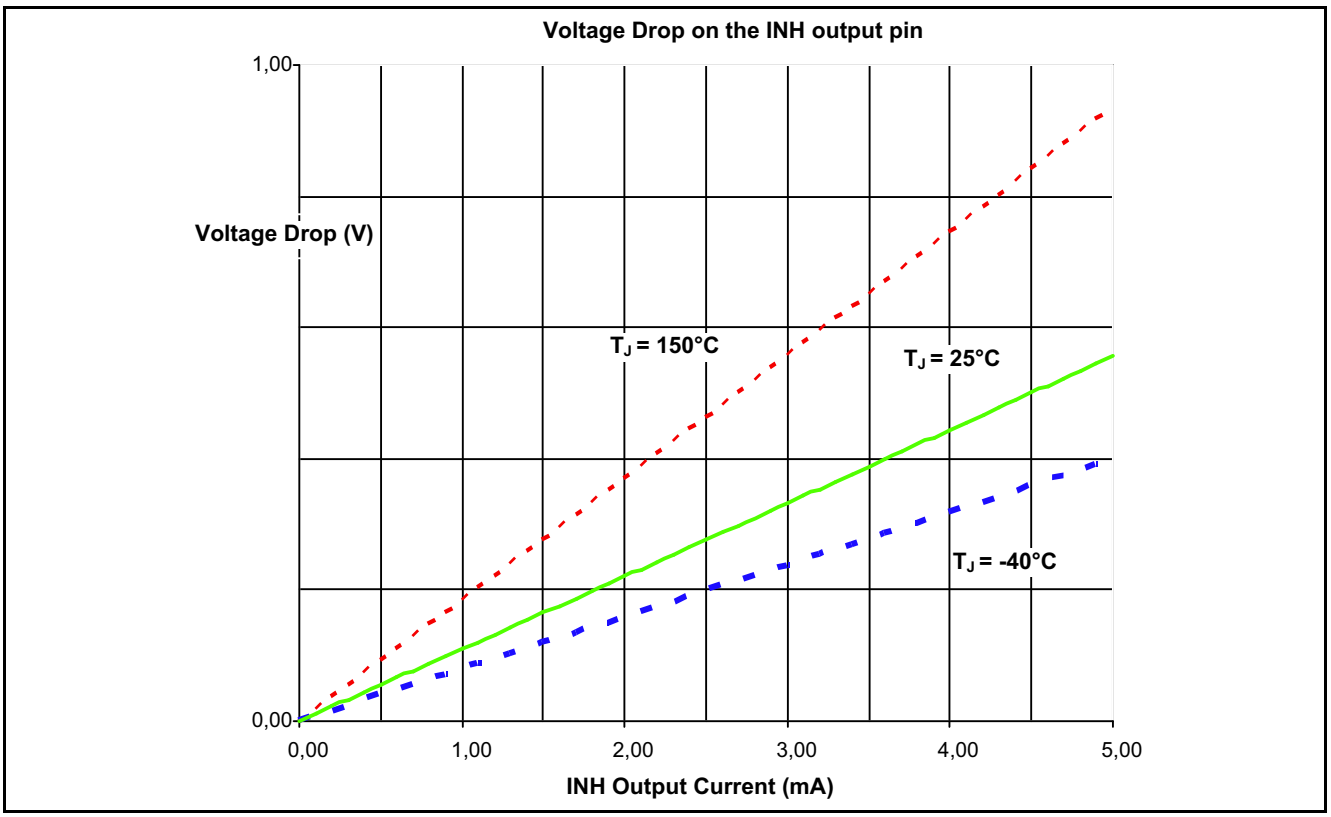


Figure 17 INH output voltage drop versus output current (typical values only!)

11.4 Mode Change to Sleep mode

Mode changes are applied either by a host command, an Wake-Up event or by an under-voltage event. To trigger a mode change by a host command or in other words by a signal change on the digital input pins EN and NSTB all power supplies, V_S V_{IO} and V_{CC} need to be available.TLE6251-2G.

By setting the EN pin to “high” and the NSTB pin to “low”, the TLE6251-2G enters the Go-To-Sleep command and after the time t = t_{hSLP} expires, the TLE6251-2G enters into the Sleep mode (see **Chapter 5.5**). For any mode change, also for a mode change to Sleep mode the TLE6251-2G disregards the signal on the CAN bus.

Therefore the TLE6251-2G can enter Sleep mode and remain in Sleep mode even when there is a short circuit on the CAN bus, for example CANH shorted to V_S or V_{CC}.

dn order to recognize a remote Wake-Up, the TLE6251-2G requires a signal change from recessive to dominant before the Wake-Up filter time starts (see **Figure 6** and **Figure 18**).

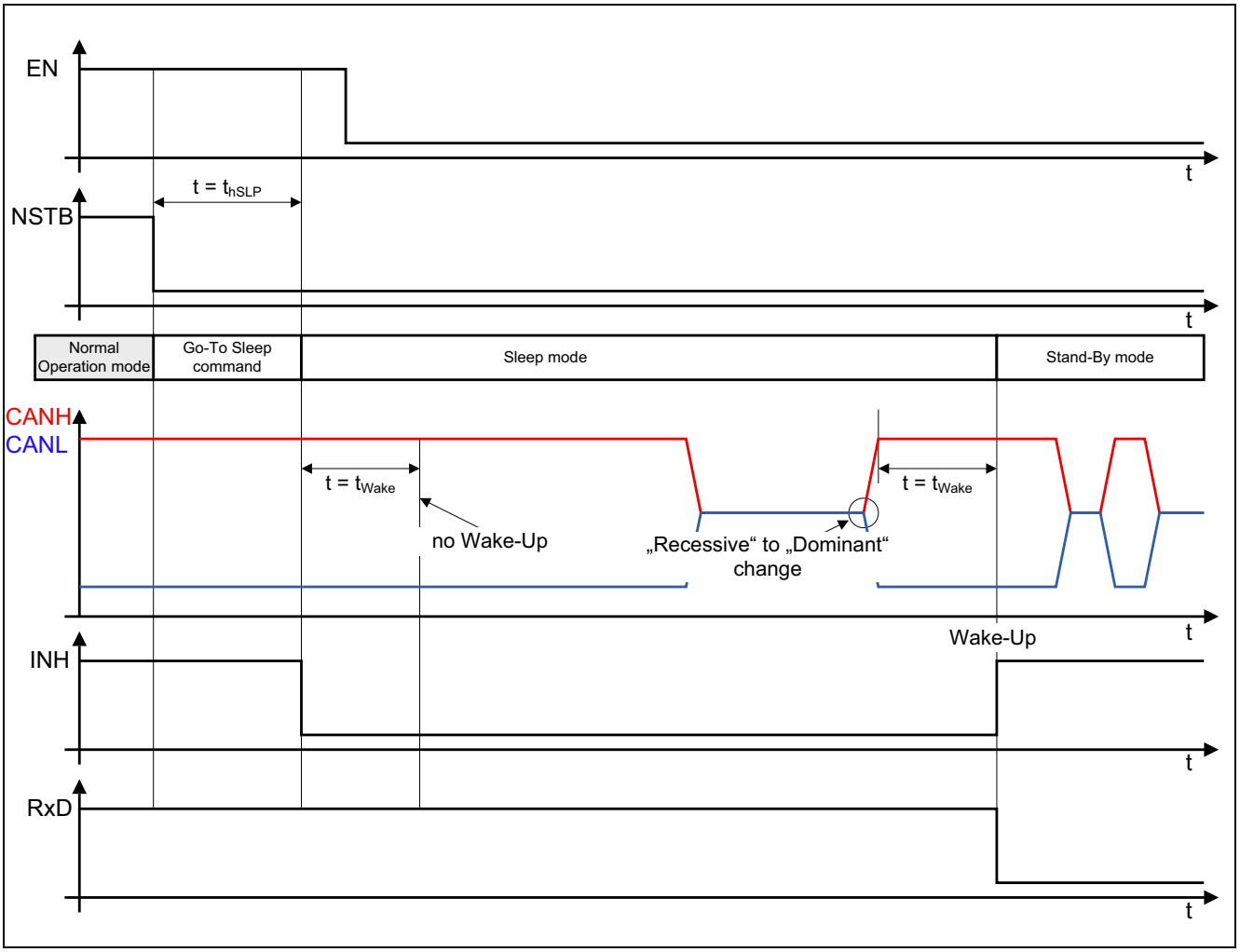
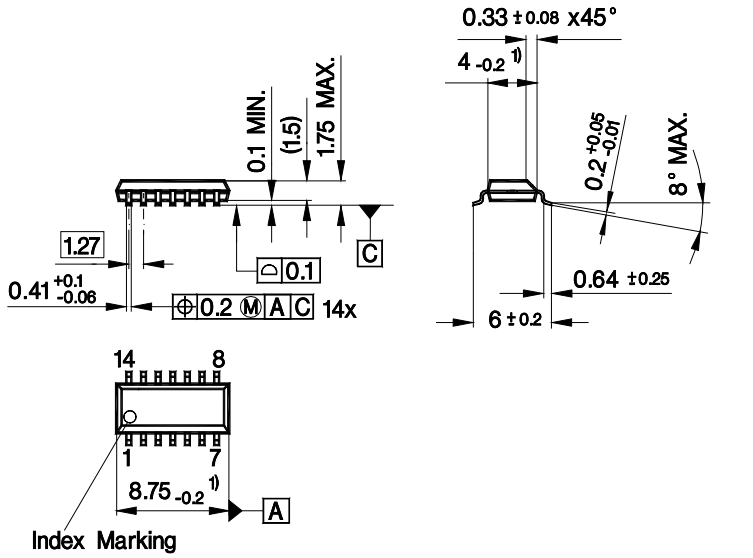


Figure 18 Mode change to Sleep while the CANH bus is dominant

11.5 Further Application Information

- Please contact us for information regarding the pin FMEA.
- Existing Application Note
- For further information you may contact **http://www.infineon.com/transceiver**

12 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side

Figure 19 PG-DSO-14 (Plastic Dual Small Outline PG-DSO-14)

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

13 Revision History

Table 9 Revision History

Revision	Date	Changes
1.22	2017-04-11	Update Data Sheet Rev.1.22 based on Data Sheet Rev. 1.21: • Editorial changes
1.21	2017-03-23	Update Data Sheet Rev.1.21 based on Data Sheet Rev. 1.2: • Typo corrected in Pin Assignment see **Figure 2** from N.C. to SPLIT.
1.2	2016-07-25	Update Data Sheet Rev.1.2 based on Data Sheet Rev. 1.1: • Data Sheet updated to new style template. • Added description for power-up behavior in Stand-by Mode in **Chapter 5.3**: “After first power-up or after an undervoltage event on V_S a wake-up is not signaled on RxD and NERR pin”. • Added footnote in **Table 3**: “After first power-up or after an undervoltage event on V_S a wake-up is not signaled on RxD and NERR pin”.
1.1	2011-05-23	Updated Data Sheet Rev. 1.0 • Cover page, new Infineon logo. • All pages: Spelling, grammar and format failure corrected. • Page 7, Figure 3: Updated. • Page 9, Chapter 5: Updated description. • Page 9, Figure 4: Updated. • Page 11, Chapter 5.3: Timing Reference $t_{h(min)}$ changed to t_{hSLP}. • Page 12, Chapter 5.4: Timing Reference $t_{h(min)}$ changed to t_{hSLP}. • Page 12, Chapter 5.4: Timing Reference $t_{h(min)}$ changed to t_{hSLP}. • Page 13, Chapter 5.6: Added head line. Timing Reference $t_{h(min)}$ changed to t_{hSLP}. • Page 13, Figure 5: Updated. • Page 14, Figure 6: Updated. • Page 15, Figure 7: Updated. • Page 16, Chapter 6.3: Text updated, from Sleep mode no mode change to the Go-To-Sleep command possible.

Revision History

Table 9 Revision History (cont'd)

Revision	Date	Changes
1.1		• Page 16, Figure 8: Updated. • Page 18, Chapter 7.2.1: Updated description. • Page 18, Figure 10: Updated. • Page 20, Figure 11: Updated. • Page 20, Chapter 7.3.1: Updated description. • Page 21, Figure 12: Updated. • Page 22, Figure 13: Updated. • Page 25, table 5, pos. 9.2.1 Updated supply range, 5.5 V to 18 V • Page 25, table 5, pos. 9.2.2 Updated extended supply range, 5.0 V to 40 V • Page 26ff, table 7, headline: Updated V_S range 5.5 V to 18 V. • Page 30, Figure 15: Updated. • Page 34, Chapter 11.4: Added.
1.0	2009-05-07	Initial Data Sheet Rev. 1.0

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