RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 50 W RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1995 MHz.

1800 MHz

- Typical single-carrier W-CDMA performance: V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 50 W Avg., input signal PAR = 9.9 dB @ 0.01% probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.9	30.1	7.7	–35.8	–17
1840 MHz	19.3	30.0	7.6	–36.5	–19
1880 MHz	19.2	30.3	7.5	–36.8	–9

1900 MHz

- Typical single-carrier W-CDMA performance: V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 50 W Avg., input signal PAR = 9.9 dB @ 0.01% probability on CCDF.

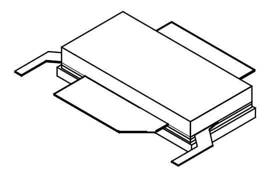
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1930 MHz	19.1	29.2	7.6	–35.1	–23
1960 MHz	19.4	29.9	7.6	–36.0	–15
1995 MHz	19.6	31.0	7.4	–35.7	–10

Features

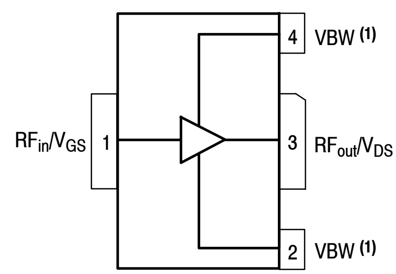
- Greater negative gate-source voltage range for improved Class C operation
- Designed for digital predistortion error correction systems
- Optimized for Doherty applications

A2T18S260-12SR3

1805–1995 MHz, 50 W AVG., 28 V AIRFAST RF POWER LDMOS TRANSISTOR



NI-780S-2L2L



(Top View)

Figure 1. Pin Connections

1. Device cannot operate with V_{DD} current supplied through pin 2 and pin 4.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 89°C, 50 W CW, 28 Vdc, I_{DQ} = 1400 mA, 1840 MHz	$R_{\theta JC}$	0.36	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 270 μAdc)	$V_{GS(th)}$	1.4	1.8	2.2	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1400 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.5	2.9	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 2.7 Adc)	$V_{DS(on)}$	0.05	0.15	0.25	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.nxp.com/RF/calculators.
3. Refer to AN1955*, Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.nxp.com/RF and search for AN1955.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests [1] (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 50 W Avg., f = 1805 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.6	18.9	20.6	dB
Drain Efficiency	η_D	27.5	30.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	7.3	7.7	—	dB
Adjacent Channel Power Ratio	ACPR	—	–35.8	–32	dBc
Input Return Loss	IRL	—	–17	–8	dB
Load Mismatch (In NXP Test Fixture, 50 ohm system) I_{DQ} = 1400 mA, f = 1840 MHz, 12 μsec(on), 10% Duty Cycle					
VSWR 10:1 at 32 Vdc, 416 W Pulsed CW Output Power (3 dB Input Overdrive from 250 W Pulsed CW Rated Power)	No Device Degradation				
Typical Performance (In NXP Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 1805–1880 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	257	—	W
P_{out} @ 3 dB Compression Point [2]	P3dB	—	323	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1805-1880 MHz bandwidth)	Φ	—	–17.4	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	85	—	MHz
Gain Flatness in 75 MHz Bandwidth @ P_{out} = 50 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.011	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.008	—	dB/°C

Table 5. Ordering Information

Device	Tape and Reel Information	Package
A2T18S260-12SR3	R3 Suffix = 250 Units, 44 mm Tape Width, 13-inch Reel	NI-780S-2L2L

1. Part internally matched both on input and output.
2. P3dB = P_{avg} + 7.0 dB where P_{avg} is the average output power measured using an unclipped W-CDMA single-carrier input signal where output PAR is compressed to 7.0 dB @ 0.01% probability on CCDF.

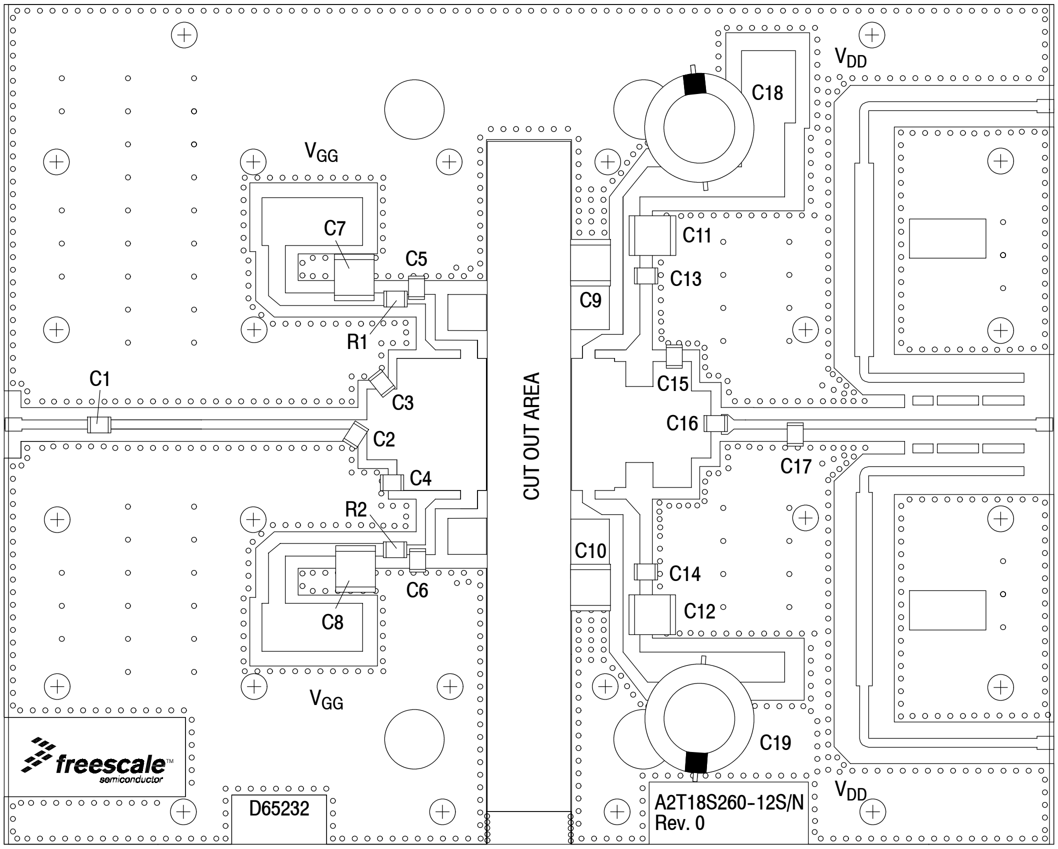


Figure 2. A2T18S260-12SR3 Test Circuit Component Layout

Table 6. A2T18S260-12SR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	5.1 pF Chip Capacitor	ATC600F5R1BT250T	ATC
C2, C3	1.1 pF Chip Capacitors	ATC600F1R1BT250T	ATC
C4	0.7 pF Chip Capacitor	ATC600F0R7BT250T	ATC
C5, C6, C13, C14, C16	15 pF Chip Capacitors	ATC600F150FT250T	ATC
C7, C8, C9, C10, C11, C12	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C15	0.5 pF Chip Capacitor	ATC600F0R5BT250T	ATC
C17	0.2 pF Chip Capacitor	ATC600F0R2BT250T	ATC
C18, C19	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	3.9 Ω, 1/4 W Chip Resistors	CRCW12063R90FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D65232	MTL

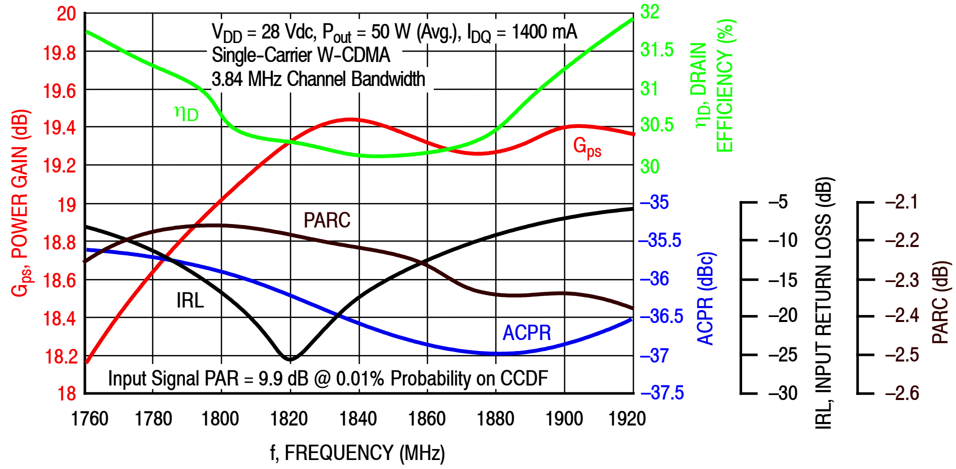


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 50 Watts Avg.

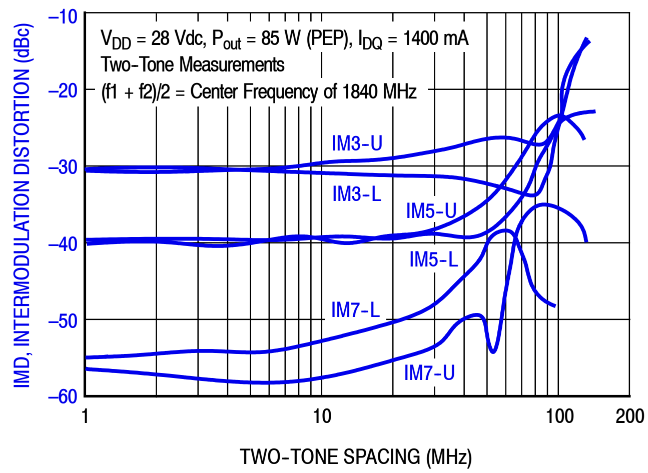


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

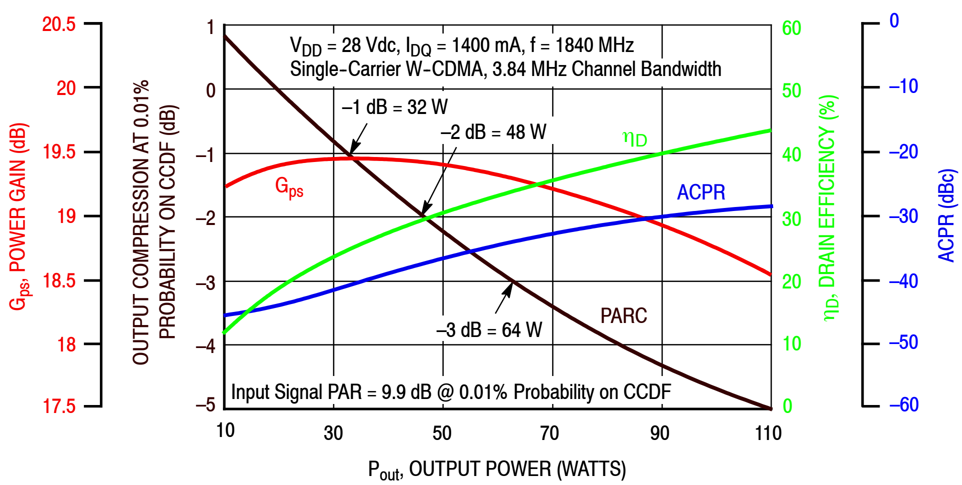


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1805–1880 MHz

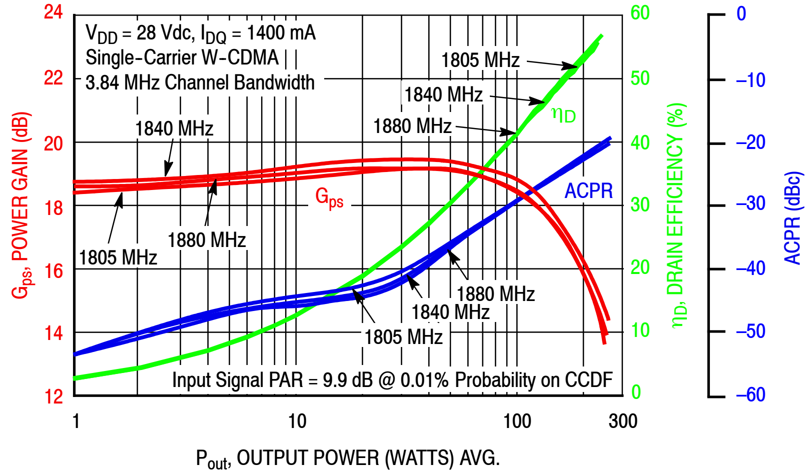


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

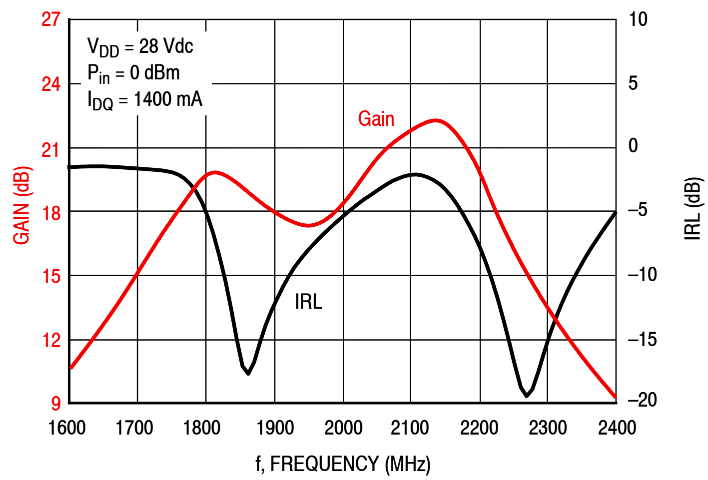


Figure 7. Broadband Frequency Response

Table 7. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1390 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.74 – j2.37	0.61 + j2.21	1.14 – j2.05	19.1	54.6	291	56.1	–13
1840	0.85 – j2.48	0.77 + j2.39	1.15 – j2.10	19.4	54.6	287	56.4	–14
1880	1.15 – j2.87	1.06 + j2.71	1.14 – j2.34	19.3	54.7	293	57.0	–15

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.74 – j2.37	0.57 + j2.27	1.19 – j2.21	17.0	55.5	357	59.9	–17
1840	0.85 – j2.48	0.74 + j2.46	1.18 – j2.37	17.0	55.4	350	58.6	–18
1880	1.15 – j2.87	1.03 + j2.82	1.21 – j2.54	17.1	55.5	356	59.5	–20

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

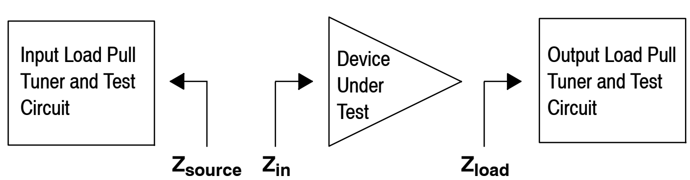
Table 8. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1390 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P1dB					
			Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.74 – j2.37	0.65 + j2.31	2.76 – j0.95	21.9	52.5	178	67.3	–17
1840	0.85 – j2.48	0.80 + j2.46	1.98 – j1.36	21.5	53.3	216	65.2	–18
1880	1.15 – j2.87	1.12 + j2.80	1.90 – j1.31	21.7	53.2	207	67.3	–19

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency					
			P3dB					
			Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1805	0.74 – j2.37	0.61 + j2.32	2.43 – j1.67	19.2	54.2	265	70.2	–21
1840	0.85 – j2.48	0.79 + j2.51	2.28 – j1.49	19.4	54.0	250	68.9	–24
1880	1.15 – j2.87	1.07 + j2.86	1.94 – j1.72	19.2	54.5	279	70.6	–24

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL LOAD PULL CONTOURS — 1840 MHz

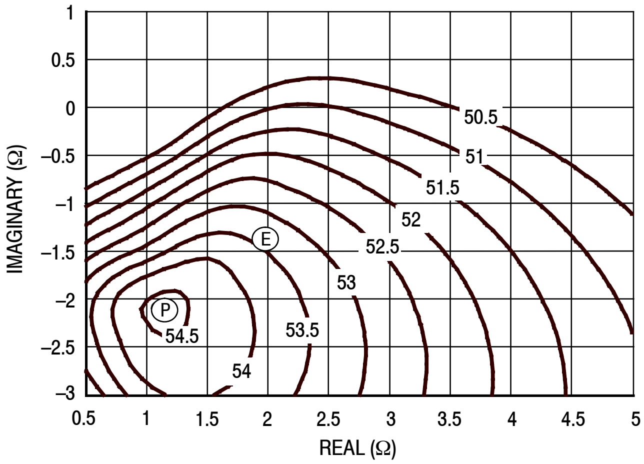


Figure 8. P1dB Load Pull Output Power Contours (dBm)

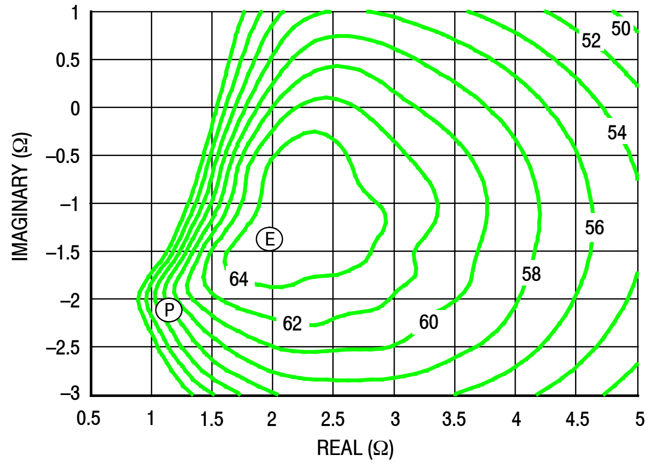


Figure 9. P1dB Load Pull Efficiency Contours (%)

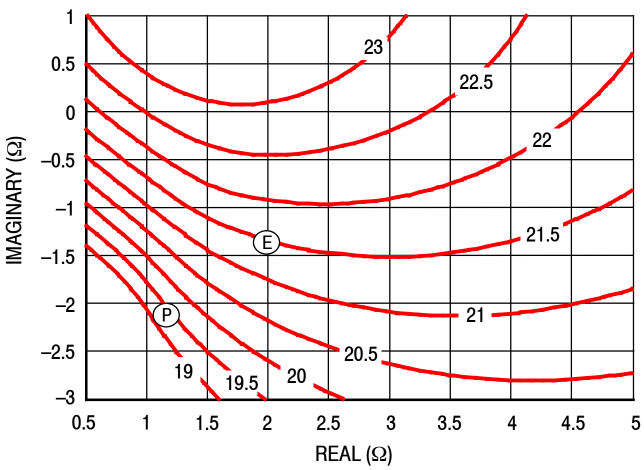


Figure 10. P1dB Load Pull Gain Contours (dB)

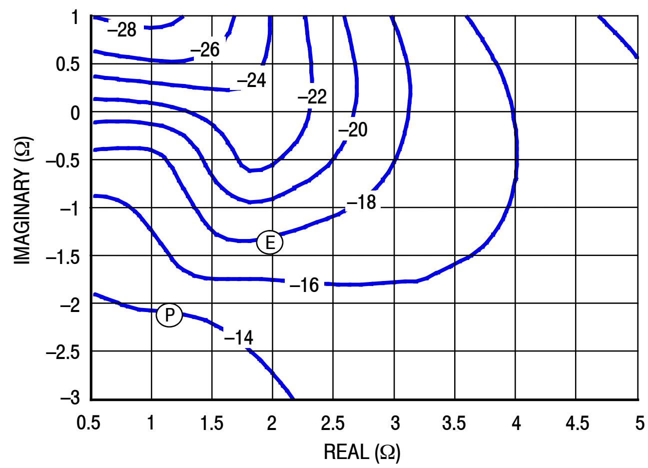


Figure 11. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power

E = Maximum Drain Efficiency

Gain

Drain Efficiency

Linearity

Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1840 MHz

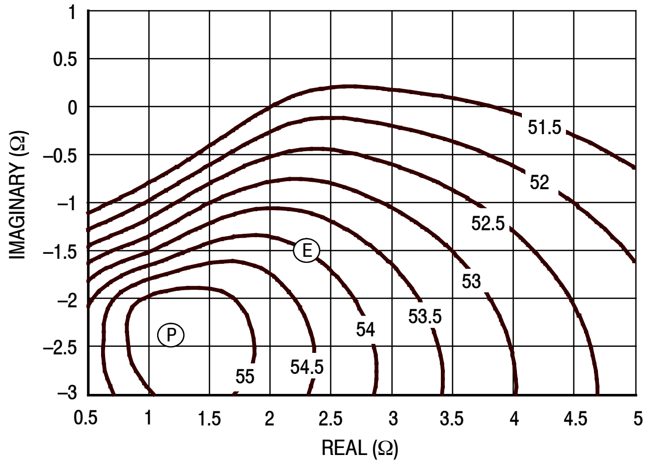


Figure 12. P3dB Load Pull Output Power Contours (dBm)

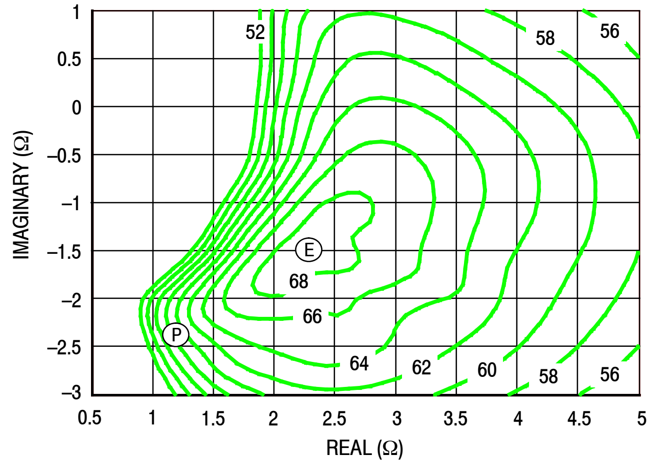


Figure 13. P3dB Load Pull Efficiency Contours (%)

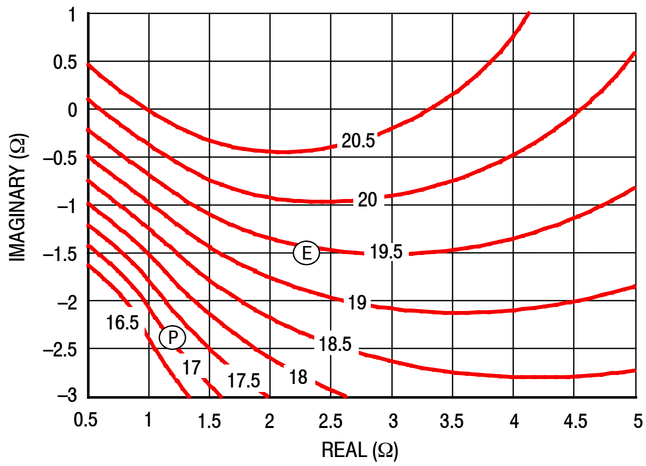


Figure 14. P3dB Load Pull Gain Contours (dB)

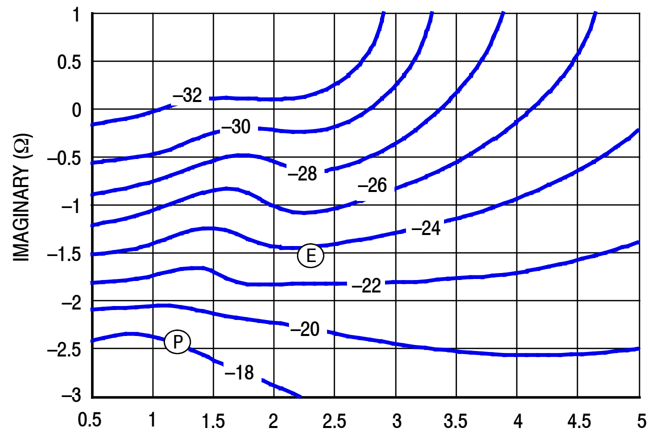


Figure 15. P3dB Load Pull AM/PM Contours (°)

NOTE: (P) = Maximum Output Power
(E) = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

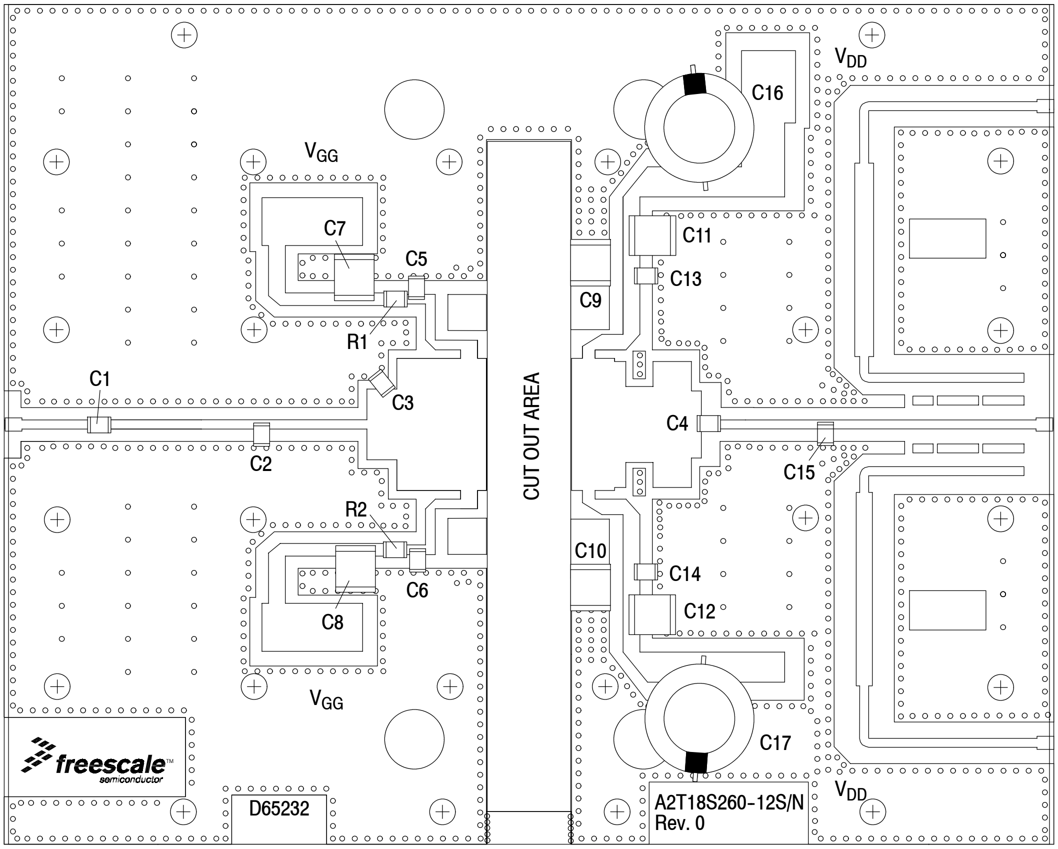


Figure 16. A2T18S260-12SR3 Test Circuit Component Layout — 1930–1995 MHz

Table 9. A2T18S260-12SR3 Test Circuit Component Designations and Values — 1930–1995 MHz

Part	Description	Part Number	Manufacturer
C1, C5, C6, C13, C14	15 pF Chip Capacitors	ATC600F150JT500XT	ATC
C2	0.6 pF Chip Capacitor	ATC600F0R6BT500XT	ATC
C3	0.7 pF Chip Capacitor	ATC600F0R7BT500XT	ATC
C4	6.8 pF Chip Capacitor	ATC600F6R8BT500XT	ATC
C7, C8, C9, C10, C11, C12	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C15	0.1 pF Chip Capacitor	ATC600F0R1BT500XT	ATC
C16, C17	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26-RH	Multicomp
R1, R2	6.8 Ω, 1/4 W Chip Resistors	CRCW12066R80FKEA	Vishay
PCB	Rogers RO4350B, 0.020″, ε_r = 3.66	D65232	MTL

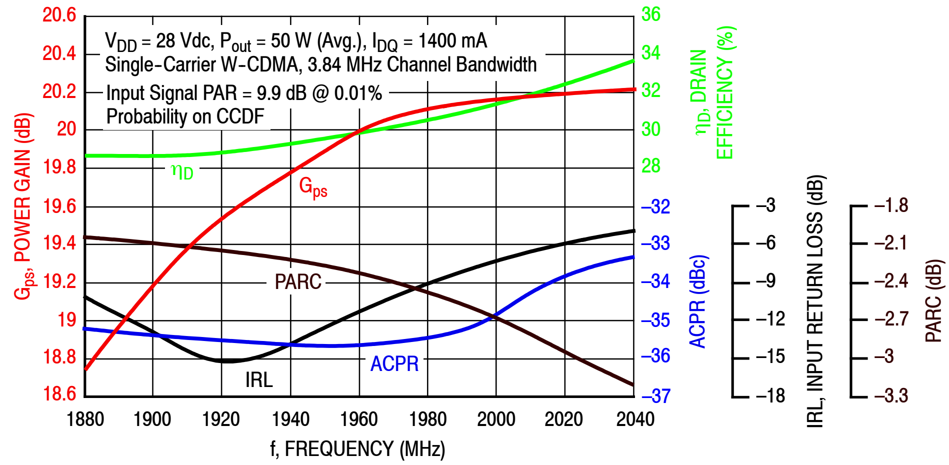


Figure 17. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 50 Watts Avg.

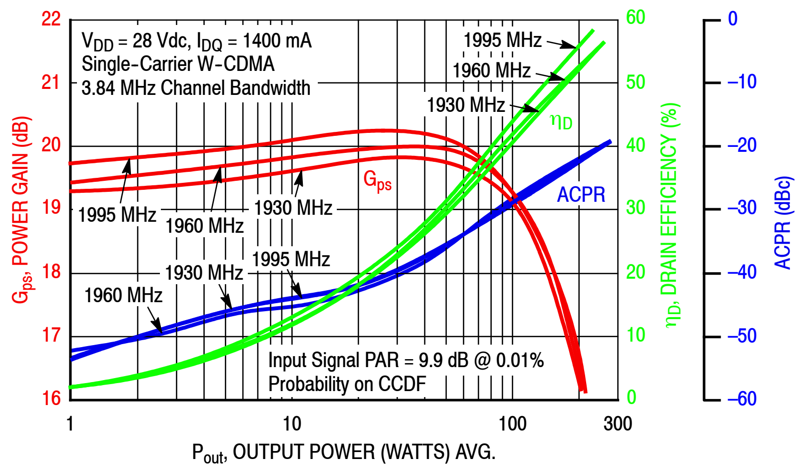


Figure 18. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

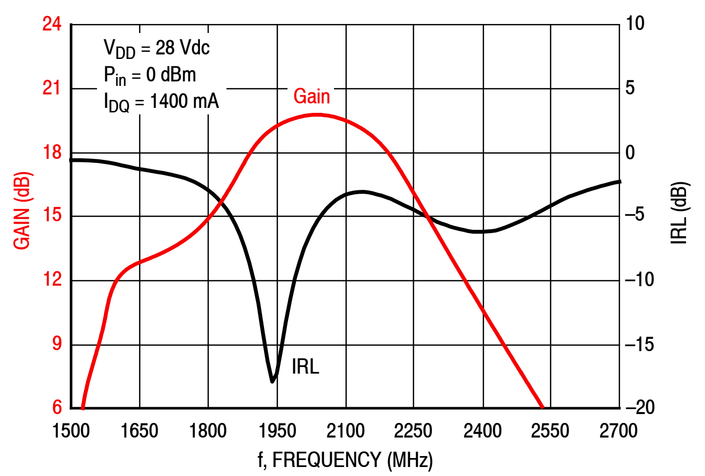


Figure 19. Broadband Frequency Response

Table 10. Load Pull Performance — Maximum Power Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1381 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Output Power					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.23 – j3.67	1.79 + j3.26	1.19 – j2.45	19.2	54.7	293	57.0	–15
1960	3.09 – j3.76	2.52 + j3.62	1.22 – j2.50	19.4	54.5	283	55.4	–15
1995	4.33 – j3.32	4.02 + j3.82	1.23 – j2.52	19.6	54.6	291	57.2	–14

			Max Output Power					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.23 – j3.67	1.80 + j3.44	1.26 – j2.62	17.0	55.5	352	58.8	–20
1960	3.09 – j3.76	2.61 + j3.86	1.31 – j2.67	17.2	55.3	339	57.0	–20
1995	4.33 – j3.32	4.29 + j4.05	1.35 – j2.70	17.4	55.4	350	59.2	–19

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

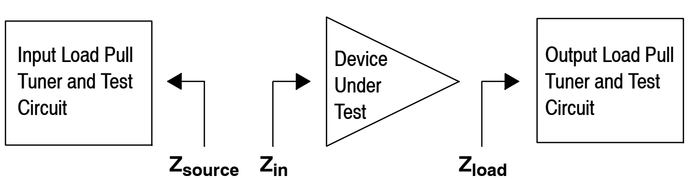
Table 11. Load Pull Performance — Maximum Efficiency Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1381 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

			Max Drain Efficiency					
			P1dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.23 – j3.67	1.92 + j3.39	1.68 – j1.31	21.6	53.1	206	66.7	–21
1960	3.09 – j3.76	2.77 + j3.69	1.66 – j1.25	21.9	52.8	189	64.7	–21
1995	4.33 – j3.32	4.40 + j3.80	1.48 – j1.47	21.8	53.3	215	67.0	–20

			Max Drain Efficiency					
			P3dB					
f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	2.23 – j3.67	1.86 + j3.53	1.67 – j1.51	19.4	54.2	261	69.7	–27
1960	3.09 – j3.76	2.85 + j3.93	1.66 – j1.28	19.9	53.6	226	67.6	–29
1995	4.33 – j3.32	4.59 + j4.05	1.52 – j1.62	19.6	54.3	269	70.2	–27

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.



P1dB - TYPICAL LOAD PULL CONTOURS — 1960 MHz

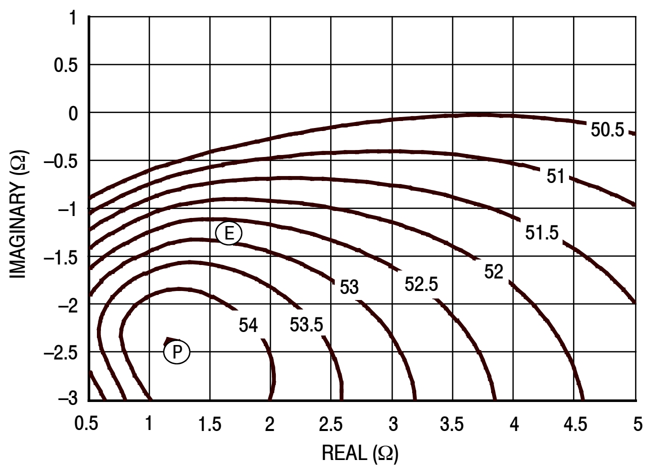


Figure 20. P1dB Load Pull Output Power Contours (dBm)

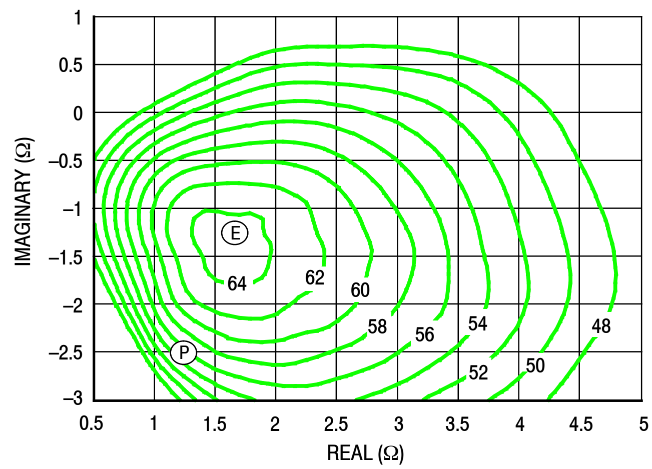


Figure 21. P1dB Load Pull Efficiency Contours (%)

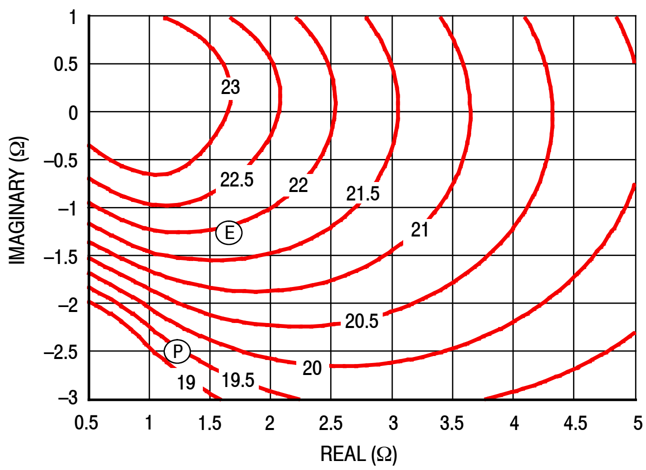


Figure 22. P1dB Load Pull Gain Contours (dB)

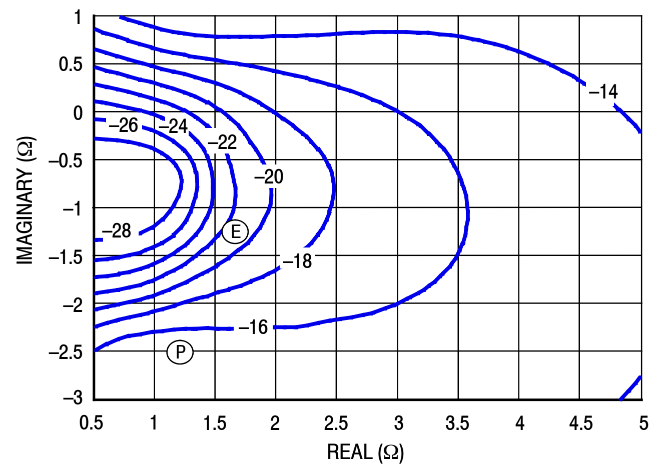


Figure 23. P1dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power
E = Maximum Drain Efficiency

Gain
Drain Efficiency
Linearity
Output Power

P3dB – TYPICAL LOAD PULL CONTOURS — 1960 MHz

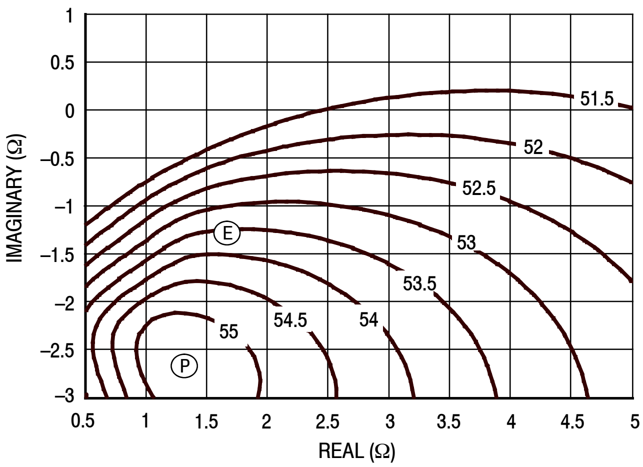


Figure 24. P3dB Load Pull Output Power Contours (dBm)

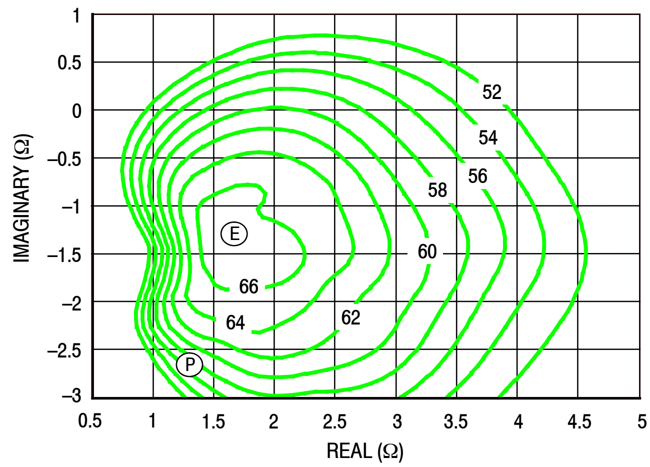


Figure 25. P3dB Load Pull Efficiency Contours (%)

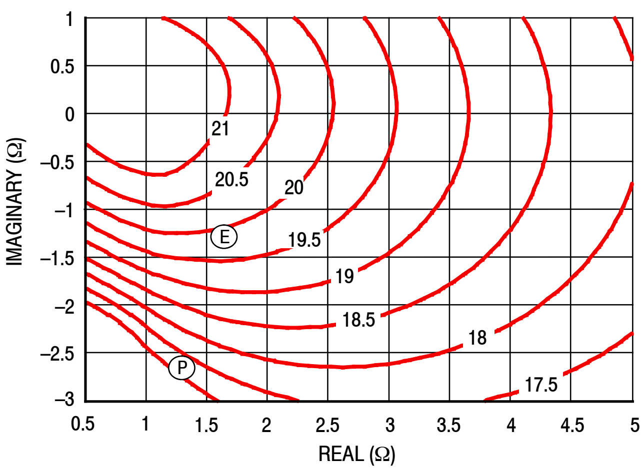


Figure 26. P3dB Load Pull Gain Contours (dB)

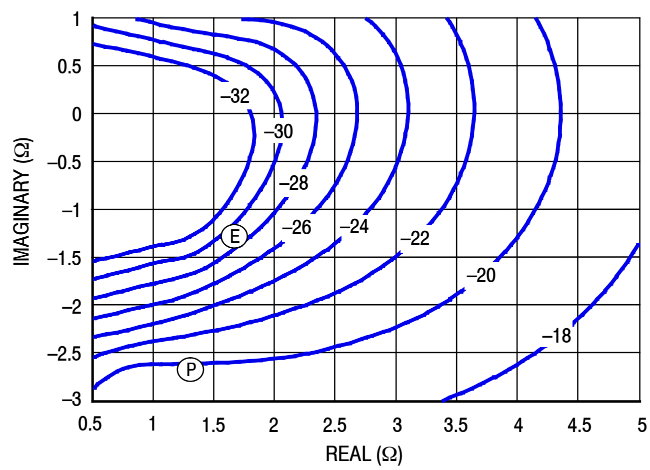


Figure 27. P3dB Load Pull AM/PM Contours (°)

NOTE: P = Maximum Output Power

E = Maximum Drain Efficiency

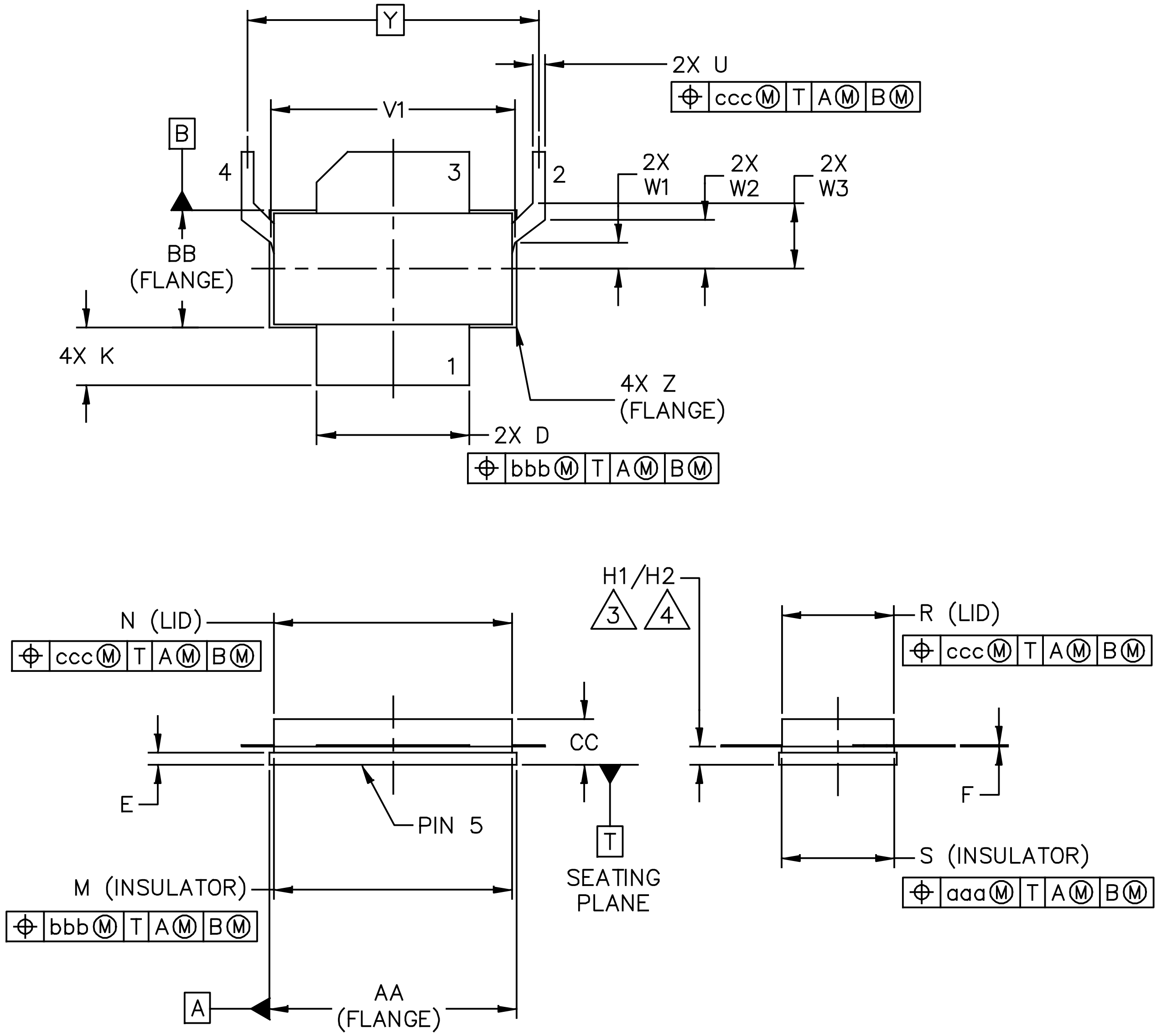
Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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	SOT1785-1	16 MAR 2016

NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE TO CLEAR THE EPOXY FLOW OUT PARALLEL TO DATUM B. H1 APPLIES TO PINS 1 & 3. H2 APPLIES TO PINS 2 & 4.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE AND COULD CHANGE ONCE SUFFICIENT MANUFACTURING DATA IS AVAILABLE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.805	.815	20.45	20.70	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.495	.505	12.57	12.83	V1	.795	.805	20.19	20.45
E	.035	.045	0.89	1.14	W1	.080	.090	2.03	2.29
F	.004	.007	0.10	0.18	W2	.155	.165	3.94	4.19
H1	.057	.067	1.45	1.70	W3	.210	.220	5.33	5.59
H2	.054	.070	1.37	1.78	Y	.956 BSC		24.28 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R0.00	R1.02
M	.774	.786	19.66	19.96	aaa	.005		0.13	
N	.772	.788	19.61	20.02	bbb	.010		0.25	
					ccc	.015		0.38	

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	SOT1785−1 16 MAR 2016	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following resources to aid your design process.

Application Notes

- AN1908: Solder Reflow Attach Method for High Power RF Devices in Air Cavity Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- .s2p File

Development Tools

- Printed Circuit Boards

To Download Resources Specific to a Given Part Number:

1. Go to http://www.nxp.com/RF
2. Search by part number
3. Click part number link
4. Choose the desired resource from the drop down menu

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Sept. 2016	• Initial release of data sheet

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Document Number: A2T18S260-12S
Rev. 0, 9/2016