PIC16C505

PIC16C505 Rev. A Silicon/Data Sheet Errata

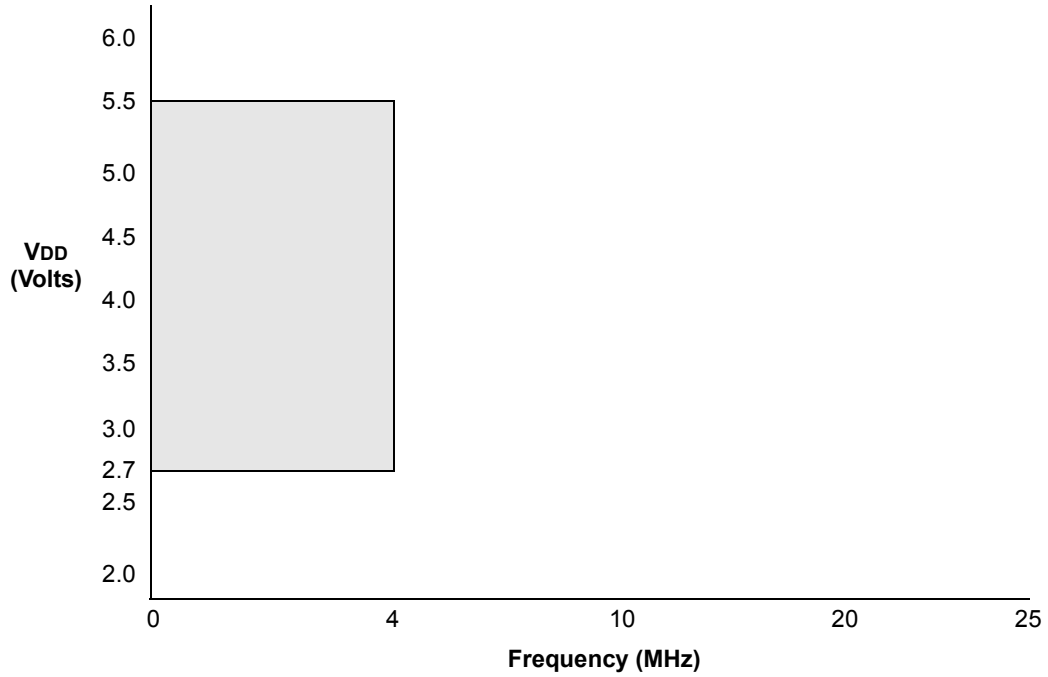
The PIC16C505 parts you have received conform functionally to the Device Data Sheet (DS40192C), except for the anomalies described below.

All of the issues listed here will be addressed in future revisions of the PIC16C505 silicon.

1. Module: Voltage Frequency Graphs

Use the following graphs for the respective graphs in the Electrical Specification Section.

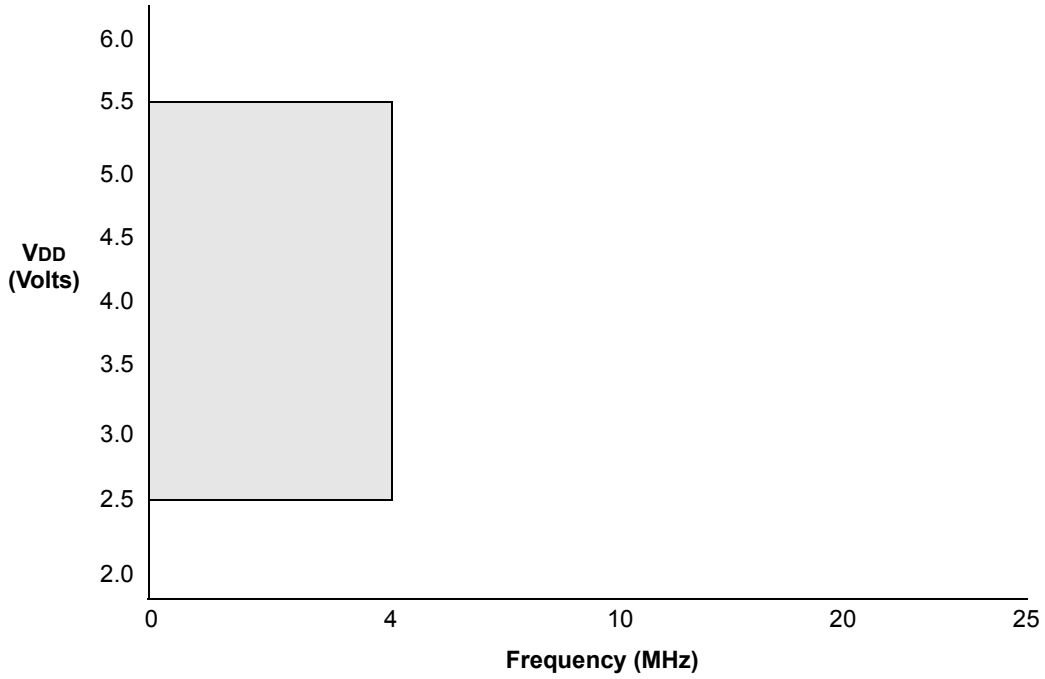
FIGURE 1: PIC16LC505 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ 0°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

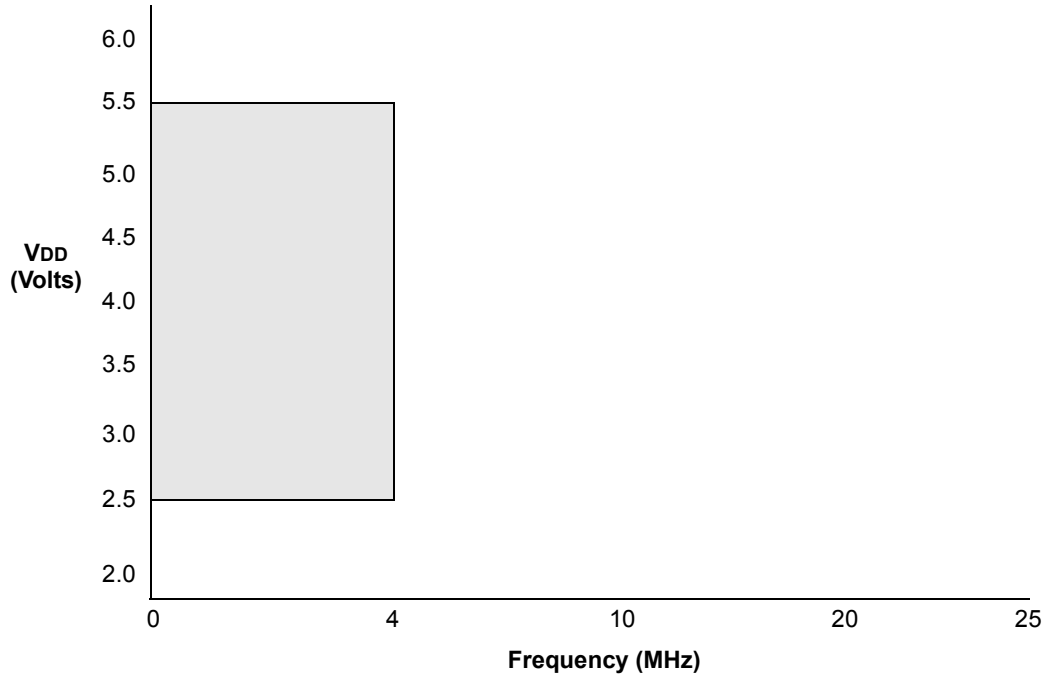
FIGURE 2: PIC16LC505 VOLTAGE-FREQUENCY GRAPH, 0°C ≤ TA ≤ +70°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

FIGURE 3: PIC16LC505 VOLTAGE-FREQUENCY GRAPH, +70°C ≤ TA ≤ +125°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

2: The maximum rated speed of the part limits the permissible combinations of voltage and frequency. Please reference the Product Identification System section for the maximum rated speed of the parts.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40192C), the following clarifications and corrections should be noted.

1. Module: Special Function Register

Corrections to the Special Function Register (SFR) Summary are shown in Table 4-1.

TABLE 4-1: SPECIAL FUNCTION REGISTER (SFR) SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on All Other Resets(2)
04h	FSR	Indirect Data Memory Address Pointer								100x xxxx	10uu uuuu

Legend: Shaded cells not used by PORT Registers, read as '0', – = unimplemented, read as '0', x = unknown, u = unchanged, q = depends on condition.

Note 1: If Reset was due to wake-up on pin change, then bit 7 = 1. All other Resets will cause bit 7 = 0.

2: Other (non-power-up) Resets include external Reset through $\overline{\text{MCLR}}$, Watchdog Timer and wake-up on pin change Reset.

2. Module: DC Characteristics

Corrections for the DC Characteristics, Sections 10.1, 10.2 and 10.3 are shown.

10.1 DC CHARACTERISTICS: PIC16C505-04 (Commercial, Industrial, Extended) PIC16C505-20(Commercial, Industrial, Extended)

DC CHARACTERISTICS POWER SUPPLY PINS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended)				
Parm. No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D010	Supply Current(3)	IDD	—	0.8	1.4	mA	FOSC = 4MHz, VDD = 5.5V, WDT disabled, XT mode **(Note 4)**
			—	0.6	1.0	mA	FOSC = 4MHz, VDD = 3.0V, WDT disabled, XT mode **(Note 4)**
			—	3	7	mA	FOSC = 10MHz, VDD = 3.0V, WDT disabled,
			—	4	12	mA	HS mode **(Note 6)**
			—	4.5	16	mA	FOSC = 20MHz, VDD = 4.5V, WDT disabled, HS mode
			—	19	27	µA	FOSC = 20MHz, VDD = 5.5V, WDT disabled, HS mode FOSC = 32kHz, VDD = 3.0V, WDT disabled, LP mode **(Note 6)**
D020	Power-Down Current (5)	IPD	—	0.25	4	µA	VDD = 3.0V **(Note 6)**
			—	0.4	5.5	µA	VDD = 4.5V **(Note 6)**
			—	3	8	µA	VDD = 5.5V, Industrial
			—	5	14	µA	VDD = 5.5V, Extended Temp.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

a) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

b) For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kOhm.

5: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS.

6: Commercial temperature range only.

10.2 DC CHARACTERISTICS: PIC16LC505-04 (Commercial, Industrial)

DC CHARACTERISTICS POWER SUPPLY PINS			Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial)				
Parm. No.	**Characteristic**	**Sym**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
D010	Supply Current(3)	IDD	—	0.8	1.4	mA	FOSC = 4MHz, VDD = 5.5V, WDT disabled, XT mode **(Note 4)**
			—	0.4	0.8	mA	FOSC = 4MHz, VDD = 2.5V, WDT disabled, XT mode **(Note 4)**
			—	15	23	µA	FOSC = 32kHz, VDD = 2.5V, WDT disabled, LP mode **(Note 6)**
D020	Power-Down Current (5)	IPD	—	0.25	3	µA	VDD = 2.5V **(Note 6)**
			—	0.25	4	µA	VDD = 3.0V **(Note 6)**
			—	3	8	µA	VDD = 5.5V Industrial

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

2: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern and temperature also have an impact on the current consumption.

c) The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VSS, T0CKI = VDD, $\overline{MCLR}$ = VDD; WDT enabled/disabled as specified.

d) For standby current measurements, the conditions are the same, except that the device is in Sleep mode.

4: Does not include current through REXT. The current through the resistor can be estimated by the formula: IR = VDD/2REXT (mA) with REXT in kOhm.

5: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS.

6: Commercial temperature range only.

10.3 DC CHARACTERISTICS: PIC16C505-04 (Commercial, Industrial, Extended) PIC16C505-20(Commercial, Industrial, Extended) PIC16LC505-04 (Commercial, Industrial))

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature 0°C ≤ TA ≤ +70°C (commercial) –40°C ≤ TA ≤ +85°C (industrial) –40°C ≤ TA ≤ +125°C (extended)				
Param No.	**Characteristic**	**Sym**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
	Input High Voltage	VIH					
	I/O ports			—			
D040	with TTL buffer		2.0	—	VDD	V	4.5 ≤ VDD ≤ 5.5V
D040A			0.25VDD+ 0.8V	—	VDD	V	Otherwise
	Input Leakage Current (Notes 2, 3)	IIL					
D061	RB3/$\overline{\text{MCLR}}$ (Note 5)		8	130	250	µA	Vss ≤ VPIN ≤ VDD
D061A	RB3/$\overline{\text{MCLR}}$ (Note 6)		—	—	±5	µA	Vss ≤ VPIN ≤ VDD
D070	RB weak pull-up current (Note 4)	IPUR	179	250	333	µA	VDD = 5V, VPIN = VSS

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16C505 be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: Does not include RB3. For RB3 see parameters D0061 and D0061A.

5: This specification applies to RB3/$\overline{\text{MCLR}}$ configured as external $\overline{\text{MCLR}}$ and RB3/$\overline{\text{MCLR}}$ configured as input with internal pull-up enabled.

6: This specification applies to RB3/$\overline{\text{MCLR}}$ configured as external $\overline{\text{MCLR}}$ and RB3/$\overline{\text{MCLR}}$ configured as input with pull-up disabled. The leakage current of the $\overline{\text{MCLR}}$ circuit is higher than the standard I/O logic.

3. Module: PORTB Pull-up Register Ranges

Corrections for the PORTB pull-up resistor ranges are shown in Table 10-1.

TABLE 10-1: PULL-UP RESISTOR RANGES – PIC16C505

VDD (Volts)	Temperature (°C)	Min	Typ	Max	Units
RB0/RB1/RB4					
2.5	–40	38K	42K	63K	Ω
	25	42K	48K	63K	Ω
	85	42K	49K	63K	Ω
	125	50K	55K	63K	Ω
5.5	–40	15K	17K	20K	Ω
	25	18K	20K	23K	Ω
	85	19K	22K	25K	Ω
	125	22K	24K	28K	Ω
RB3(1)					
2.5	–40	65K	80K	850K	Ω
	25	80K	100K	1150K	Ω
	85	85K	110K	1300K	Ω
	125	100K	120K	1500K	Ω
5.5	–40	50K	60K	600K	Ω
	25	60K	65K	750K	Ω
	85	65K	80K	900K	Ω
	125	75K	90K	990K	Ω

* These parameters are characterized but not tested.

Note 1: The weak pull-up resistor and associated current for the RB3/$\overline{\text{MCLR}}$ pin is nonlinear when the respective pin voltage is less than VDD – 1.0V. See parameter D061 for RB3/$\overline{\text{MCLR}}$ pin current specifications.

4. Module: Reset (CLKIN/CLKOUT)

For the section titled “Reset”, additional information is provided on OSC1/CLKIN and OSC2/CLKOUT pin states during a $\overline{\text{MCLR}}$.

Reset

When $\overline{\text{MCLR}}$ is asserted, the state of the OSC1/CLKIN and CLKOUT/OSC2 pins are as follows:

CLKIN/CLKOUT PIN STATES WHEN $\overline{\text{MCLR}}$ ASSERTED

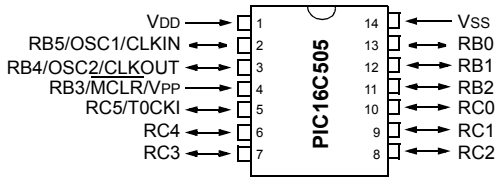
Oscillator Mode	OSC1/CLKIN Pin	OSC2/ CLKOUT Pin
EXTRC, CLKOUT on OSC2	OSC1 pin is tri-stated and driven by external circuit	OSC2 pin is driven low
EXTRC, OSC2 is I/O	OSC1 pin is tri-stated and driven by external circuit	OSC2 pin is tri-state input
INTRC, CLKOUT on OSC2	OSC1 pin is tri-state input	OSC2 pin is driven low
INTRC, OSC2 is I/O	OSC1 pin is tri-state input	OSC2 pin is tri-state input

5. Module: Packaging (TSSOP)

Update data sheet to include TSSOP as follows:

Pin Diagram:

PDIP, SOIC, TSSOP, Ceramic Side Brazed



PIC16C505 Product Identification System

PART NO. -XX X /XX XXX

Pattern:	Special Requirements		
Package:	SL	=	150 mil SOIC
	P	=	300 mil PDIP
	JW	=	300 mil Windowed Ceramic Side Brazed
	ST	=	**Thin Shrink Small Outline (TSSOP)**
Temperature Range:	-	=	0°C to +70°C
	I	=	-40°C to +85°C
	E	=	-40°C to +125°C
Frequency Range:	04	=	4 MHz (XT, INTRC, EXTRC OSC)
	20	=	20 MHz (HS OSC)
Device	PIC16C505		
	PIC16LC505		
	PIC16C505T (Tape & reel for SOIC only)		
	PIC16LC505T (Tape & reel for SOIC only)		

Examples

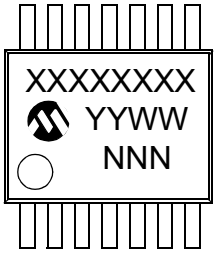
a) PIC16C505-04/P Commercial Temp., PDIP Package, 4 MHz, normal VDD limits

b) PIC16C505-04I/SL Industrial Temp., SOIC package, 4 MHz, normal VDD limits

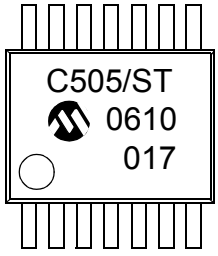
c) PIC16C505-04I/P Industrial Temp., PDIP package, 4 MHz, normal VDD limits

10.3 Package Marking Information

14-Lead TSSOP



Example



APPENDIX A: REVISION HISTORY

Revision D (5/2007)

Updates throughout document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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