



# STL38N65M5

N-channel 650 V, 0.090  $\Omega$  typ., 22.5 A MDmesh™ V Power MOSFET in a PowerFLAT™ 8x8 HV package

Datasheet — preliminary data

## Features

Order code	V <sub>DS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STL38N65M5	710 V	0.105 $\Omega$	22.5 A <sup>(1)</sup>

1. The value is rated according to R<sub>thj-case</sub> and limited by package.

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

## Applications

- Switching applications

## Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

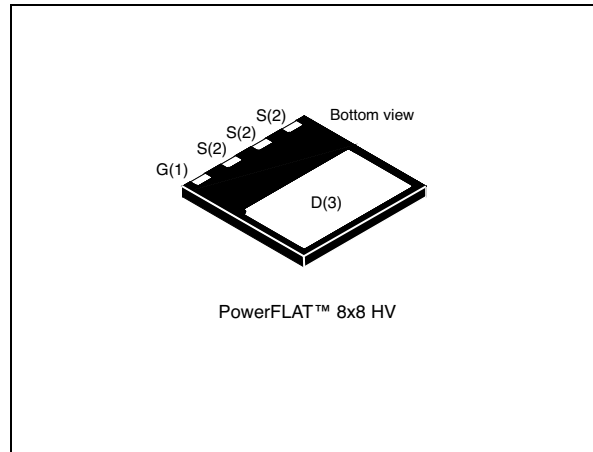


Figure 1. Internal schematic diagram

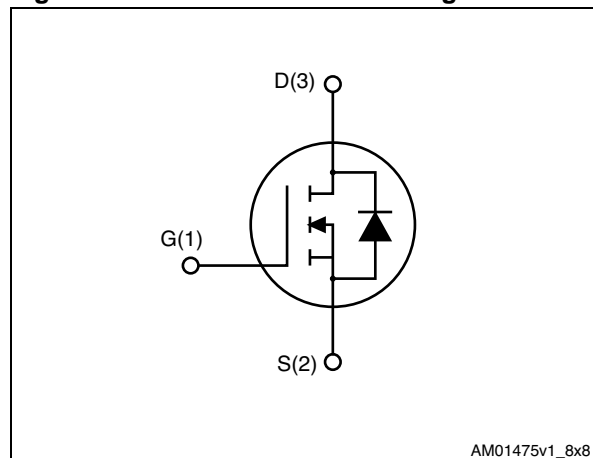


Table 1. Device summary

Order code	Marking	Package	Packaging
STL38N65M5	38N65M5	PowerFLAT™ 8x8 HV	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	650	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	22.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	16	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	90	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	3.5	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	2.2	A
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	2.8	W
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	7	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	660	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-case}$ , and limited by package.
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of  $\text{inch}^2$ , 2oz Cu.
4.  $I_{SD} \leq 22.5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of  $\text{inch}^2$ , 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$ $V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 12.5\text{ A}$		0.090	0.105	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	3000	-	pF
$C_{oss}$	Output capacitance			74		pF
$C_{rss}$	Reverse transfer capacitance			5.8		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0,$ $V_{DS} = 0\text{ to }80\% V_{(BR)DSS}$	-	70	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related			244		pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	2.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 15\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	71	-	nC
$Q_{gs}$	Gate-source charge			18		nC
$Q_{gd}$	Gate-drain charge			30		nC

- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 400\text{ V}$ , $I_D = 20\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 20</a> )		66		ns
$t_{r(V)}$	Voltage rise time		-	9	-	ns
$t_{f(i)}$	Crossing fall time		9			ns
$t_{c(off)}$	Crossing time		13			ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		22.5	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)				90	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 22.5\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see <a href="#">Figure 17</a> )	-	354		ns
$Q_{rr}$	Reverse recovery charge			6		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			34		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 22.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17</a> )	-	428		ns
$Q_{rr}$	Reverse recovery charge			8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			38		A

1. The value is rated according to  $R_{thj-case}$  and limited by package
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

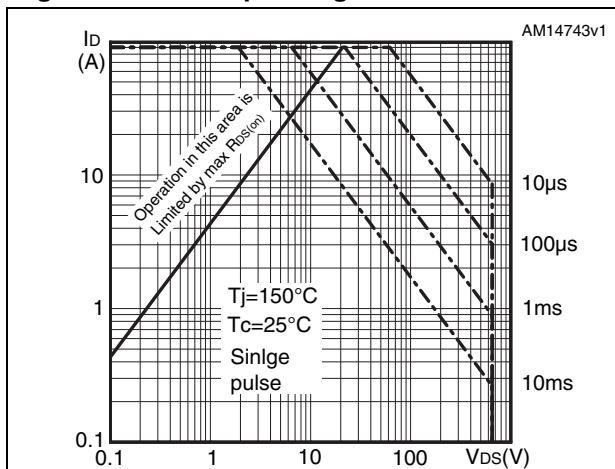


Figure 3. Thermal impedance

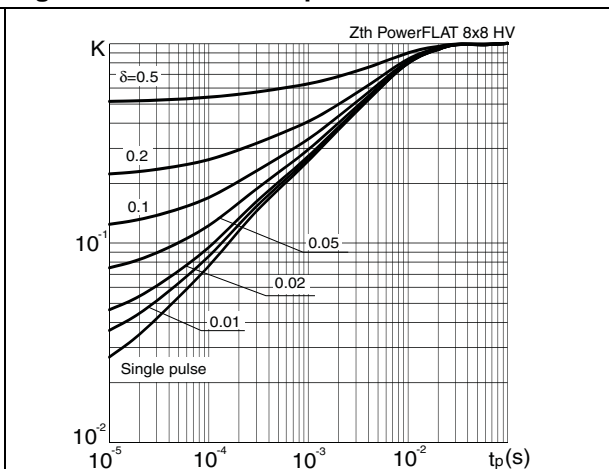


Figure 4. Output characteristics

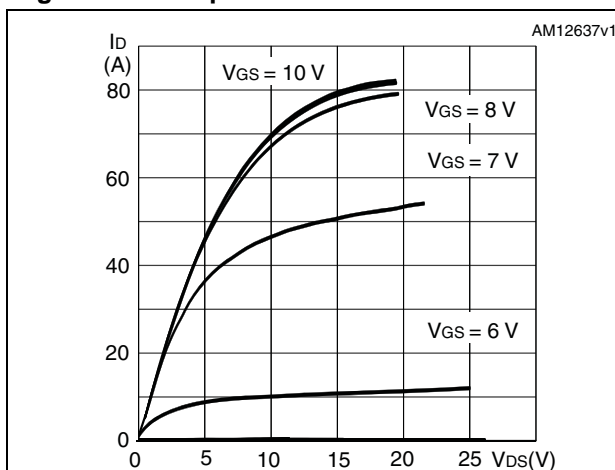


Figure 5. Transfer characteristics

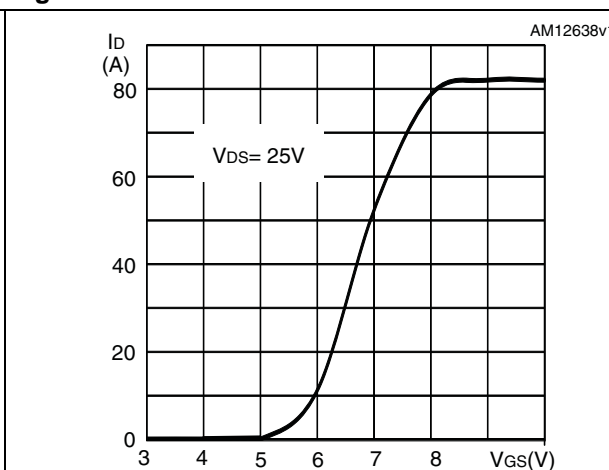


Figure 6. Gate charge vs gate-source voltage

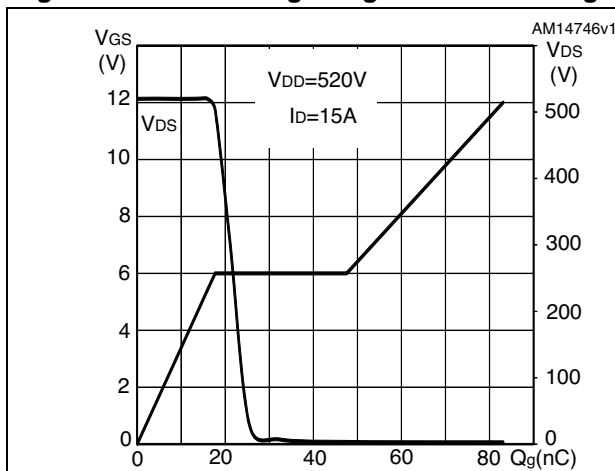


Figure 7. Static drain-source on-resistance

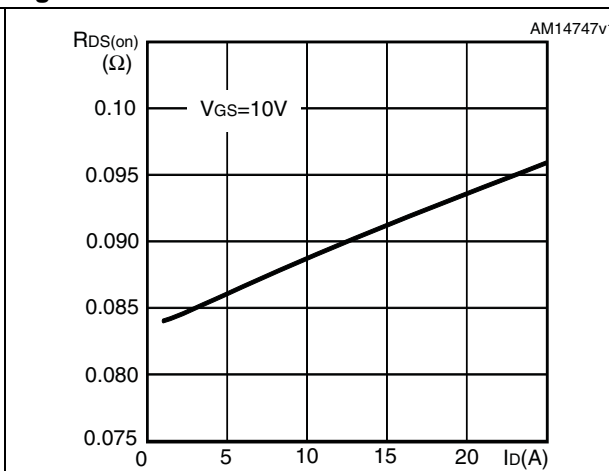


Figure 8. Capacitance variations

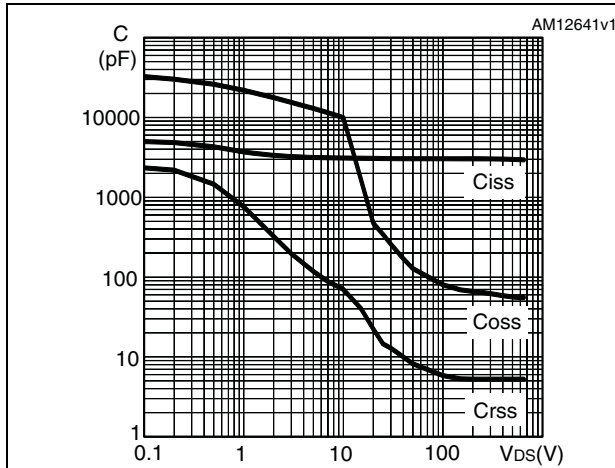


Figure 9. Output capacitance stored energy

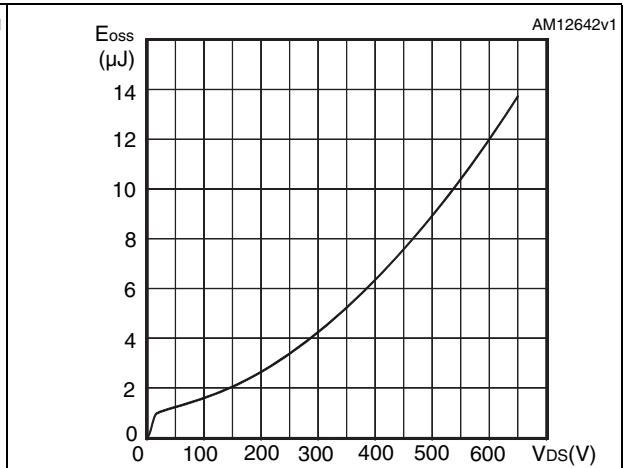


Figure 10. Normalized gate threshold voltage vs temperature

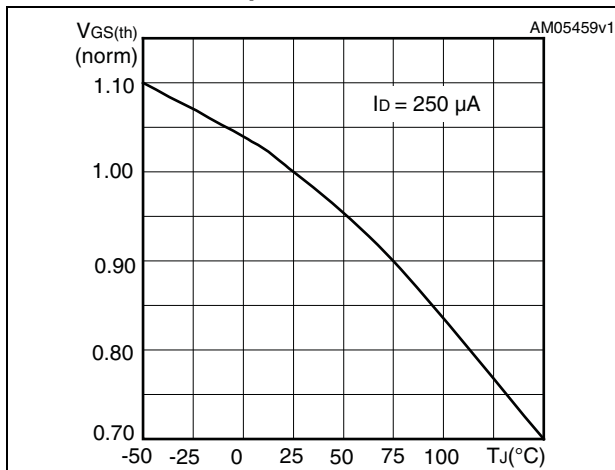


Figure 11. Normalized on-resistance vs temperature

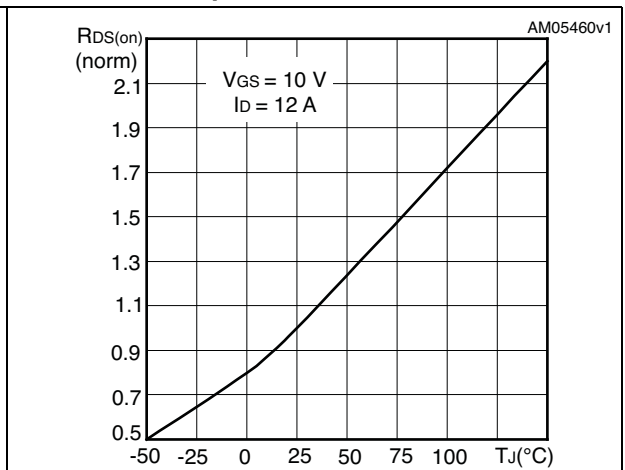


Figure 12. Source-drain diode forward characteristics

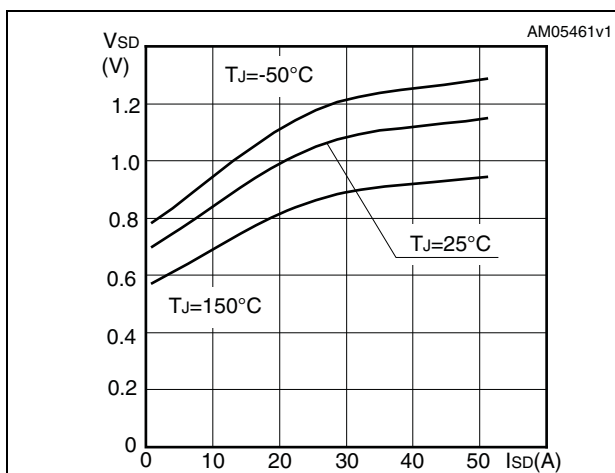


Figure 13. Normalized VDS vs temperature

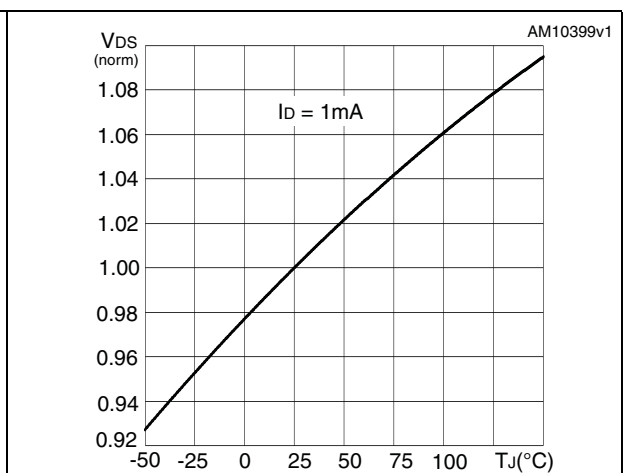
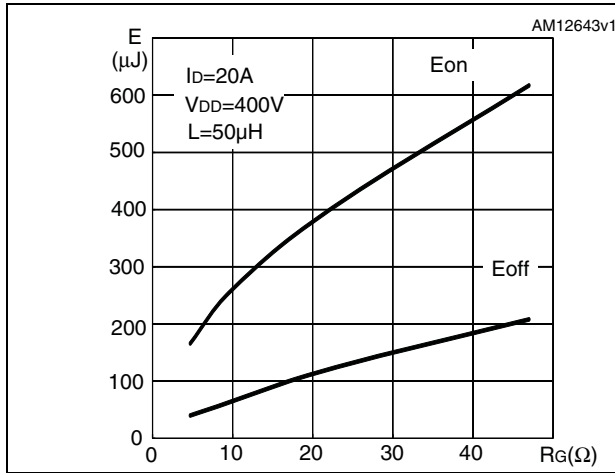


Figure 14. Switching losses vs gate resistance (1)



1.  $E_{on}$  including reverse recovery of a SiC diode.



### 3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit



Figure 17. Test circuit for inductive load switching and diode recovery times

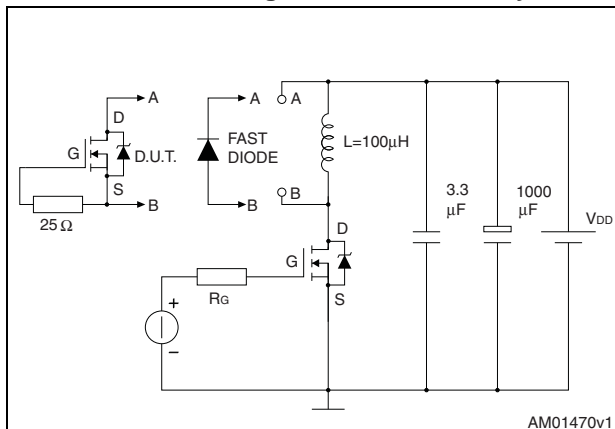


Figure 18. Unclamped inductive load test circuit



Figure 19. Unclamped inductive waveform

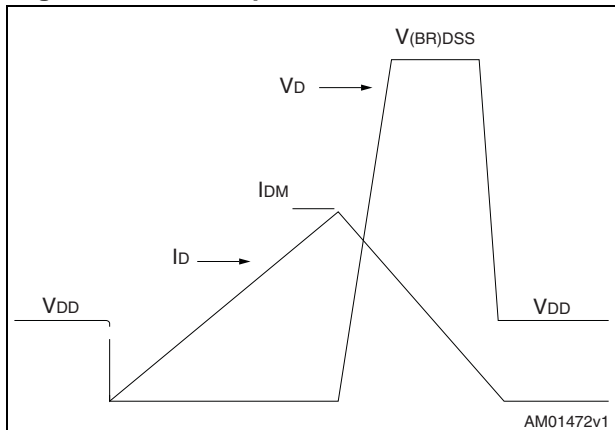
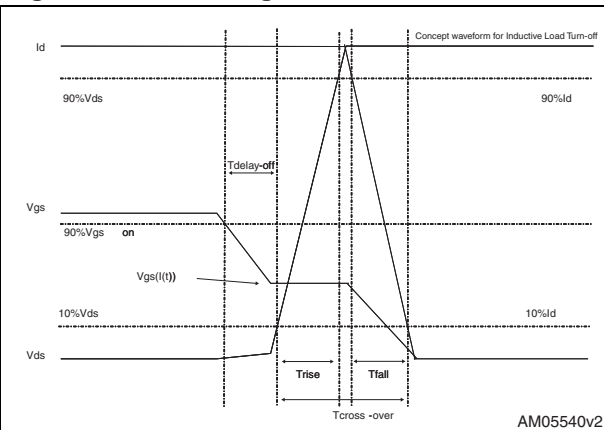


Figure 20. Switching time waveform



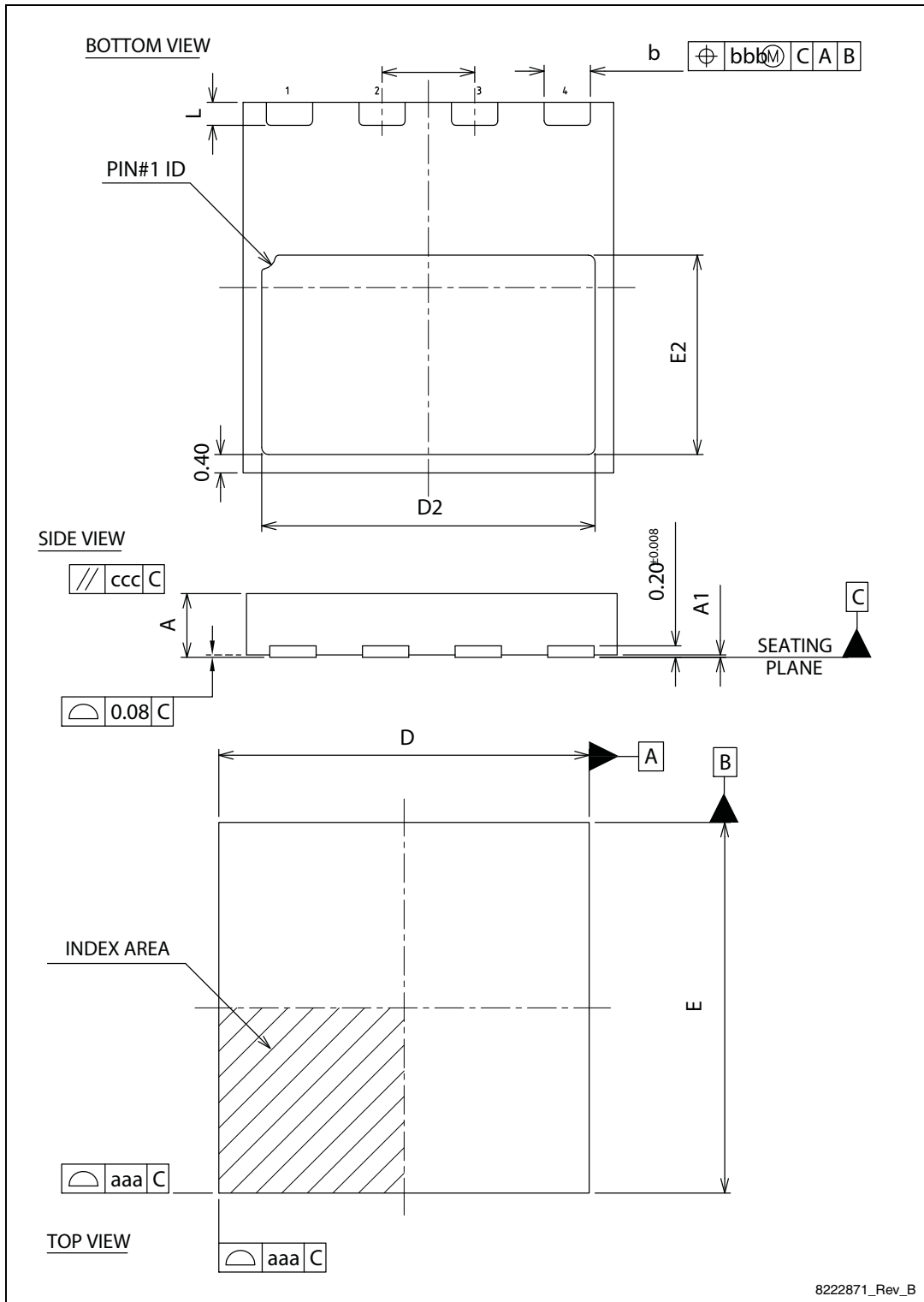
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. PowerFLAT™ 8x8 HV mechanical data

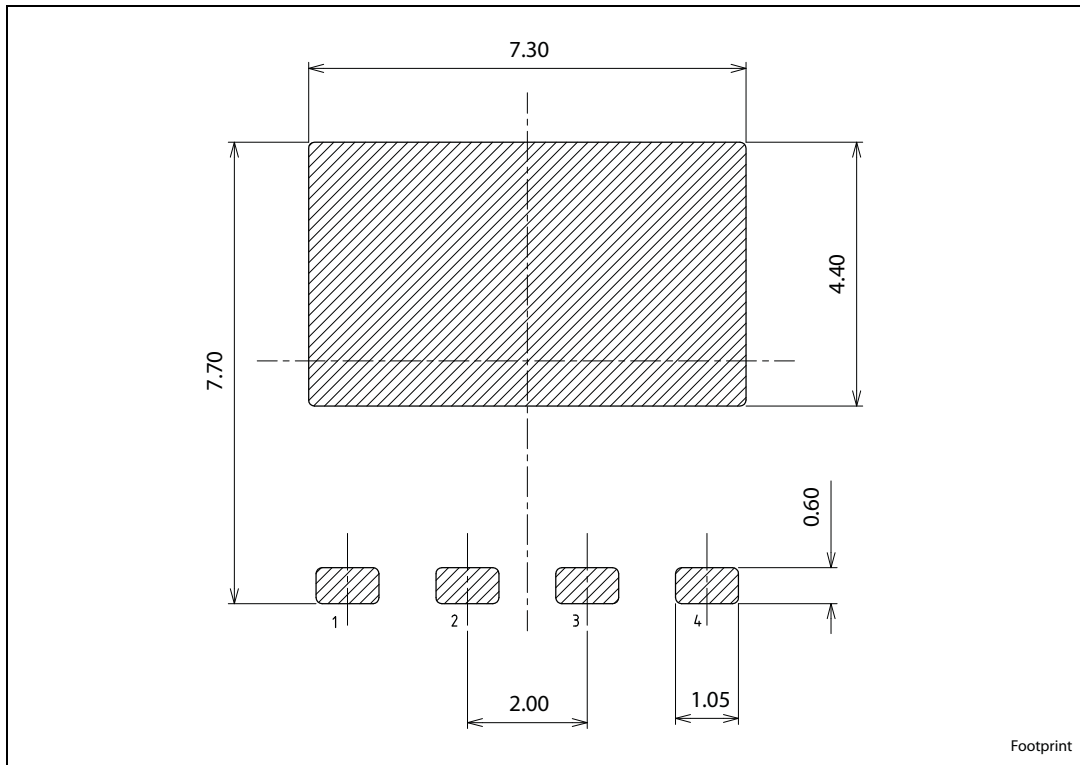
Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60
aaa		0.10	
bbb		0.10	
ccc		0.10	

Figure 21. PowerFLAT™ 8x8 HV drawing mechanical data



8222871\_Rev\_B

Figure 22. PowerFLAT™ 8x8 HV recommended footprint



# 5 Packaging mechanical data

Figure 23. PowerFLAT™ 8x8 HV tape

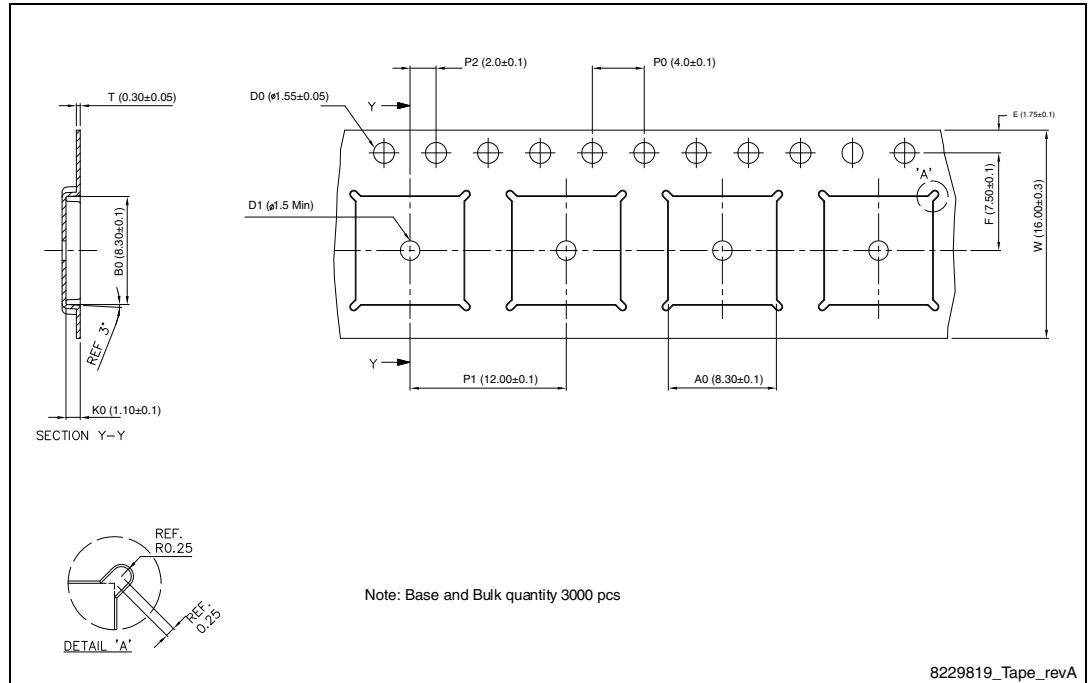


Figure 24. PowerFLAT™ 8x8 HV package orientation in carrier tape.

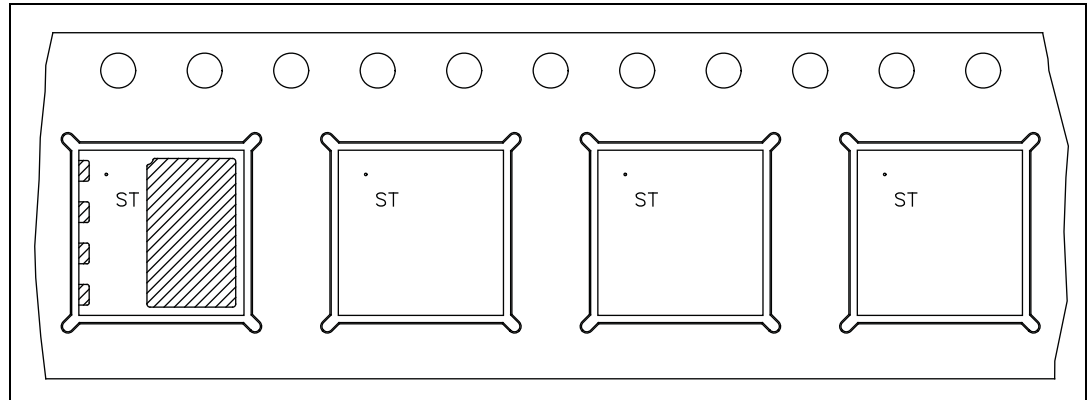
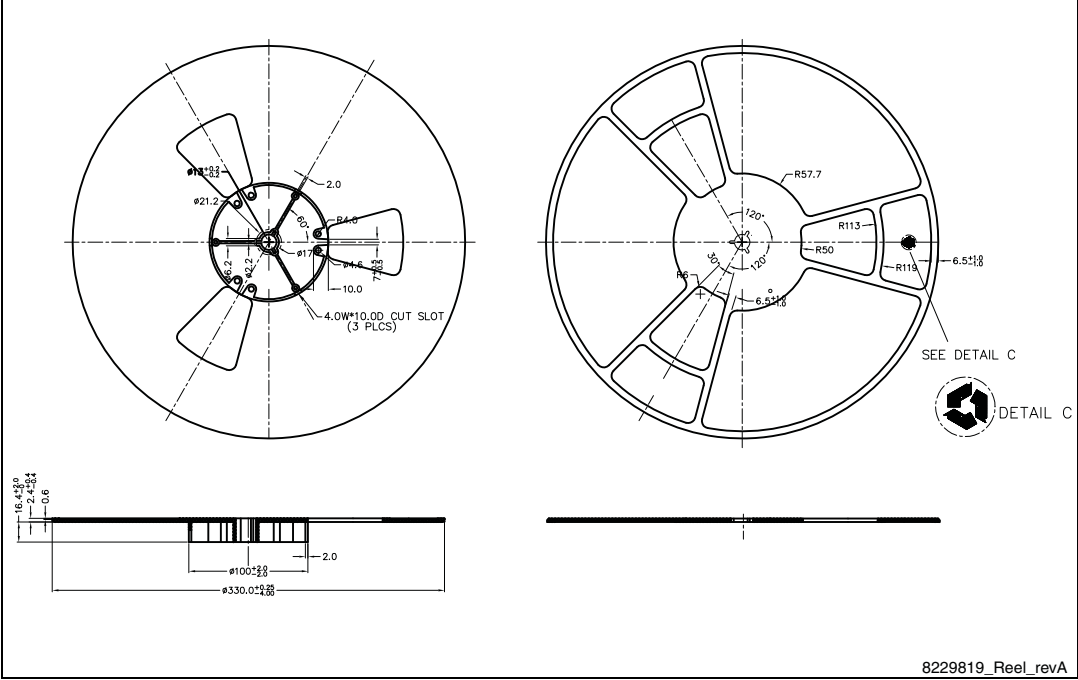


Figure 25. PowerFLAT™ 8x8 HV reel



## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
17-Jan-2013	1	First release.



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