AN2787
Application note

Monolithic VR demonstration board for chipset and DDR2/3 supply for ultramobile PC (UMPC) applications

Introduction

PM6641 demonstration board order code: STEVAL-ISA050V1 (previously coded as PM6641EVAL).

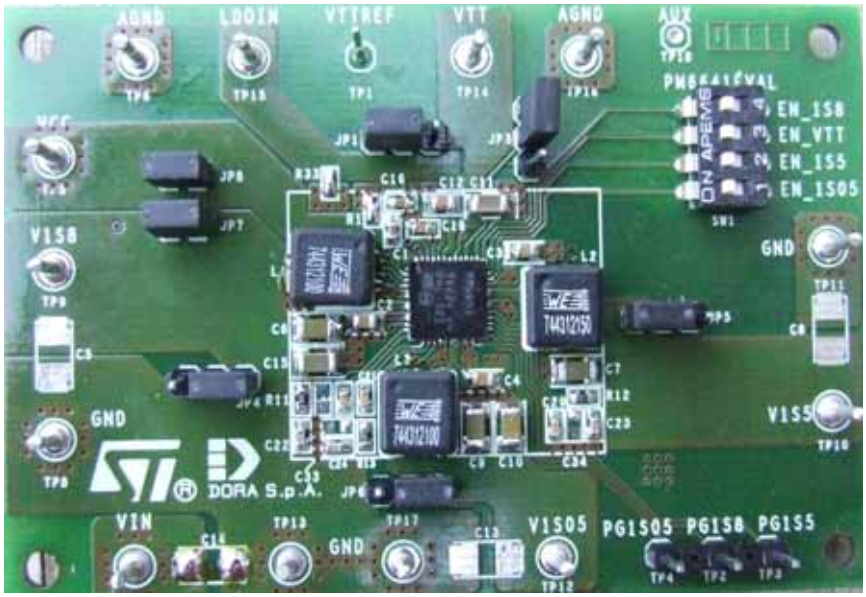
The PM6641 demonstration board is a monolithic voltage regulator (VR) module with internal power MOSFETs, specifically designed to supply DDR2/3 memory and chipset in ultramobile PC and real estate constrained portable systems.

It integrates three independent, adjustable, constant frequency buck converters, a ±2 Apk low dropout (LDO) linear regulator, and a ±15 mA low-noise buffered reference.

Each regulator is provided with basic undervoltage (UV) and overvoltage (OV) protections, programmable soft-start and current limit, active soft-end, and pulse skipping at light loads.

This document describes all features of the PM6641 demonstration board.

Figure 1. PM6641 demonstration board



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1 Main features

Switching section

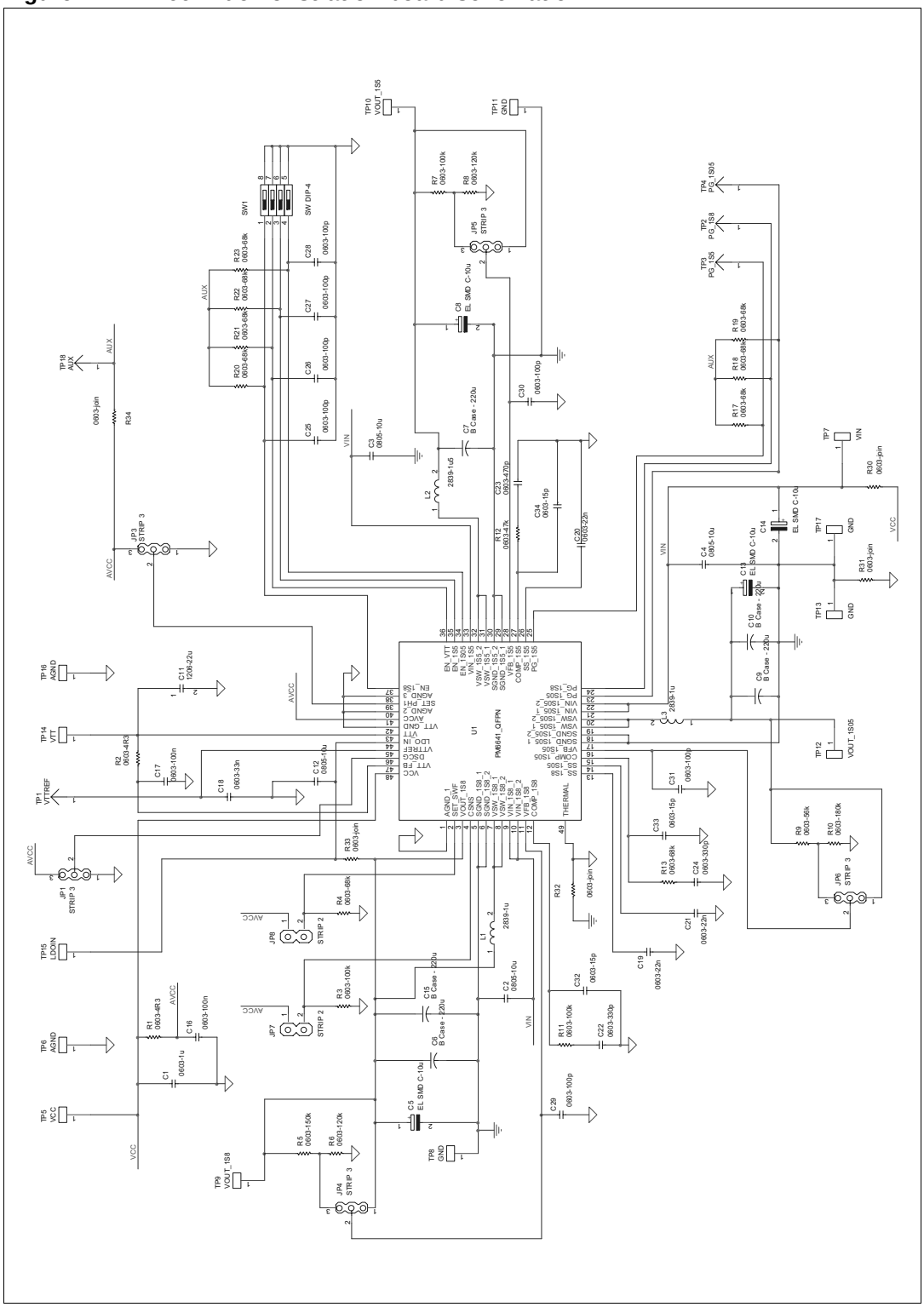
- 0.8 V ±1% voltage reference
- 2.7 V to 5.5 V input voltage range
- Fast response, constant frequency, current mode control
- Three independent, adjustable, SMPS for DDR2/3 (VDDQ) and chipset supply
- S3-S5 states compliant with DDR2/3 section
- Active soft-end for all outputs
- Selectable tracking discharge for VDDQ
- Separate Power Good signals
- Pulse skipping at light load
- Programmable current limit and soft-start for all outputs
- Latched OVP, UVP protection
- Thermal protection

Reference and termination voltages (VTTREF and VTT)

- ±2 Apk LDO for DDR2/3 termination (VTT) with foldback
- Remote VTT output sensing
- High-Z VTT output in S3
- ±15 mA low-noise DDR2/3 buffered reference (VTTREF)

2 Demonstration kit schematic

Figure 2. PM6641 demonstration board schematic



3 Bill of material

Table 1. PM6641 demonstration board list of components

Qty	Component	Description	Package	Part number	MFR	Value	Note
1	C1	Ceramic, 10 V, X5R, 20%	SMD 0603		Standard	1 µ	
4	C2, C3, C4, C12	Ceramic, 10 V, X5R, 20%	SMD 0805	GRM21BR61A106KE19	Murata	10 µ	
4	C5, C8, C13, C14		SMD C case				n.m.
5	C6, C7, C9, C10, C15	Ceramic, 4 V, X5R, 20%	SMD 1206	AMK316BJ107ML	Taiyo Yuden	100 µ	
1	C11	Ceramic, 6.3 V, X5R, 10%	SMD 1206	GRM31CR60J226KE19	Murata	22 µ	
2	C16, C17	Ceramic, 16 V, X7R, 10%	SMD 0603		Standard	100 n	
1	C18	Ceramic, 25 V, X7R, 10%	SMD 0603	GRM188R71E333KA01	Murata	33 n	
3	C19, C20, C21	Ceramic, 16 V, X7R, 10%	SMD 0603		Standard	22 n	
2	C22, C24	Ceramic, 50 V, C0G, 5%	SMD 0603		Standard	330 pF	
1	C23	Ceramic, 50 V, C0G, 5%	SMD 0603		Standard	470 pF	
4	C25, C26, C27, C28	Ceramic, 50 V, C0G, 5%	SMD 0603		Standard	100 pF	
3	C29, C30, C31	Ceramic, 50 V, C0G, 5%	SMD 0603				n.m.
3	C32, C33, C34	Ceramic, 50 V, C0G, 5%	SMD 0603				n.m.
2	R1, R2	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	3R3	
1	R3	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	100 kΩ	
9	R4, R13 R17, R18, R19, R20, R21, R22, R23	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	68 kΩ	
1	R16	Chip resistor, 0.1 W, 1%	SMD 0603				n.m.
1	R5	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	150 kΩ	

Table 1. PM6641 demonstration board list of components (continued)

Qty	Component	Description	Package	Part number	MFR	Value	Note
2	R6, R8	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	120 kΩ	
1	R7	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	100 kΩ	
1	R9	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	56 kΩ	
1	R10	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	180 kΩ	
1	R11	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	100 kΩ	
1	R12	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	47 kΩ	
3	R32, R33, R34	Chip resistor, 0.1 W, 1%	SMD 0603		Standard	0 Ω	short
2	R30, R31	Chip resistor, 0.1 W, 1%	SMD 0603				n.m.
2	L1, L3	SMT 11Arms, 9.5 mΩ	SMD 2827	744312100 /LF	Würth	1.0 µH	
1	L2	SMT 9 Arms, 10.5 mΩ	SMD 2827	744312150 /LF	Würth	1.5 µH	
1	U1	IC VR - 48-pin	VFQFPN 7x7	PM6641	STMicroelectronics		
5	JP1, JP3, JP4, JP5, JP6	Header, 3-pin	SIP3				
2	JP7, JP8	Header, 2-pin	SIP2				
5	TP1, TP2, TP3, TP4, TP18	Header, single pin					
13	TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17	Test point					
1	SW1	Switch 4-SPST	DIP-8		Standard		

4 Component assembly and layout

Figure 3. Top side component placement

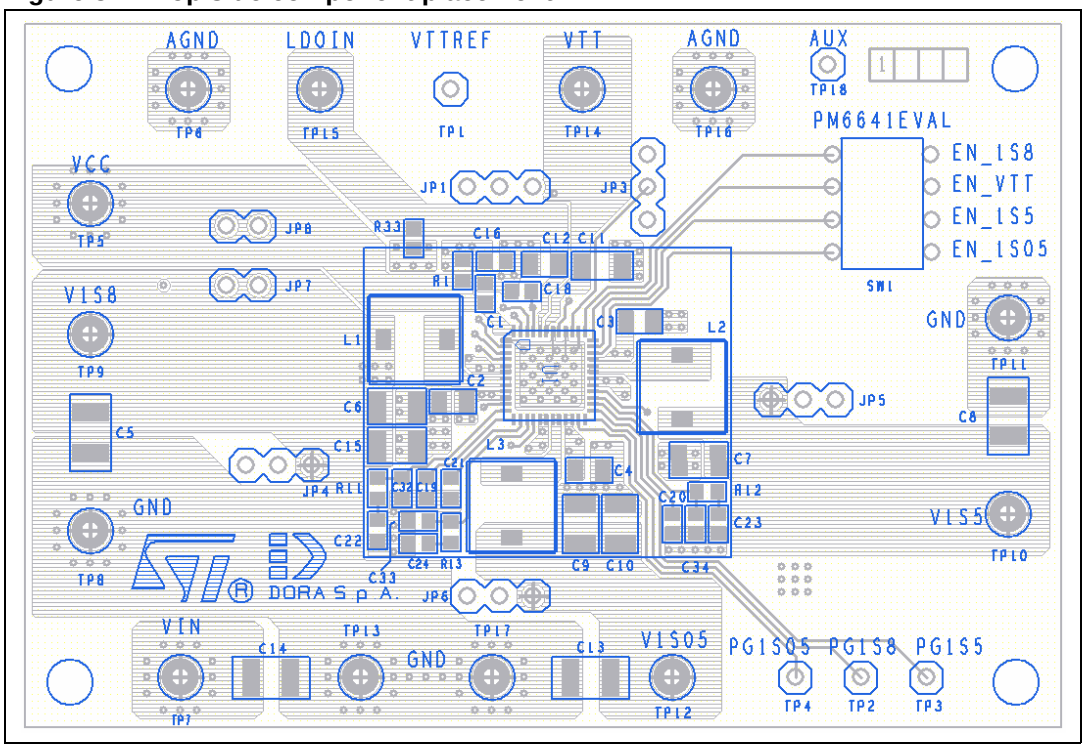


Figure 4. Top view

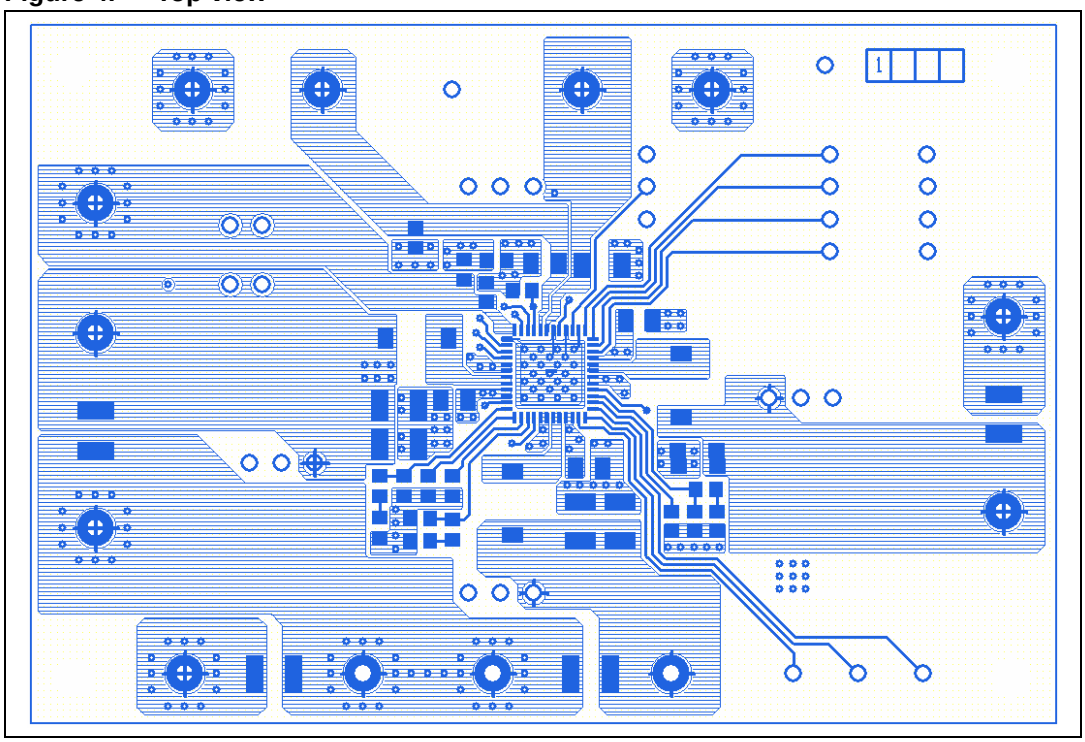


Figure 5. Layer 2 view

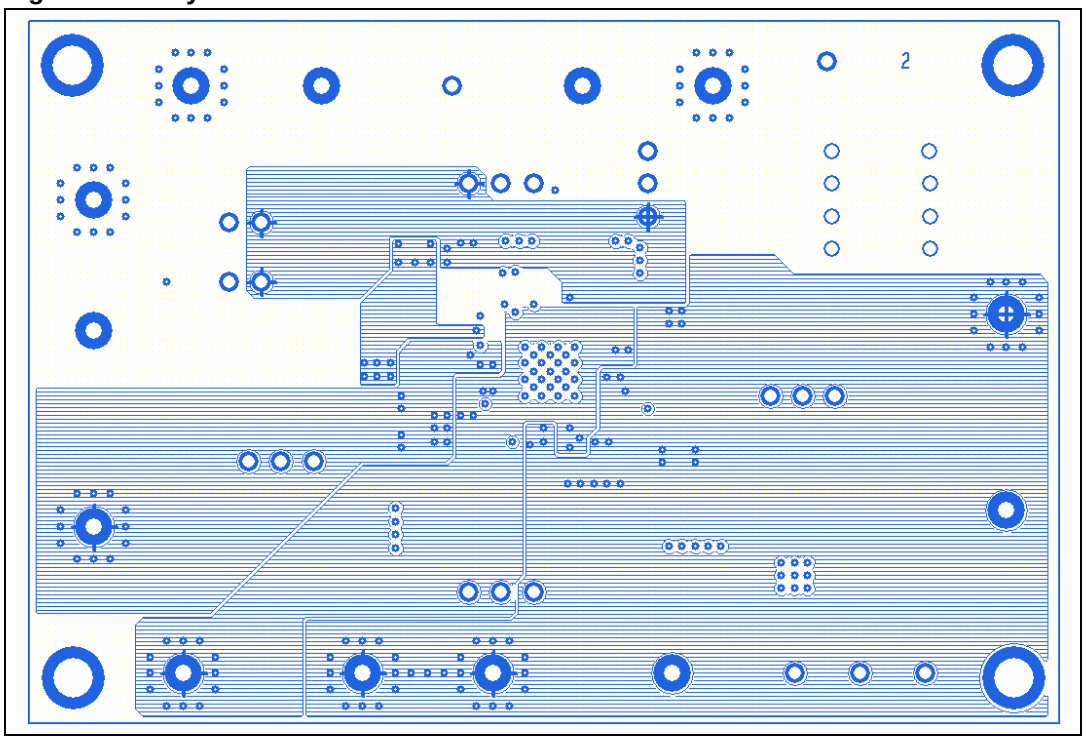


Figure 6. Layer 3 view

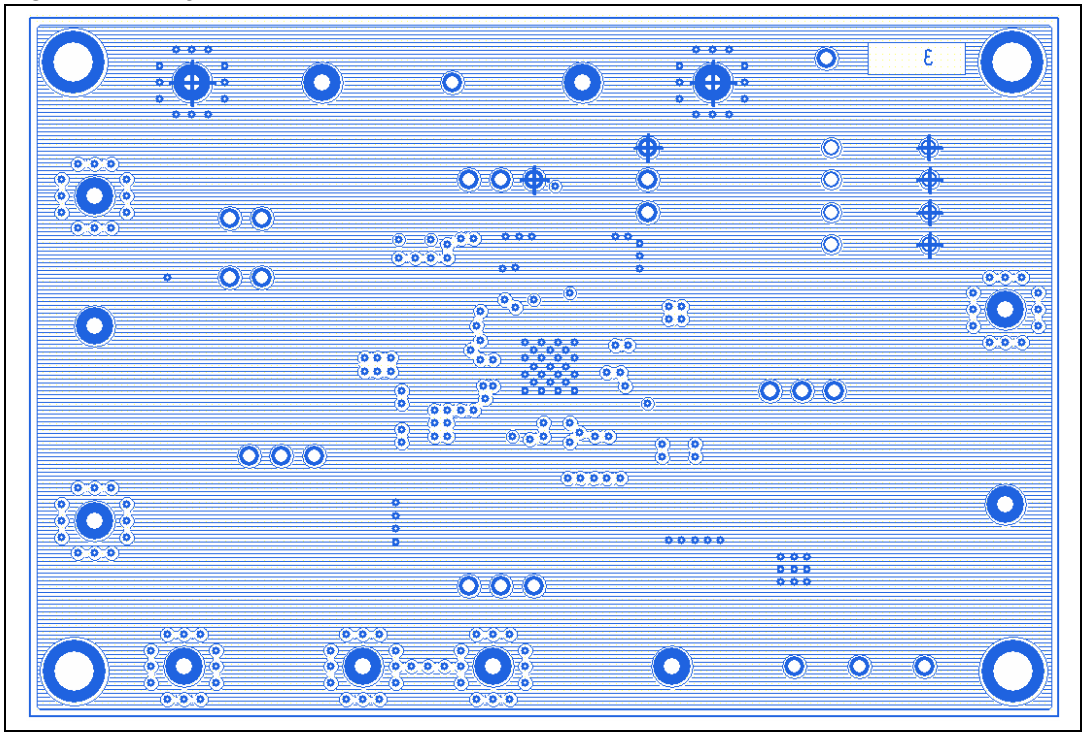


Figure 7. Bottom view

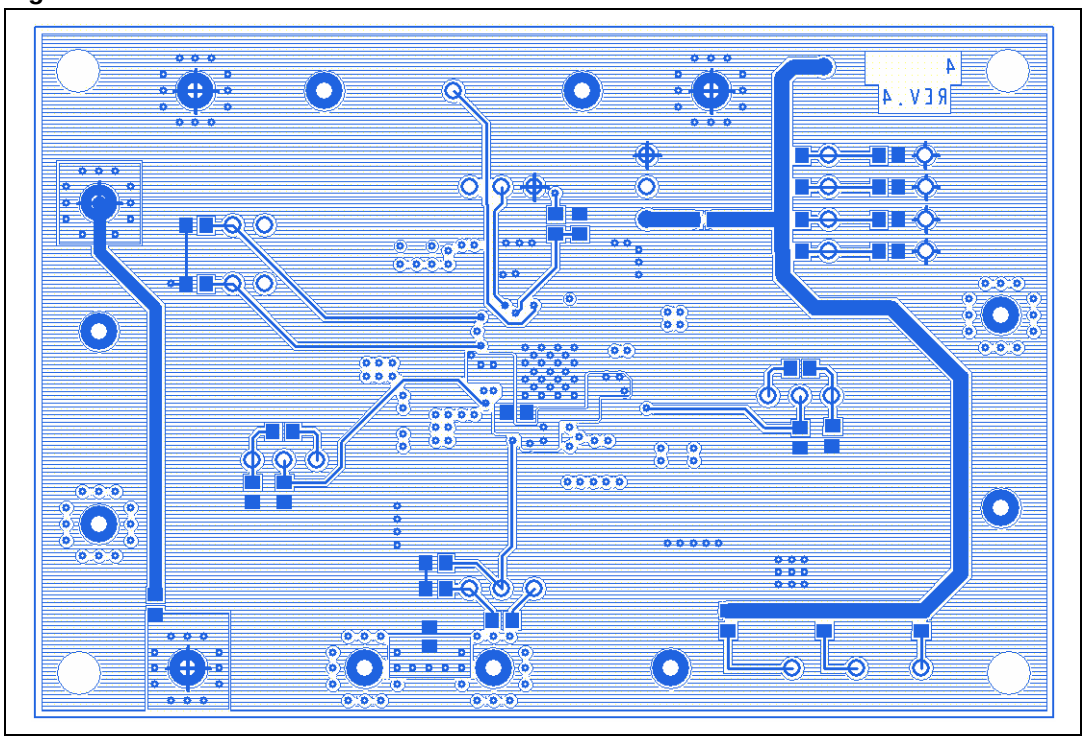
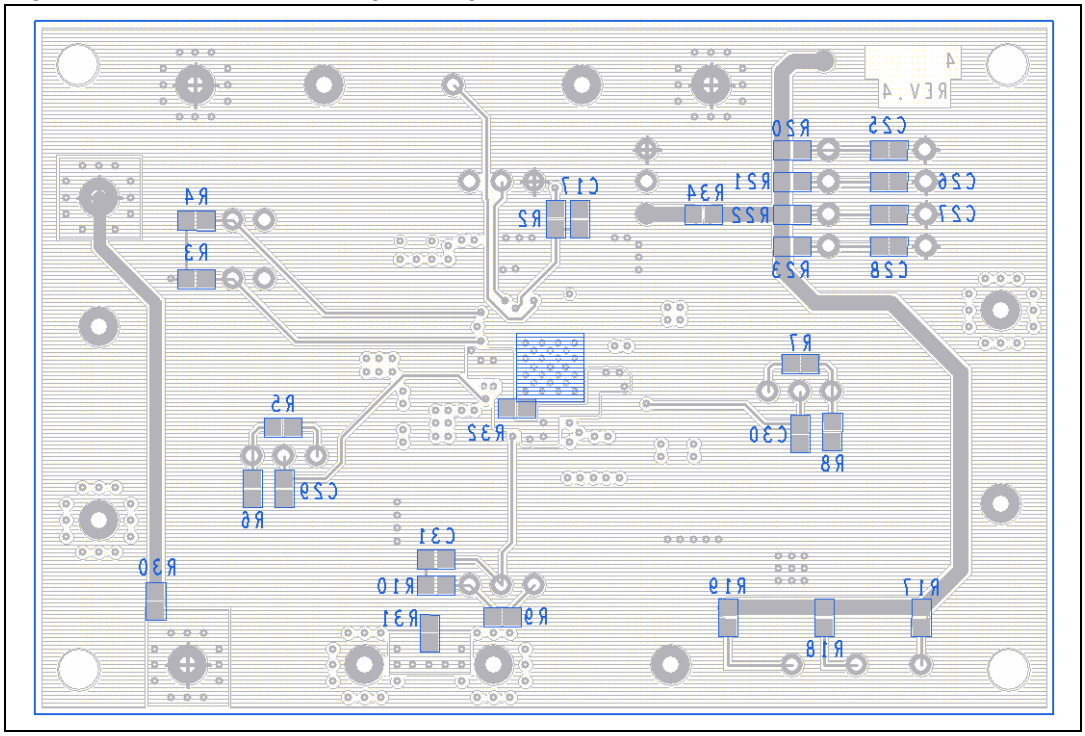


Figure 8. Bottom side component placement



5 I/O interface

The PM6641 demonstration board has the following test points given in *Table 2*.

Table 2. PM6641 demonstration board input/output interface

Test point	Description
VCC (TP5)	+5 V IC supply, positive terminal
LDOIN (TP15)	LDO (VTT) linear regulator input power supply
AUX (TP18)	Auxiliary 3.3 V for pull-up (not required)
AGND (TP6, TP16)	VCC, LDO, VTT and VTTREF common return
VIN (TP7)	Power supply input voltage positive terminal
GND (TP8, TP11, TP13, TP17)	Power supply and switching regulator outputs common return
V1S8 (TP9)	1.8 V (VDDQ) switching regulator output
V1S5 (TP10)	1.5 V switching regulator output
V1S05 (TP12)	1.05 V switching regulator output
VTT (TP14)	LDO (VTT) linear regulator output
VTTREF (TP1)	Voltage reference (VTTREF) buffer output
PG1S8 (TP2)	1.8 V (VDDQ) switching regulator Power Good signal
PG1S5 (TP3)	1.5 V switching regulator Power Good signal
PG1S05 (TP4)	1.05 V switching regulator Power Good signal

6 Recommended equipment

- 5 V power supply
- 3.3 V, 20 W power supply
- Active loads
- Digital multimeters
- 500 MHz four-trace oscilloscope

7 Configuration

The PM6641 demonstration board allows the user to test all the main features of the VR PM6641, acting on 7 different jumpers and 4 switches. SW1 (4 SPST switches) lets the user enable the switching regulators and the VTT linear regulator.

In the following sections each jumper is analyzed.

7.1 JP1 VDDQ output discharge (DSCG pin)

The JP1 jumper is used to choose between the tracking discharge or nontracking discharge of the 1.8 V rail (VDDQ) output.

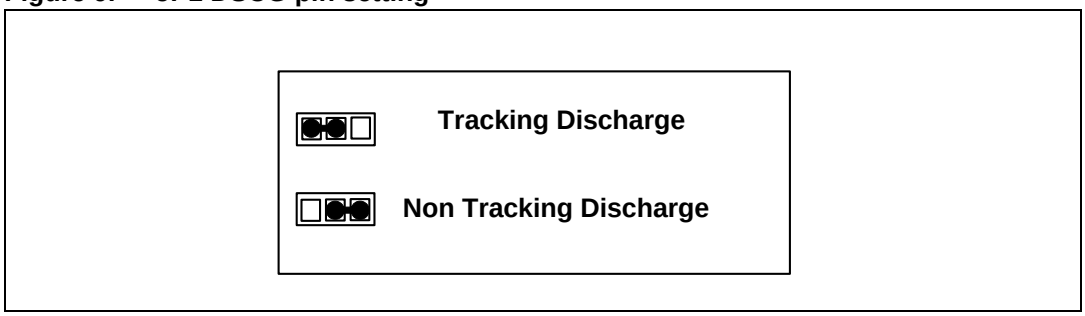
When the 1.8 V rail is deactivated (EN_1S8 goes low) and the DSCG is set high, tracking discharge takes place:

- The 1.8 V rail regulator is discharged by the internal MOSFETs
- The 0.9 V LDO and VTTREF work tracking with half of the 1.8 V rail

When the 0.9 V LDO and VTTREF reach a voltage threshold of about 300 mV, the nontracking discharge mode is performed by closing the internal discharge MOSFETs.

If the nontracking discharge mode is chosen, when EN_1S8 goes low, the 1.8 V and 0.9 V rails and the VTTREF buffer are independently discharged by internal MOSFETs.

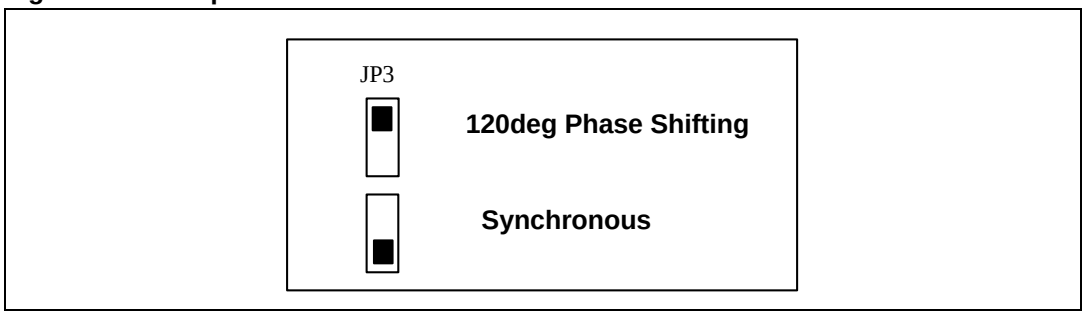
Figure 9. JP1 DSCG pin setting



7.2 JP3 switching regulator phase control (SET_PH1 pin)

The JP3 jumper allows selecting two different oscillator settings in order to change the delay between the pulses that start the control cycle. The inner clock is divided in order to obtain three slower clocks with a fixed delay of 120 deg. By setting JP3 as depicted in *Figure 10*, it is possible to synchronize the 1.8 V, 1.5 V and 1.05 V switching regulator clocks or to select 120 deg delay in order to decrease the total RMS input current.

Figure 10. JP3 phase control



The 120 deg phase shifting is the default configuration in which the inner clock is divided and three pulses delayed by 120 deg are obtained to trigger the switching regulator loops.

The synchronous clocking allows all the regulators to start at the same pulse, avoiding the jitter due to simultaneous turn-on and off of different sections, but increasing the overall RMS input current.

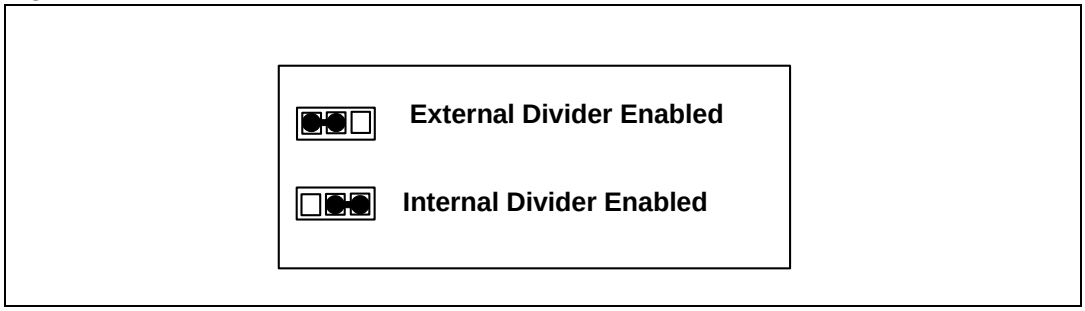
7.3 JP4 1.8 V (VDDQ) external/internal divider (VFB_1S8 pin)

The JP4 jumper allows selecting the internal divider or the external divider for the 1.8 V switching regulator. When the VFB_1S8 pin is connected directly to the output capacitor, the internal divider is enabled and this section provides 1.8 V output voltage. When the multifunction pin VFB_1S8 is tied to the central tap of an external divider, the switching regulator becomes adjustable, with the following output voltage:

Equation 1

$$Vout = \left(\frac{R_5}{R_6} + 1\right) \cdot 0.8\ V$$

Figure 11. JP4 1.8 V divider selection



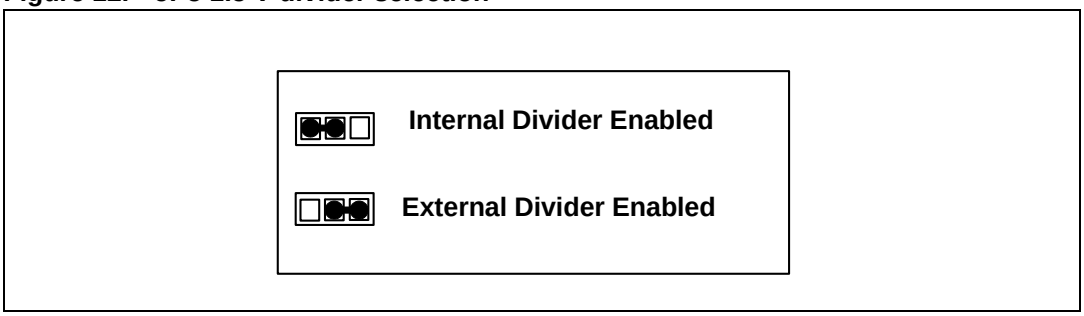
7.4 JP5 1.5 V external/internal divider (VFB_1S5 pin)

The JP5 jumper allows selecting the internal divider or the external divider for the 1.5 V switching regulator. When the VFB_1S5 pin is connected directly to the output capacitor, the internal divider is enabled and this section provides 1.5 V output voltage. When the multifunction pin VFB_1S5 is tied to the central tap of an external divider, the switching regulator becomes adjustable, with the following output voltage:

Equation 2

$$Vout = \left(\frac{R_7}{R_8} + 1\right) \cdot 0.8\ V$$

Figure 12. JP5 1.5 V divider selection



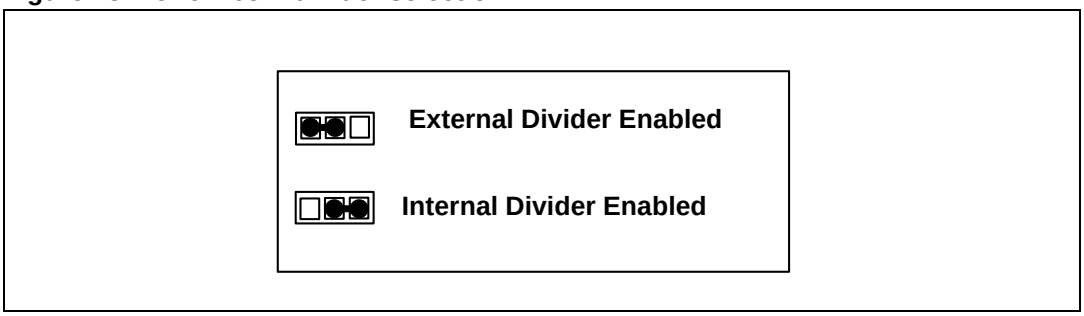
7.5 JP6 1.05 V external/internal divider (VFB_1S05 pin)

The JP6 jumper allows selecting the internal divider or the external divider for the 1.05 V switching regulator. When the VFB_1S05 pin is connected directly to the output capacitor, the internal divider is enabled and this section provides 1.05 V output voltage. When the multifunction pin VFB_1S5 is tied to the central tap of an external divider, the switching regulator becomes adjustable, with the following output voltage:

Equation 3

$$Vout = \left(\frac{R_9}{R_{10}} + 1\right) \cdot 0.8\ V$$

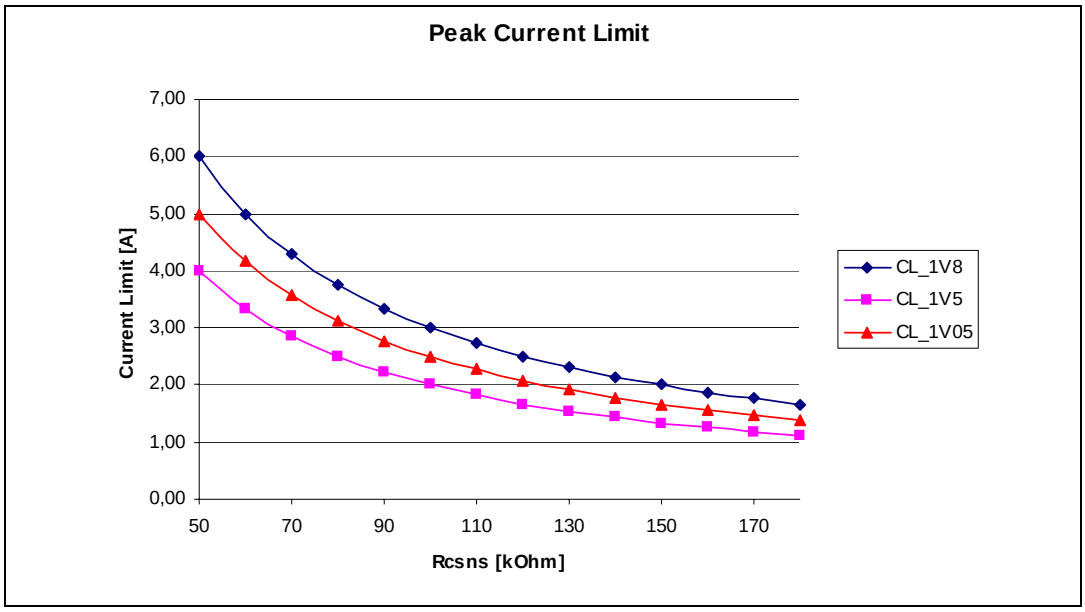
Figure 13. JP6 1.05 V divider selection



7.6 JP7 current limit (CSNS pin)

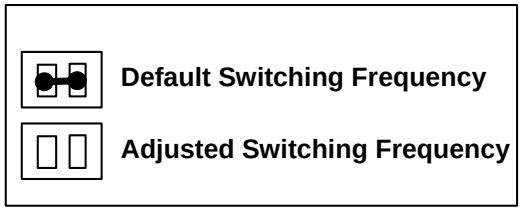
Each switching regulator current limit is set by inserting a resistor between the CSNS pin and AGND. By changing this resistor value, all the current limits change, as shown in *Figure 14*.

Figure 14. PM6641 demonstration board programmed current limit vs. CSNS resistor



If the CSNS pin is tied to AVCC, the current limit is set through the inner reference resistor (equal to 50 kΩ).

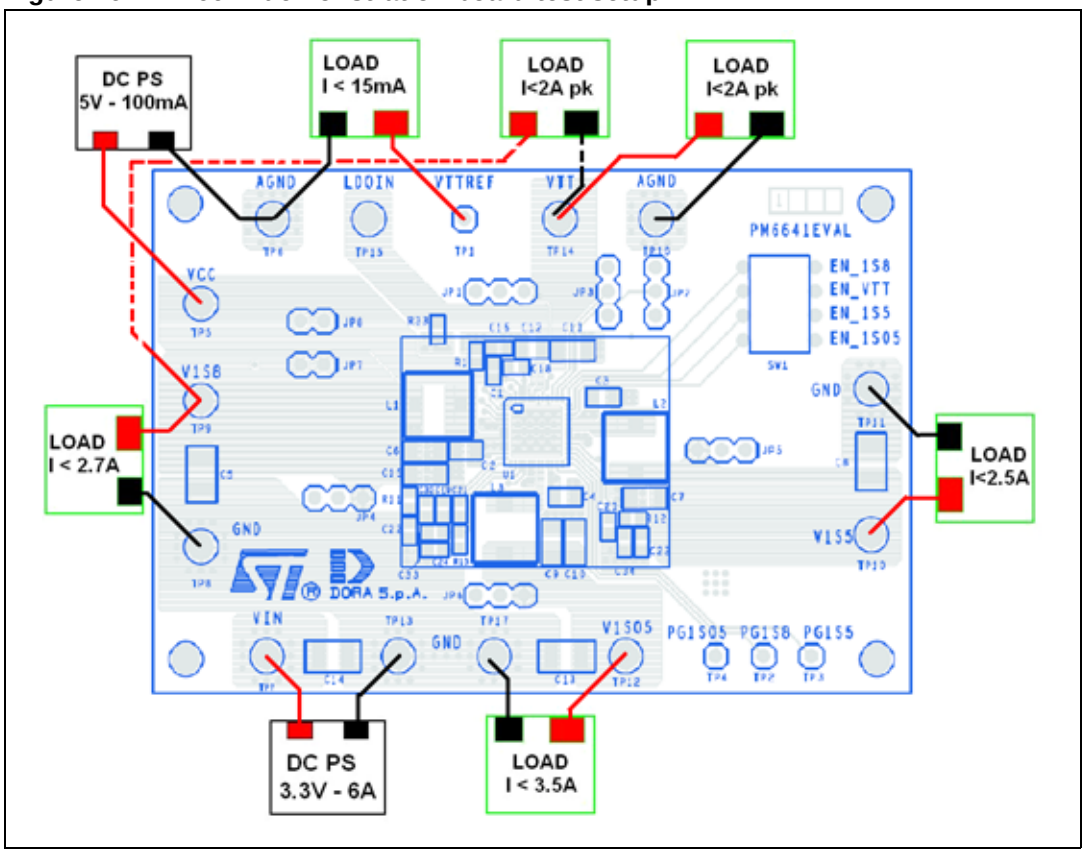
Figure 15. JP8 setting switching frequency



8 Test setup

Figure 16 shows the suggested setup connections between the PM6641 demonstration board, the loads, and the external supply.

Figure 16. PM6641 demonstration board test setup



9 Getting started

The following step-by-step power-up and power-down sequences are provided in order to correctly evaluate the PM6641 demonstration board performance.

Power-up sequence

- Connect power supplies as shown in the PM6641 demonstration board test setup (*Figure 16*) and insert the meters in order to perform the desired performance evaluation. Connect the scope-probes as desired
- Set the JP1 through JP8 jumpers in order to properly configure the PM6641 demonstration board. Set the SW1 switches (EN_1S8, EN_VTT, EN_1S5, EN_1S05) to the ON position. Do not change jumper settings when the board is powered
- Set the VCC supply to 5 V ±5% and the current limit to 100 mA
- Set the VIN supply to a voltage in the range 2.7 V to 3.6 V
- Set all active loads to 0 A
- Turn-on the VIN supply
- Turn-on the VCC supply
- Vary the 1.8 V (VDDQ) load from 0 A to 4 A
- Vary the 1.5 V load from 0A to 2.5 A
- Vary the 1.05 V load from 0A to 3.5 A
- Vary the 0.9 V (VTT) load from 0 A to 2 A to test source capability. To test sink capability use the alternative VTT load connection shown in *Figure 16*
- Vary VTTREF load to test source capabilty.

Power-down sequence

- Decrease VTTREF and VTT loads to 0 A
- Turn-off the 1.8 V (VDDQ), 1.5 V, 1.05 V loads
- Decrease VCC supply from 5 V to 3.8 V in order to test the input undervoltage lockout (UVLO)
- Increase VCC supply from 3.8 V to 5 V to restart the device
- Use the EN_1S8 and En_VTT switches to enter/exit the S0-S3-S5 states
- Turn-off the VCC supply
- Turn-off the VIN supply.

10 STEVAL-ISA050V1 evaluation tests

10.1 SW regulators turn-on (soft-start)

When the EN_xx pin is toggled high, the correspondent SW regulator performs the soft-start as programmed through the external soft-start capacitor. *Figure 17* depicts VDDQ (1.8 V) turn-on with C_{SS} = 22 nF.

Figure 17. VDDQ turn-on

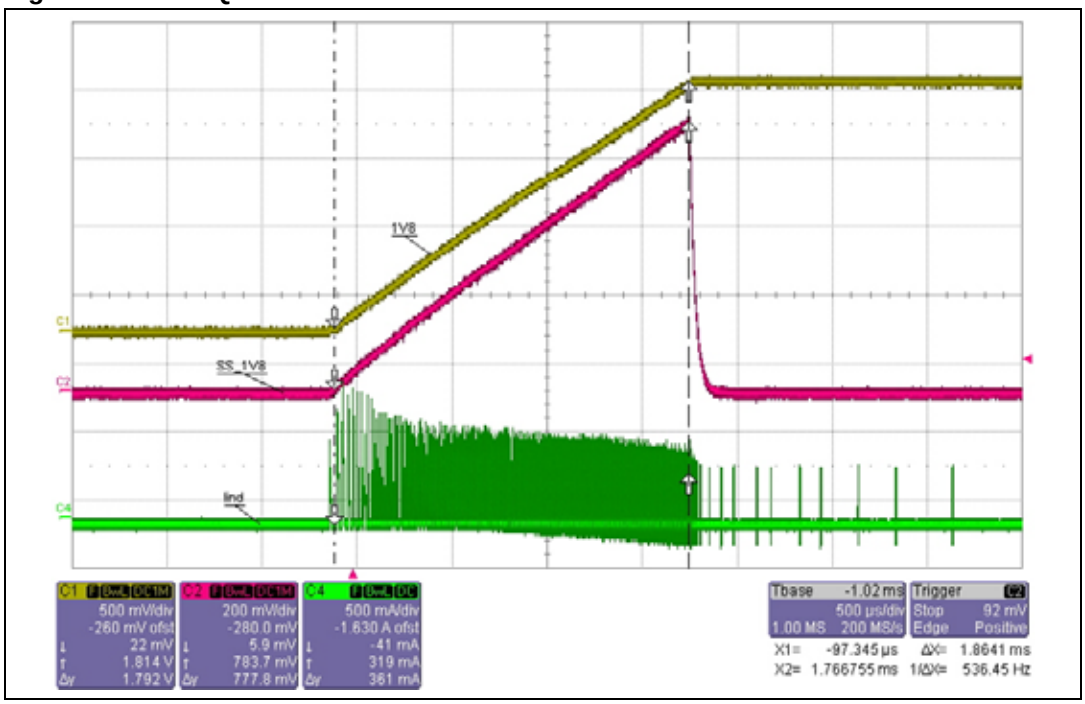
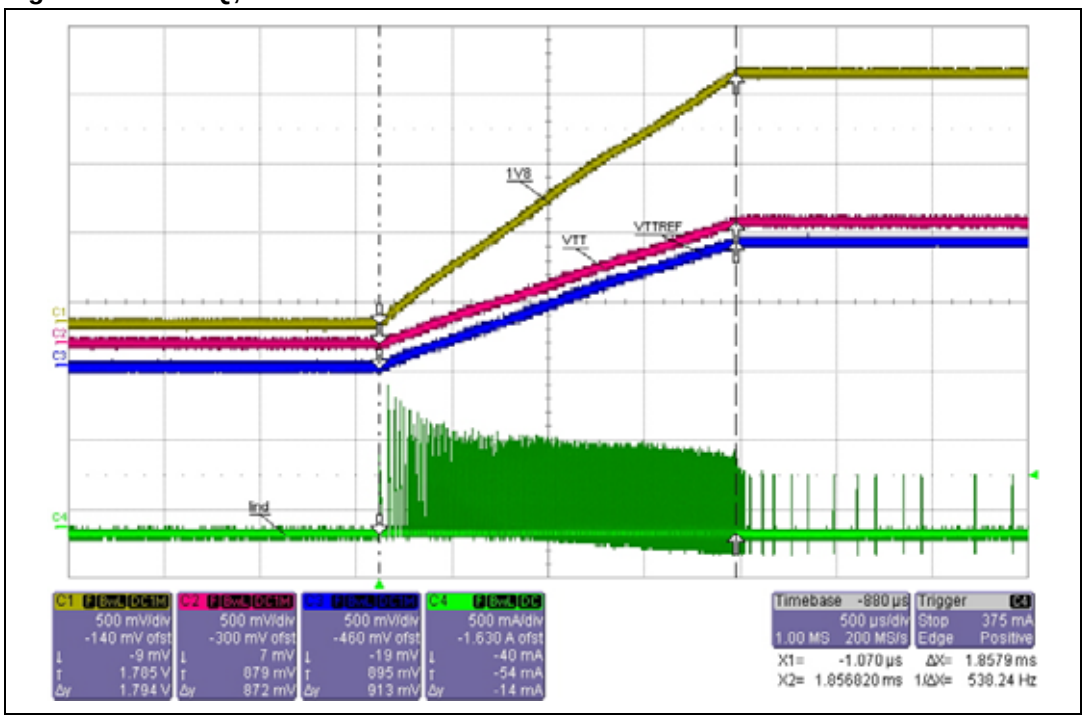


Figure 18. VDDQ, VTT and VTTREF turn-on



10.2 SW regulator - working mode

Each switching regulator changes working mode with the appropriate load. When the load is heavy, the SW enters PWM mode, but when the load is light, pulse skip mode is entered. Each SW regulator is also able to sink current from the output (forced PWM mode when a soft overvoltage occurs).

Figure 19. PWM mode: VDDQ output voltage, phase voltage and inductor current, current load = 2.3 A

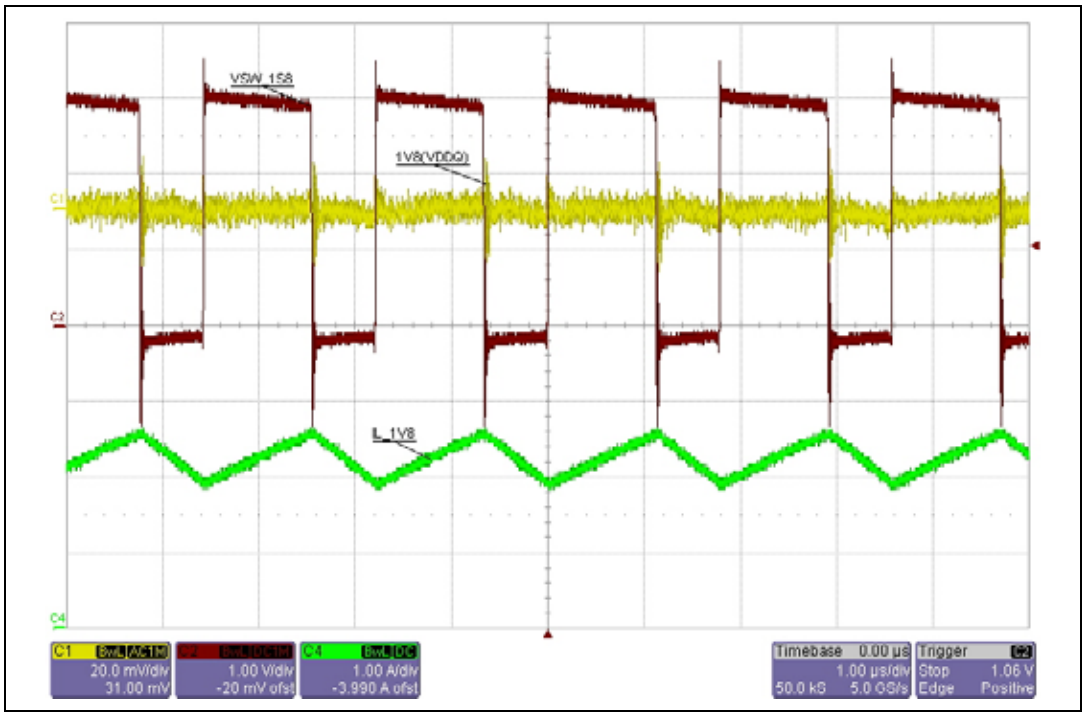


Figure 20. Pulse skip mode: VDDQ output voltage, phase voltage and inductor current, current load = 0 A

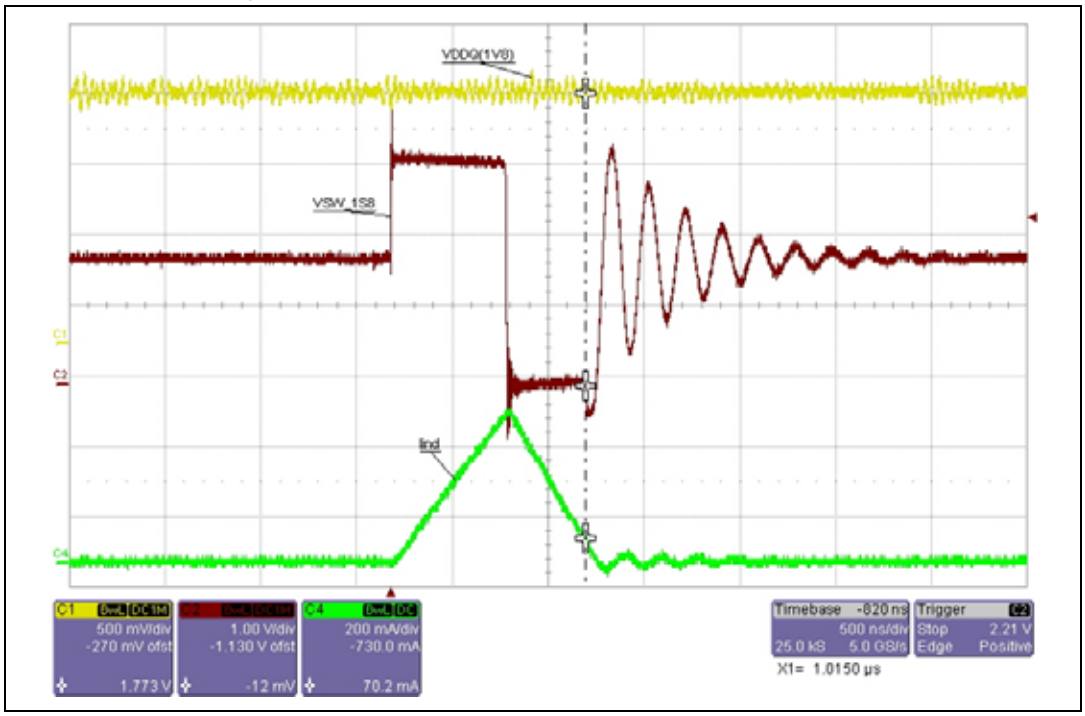
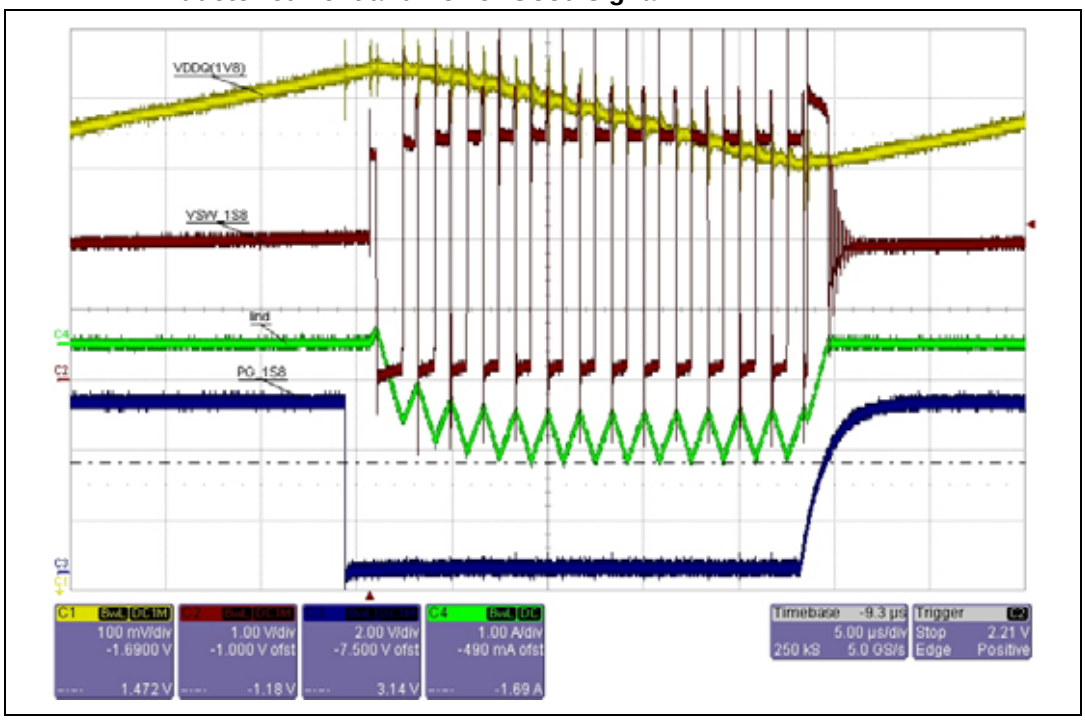


Figure 21. Forced PWM mode (soft OV): VDDQ output voltage, phase voltage, inductor current and Power Good signal



10.3 Load regulation

Figure 22. VDDQ (1.8 V) load regulation

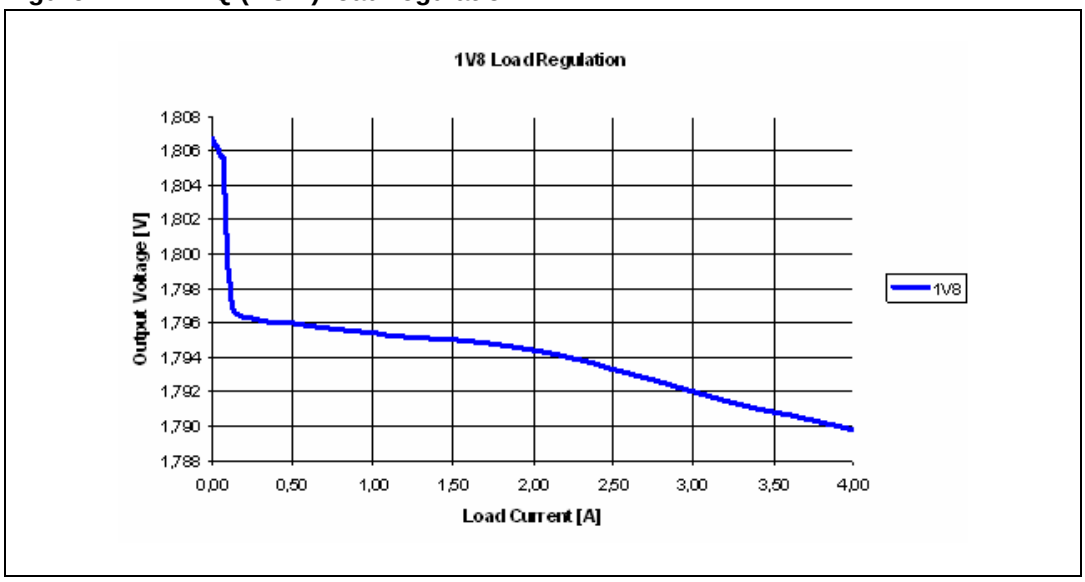


Figure 23. 1.5 V load regulation

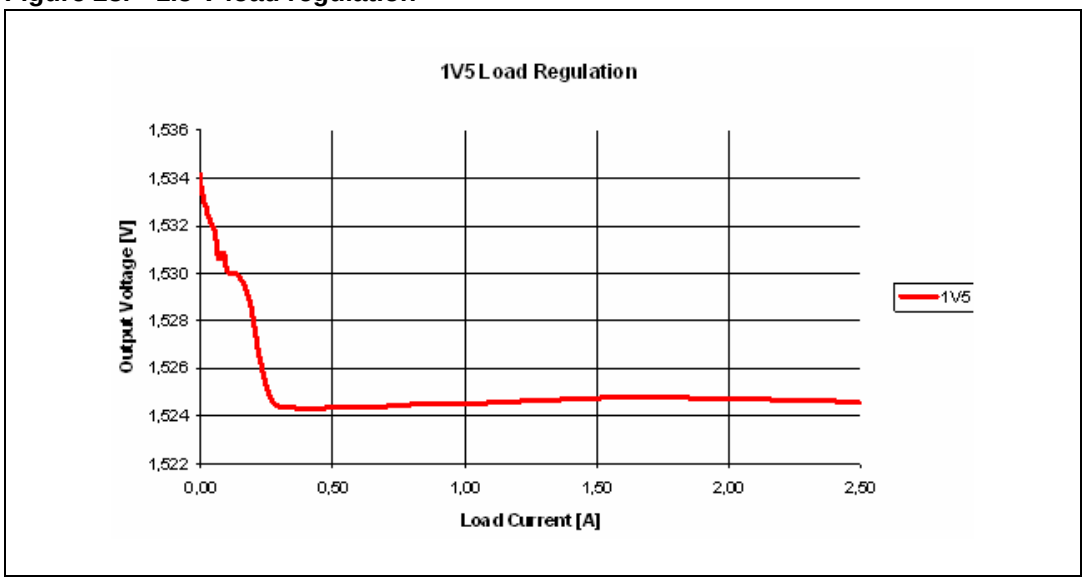


Figure 24. 1.05 V load regulation

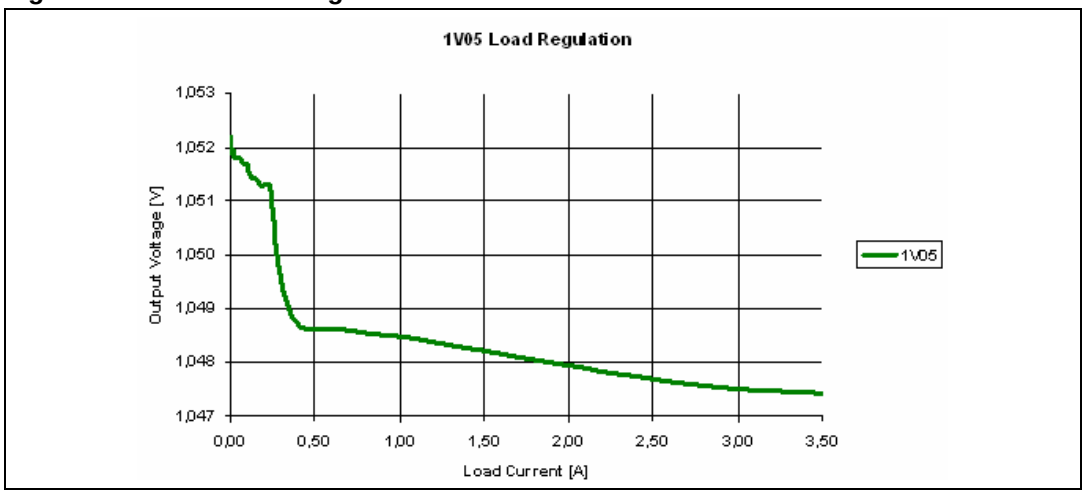


Figure 25. VTT load regulation

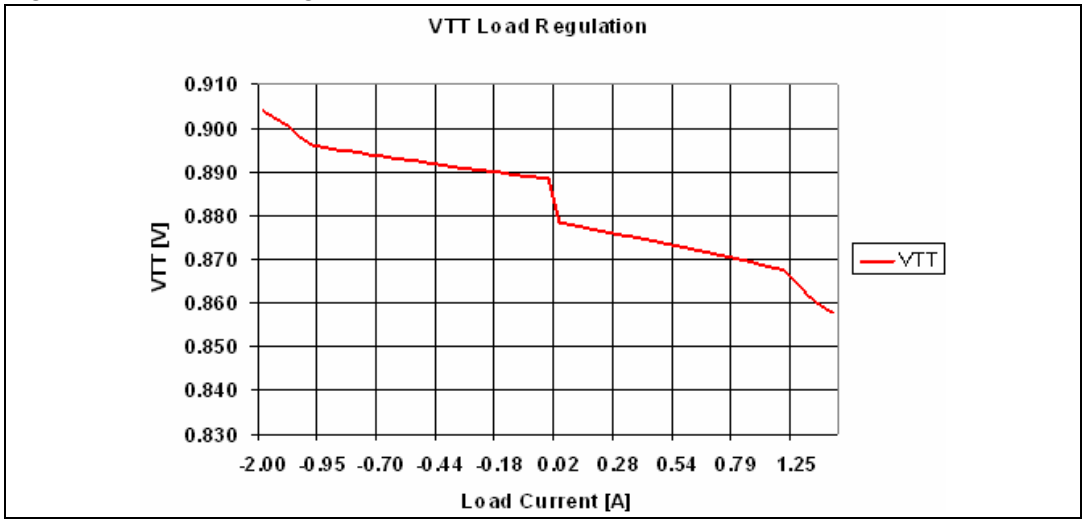
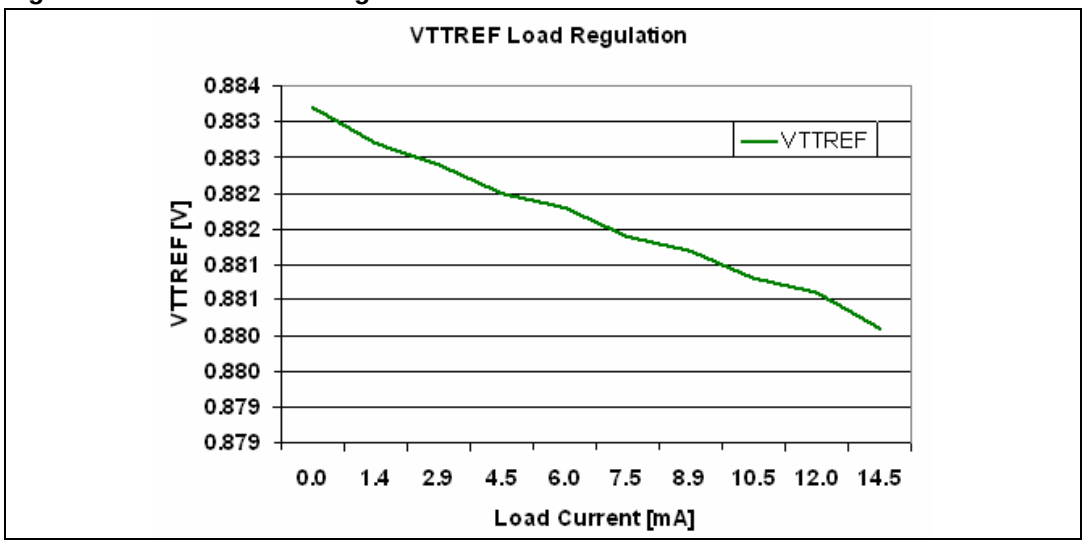


Figure 26. VTTREF load regulation



10.4 Load transient responses

Figure 27. VDDQ, VTT and VTTREF, VDDQ load transient response, IVDDQ = 0 to 2.3 A at 2.5 A/µs

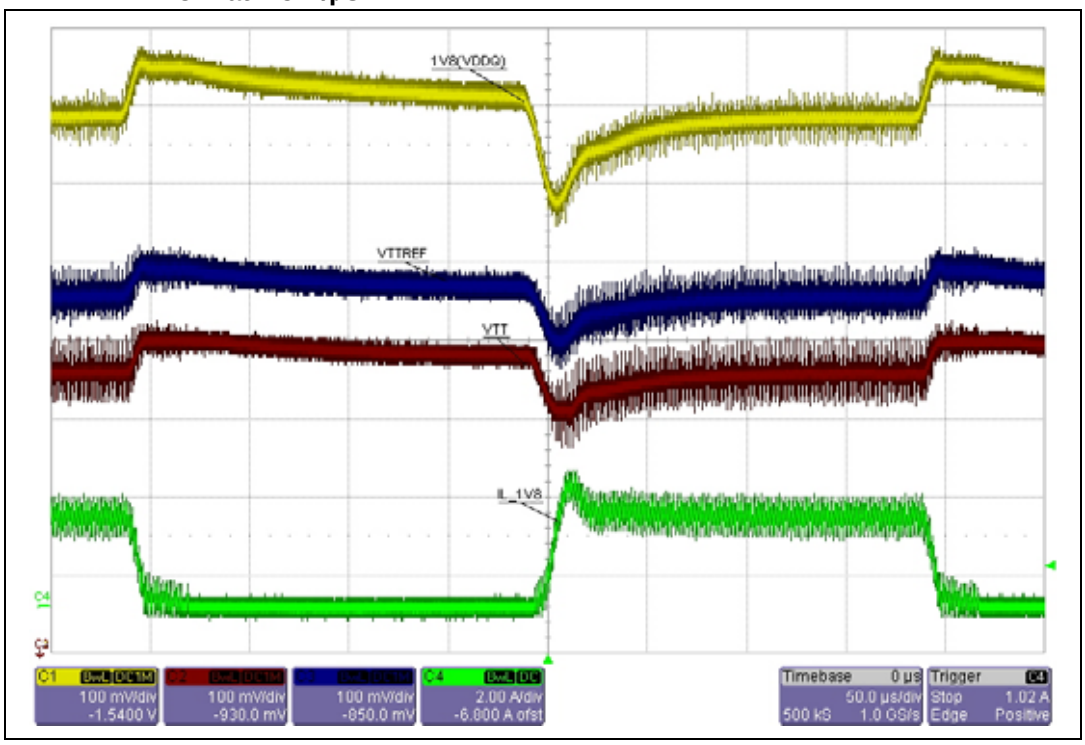


Figure 28. 1.5 V output voltage and inductor current, 1.5 V rail load transient response, 1.5 V = 0 to 1.25 A at 2.5 A/µs

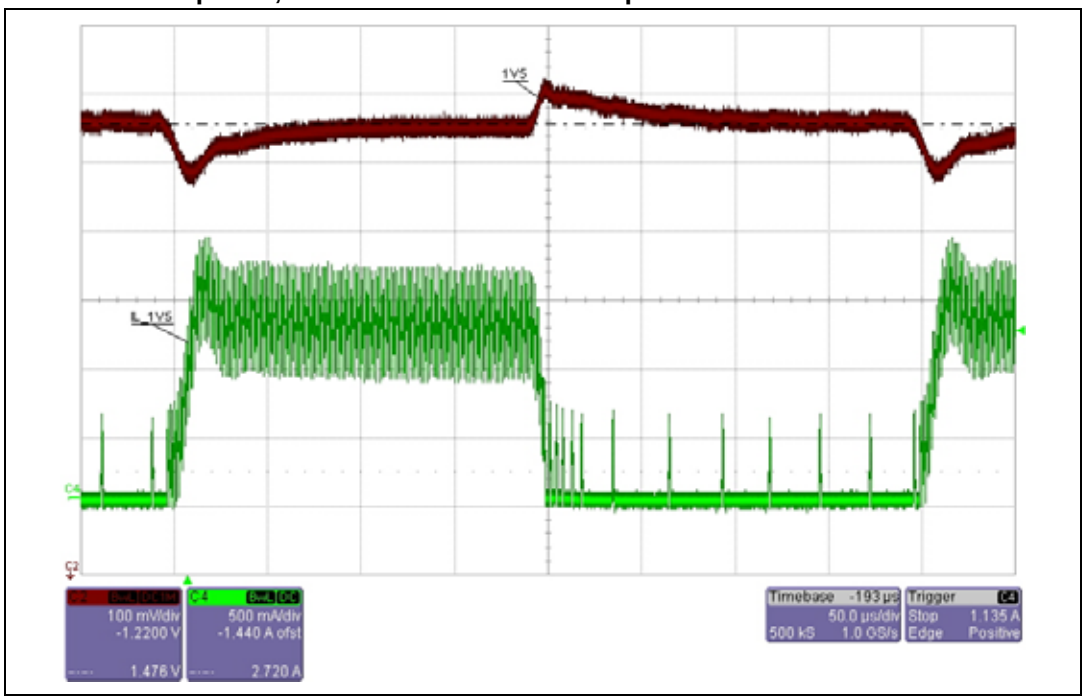


Figure 29. 1.05 V output voltage and inductor current, 1.05 V rail load transient response. $I_{1.05\ V}$ = 0 to 1.75 A at 2.5 A/µs

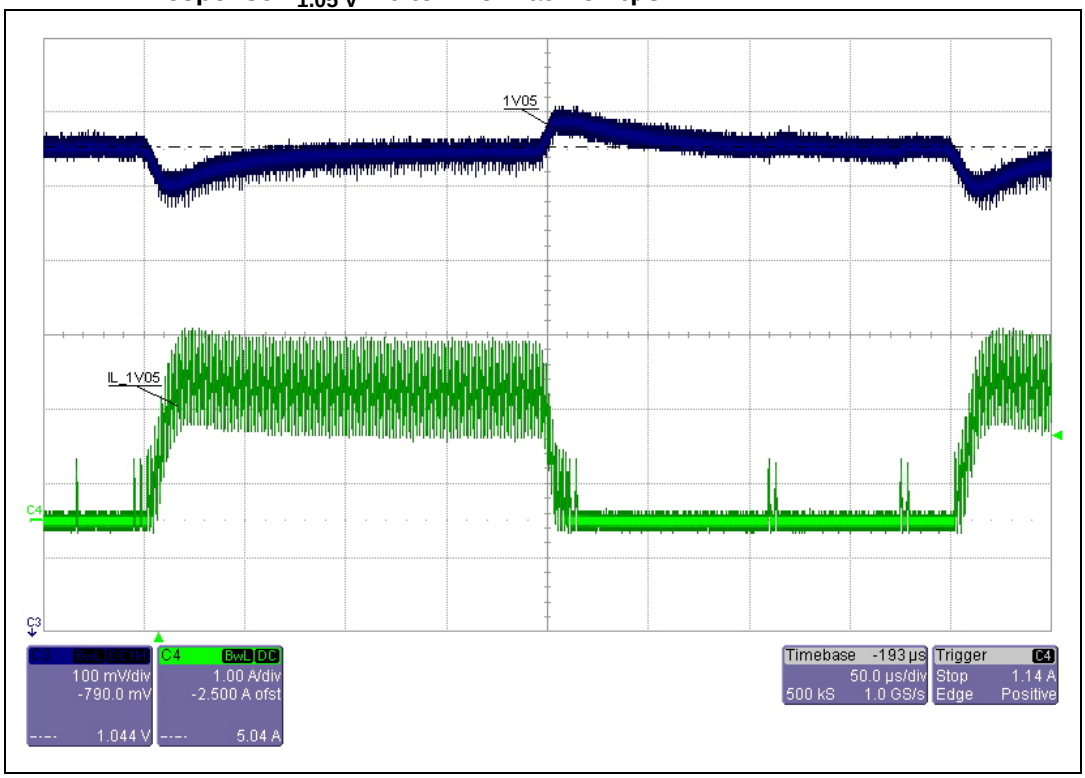
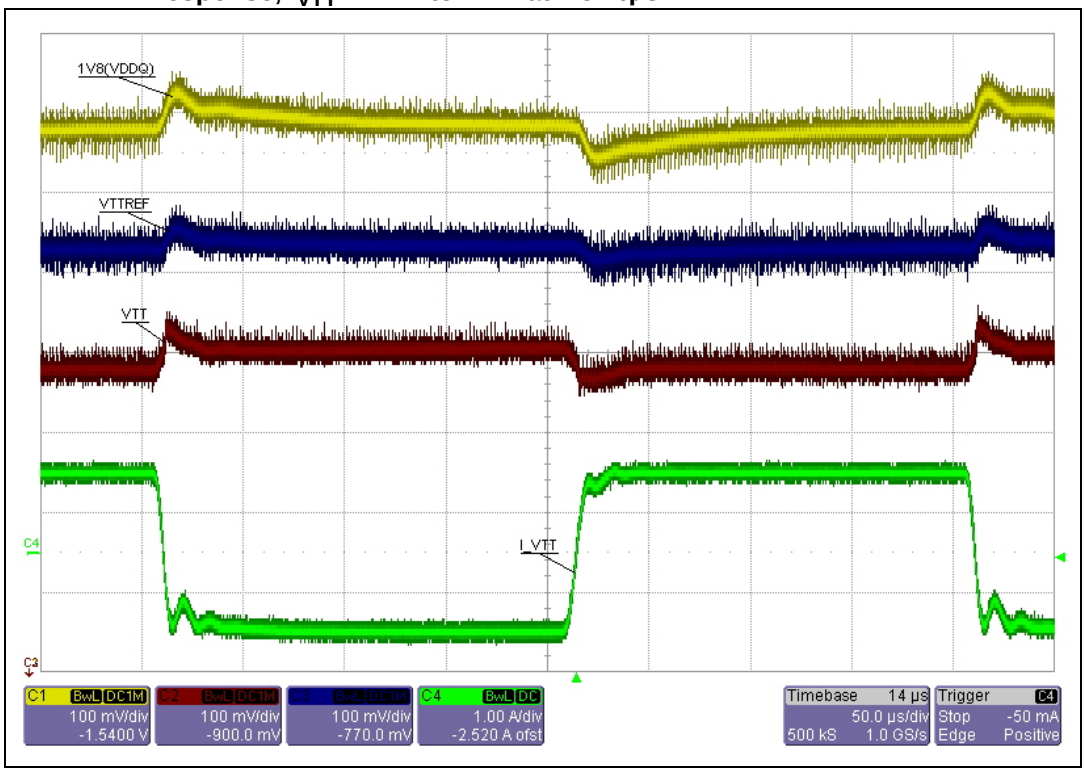
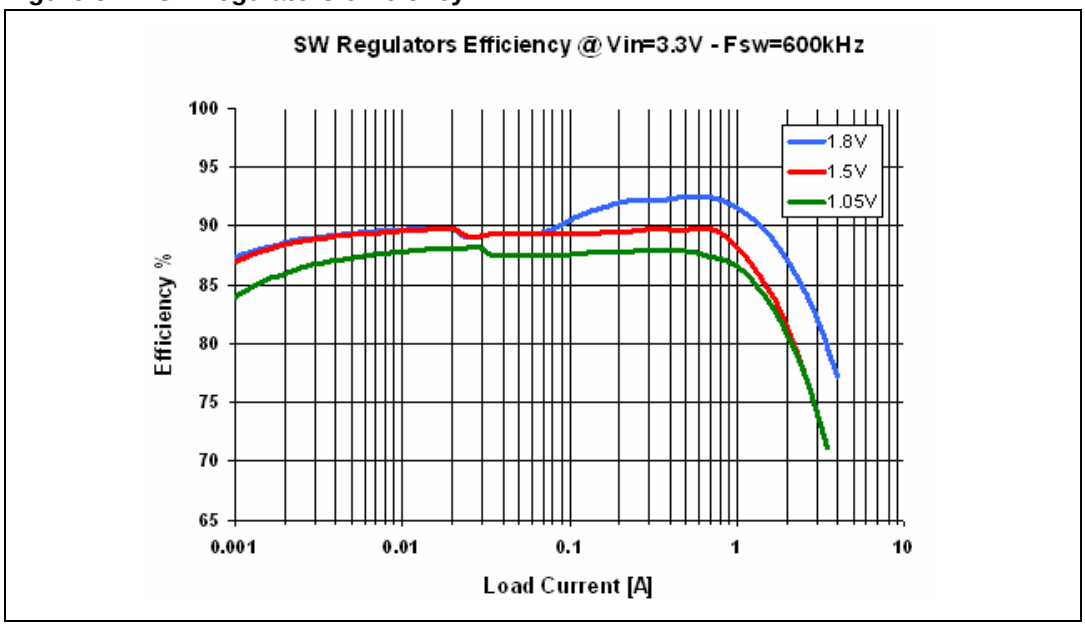


Figure 30. VDDQ, VTTREF, VTT and VTT output current, VTT rail load transient response, I_{VTT} = –1 A to +1 A at 2.5 A/µs



10.5 Efficiency

Figure 31. SW regulators efficiency



10.6 Phase management

Figure 32 and *33* show the SW regulators loaded with 1.3 A (VDDQ rail), 1.25 A (1.5 V rail) and 1.75 A (1.05 V rail). By connecting the SETPH1 pin to AGND or to AVCC the following two different phase shifts are allowed.

Figure 32. SW regulators phases, 120 deg phase shift. SETPH1 pin tied to AGND

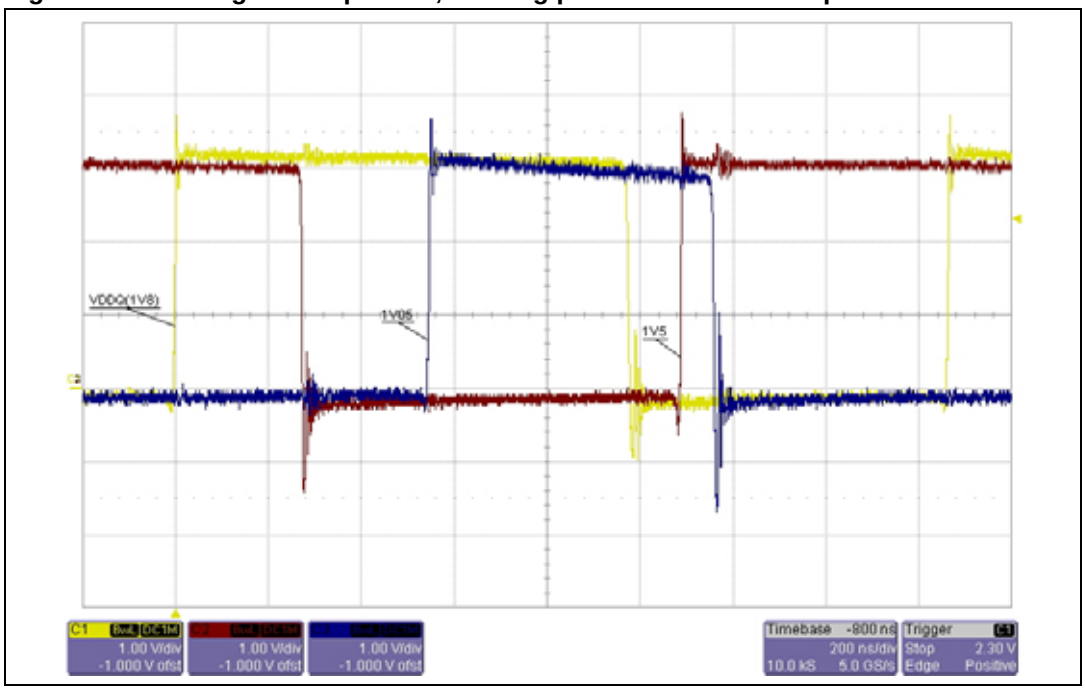
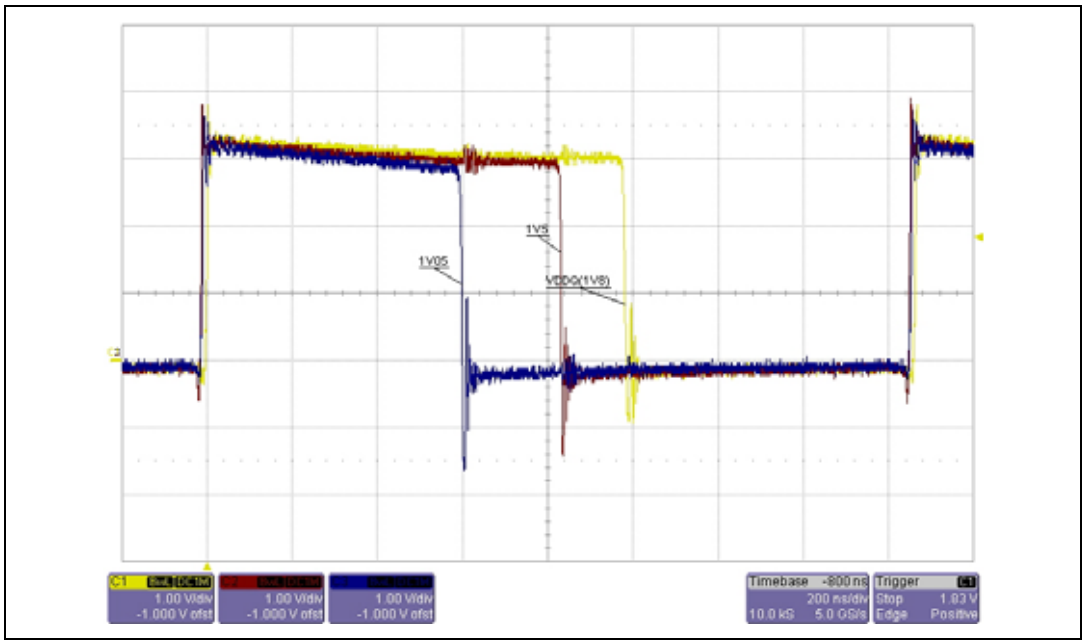


Figure 33. SW regulators phases, no phase shift - synchronous clock, SETPH1 pin tied to AVCC



10.7 Fault management (OVP, UVP, UVLO, thermal)

Each switching regulator is able to detect the output overvoltage and undervoltage. When the OV is detected the high-side MOSFET is turned off and the low-side MOSFET is turned on. When the UV is detected, the power MOSFETs are both turned off and the discharge MOSFET is turned on (soft-end). The soft-end is also performed when the junction temperature is higher than 150 °C.

Figure 34. VDDQ, VTT, VTTREF output voltage, VDDQ temporarily shorted to 3.3 V, output overvoltage protection triggered

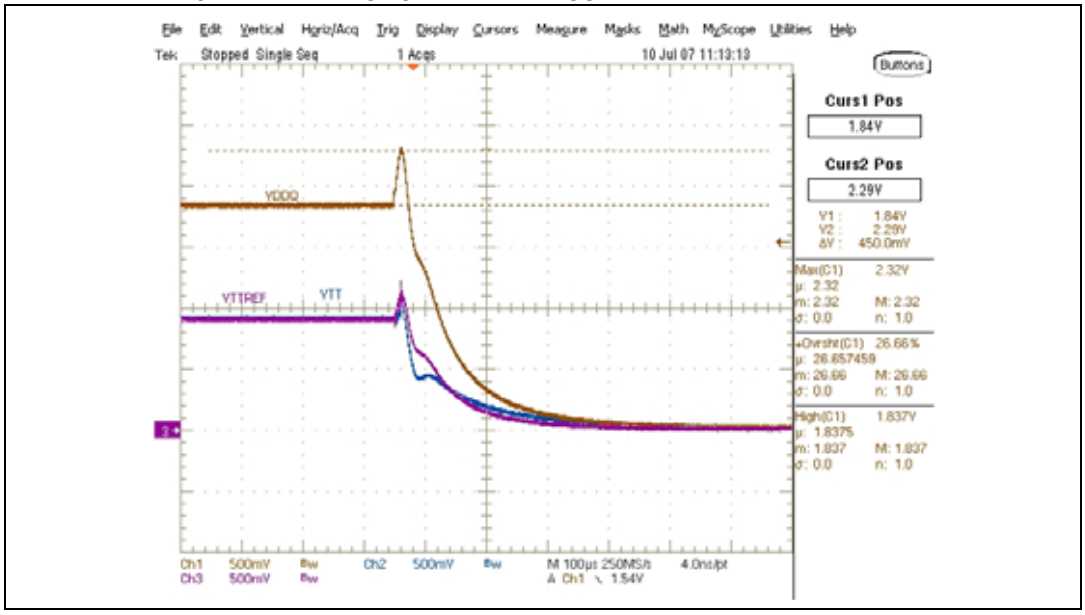
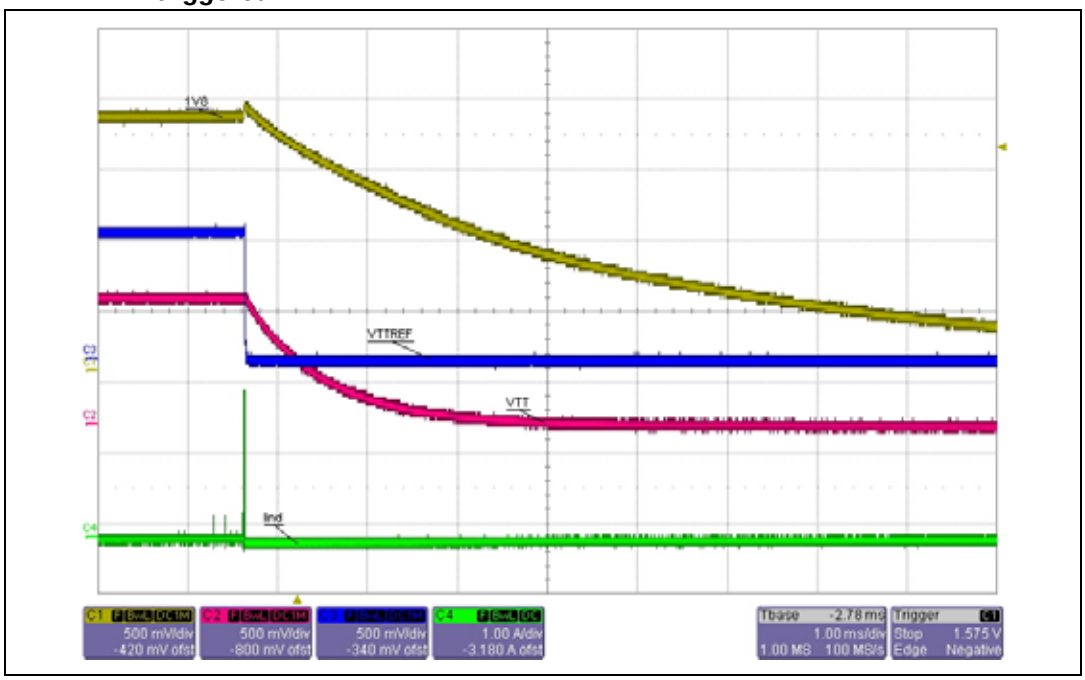


Figure 35. VDDQ, VTT, VTTREF output voltage and VDDQ inductor current, VDDQ feedback pin temporarily shorted to GND, output undervoltage protection triggered



When the input undervoltage is detected, the VDDQ (1.8 V) rail performs the output voltage soft-end. The 1.5 V and 1.05 V rails turn-off the high-side power MOSFET and turn-on the low-side one.

Figure 36. VDDQ (1.8 V), 1.5 V, 1.05 V output voltage and AVCC input power supply, input undervoltage lockout triggered

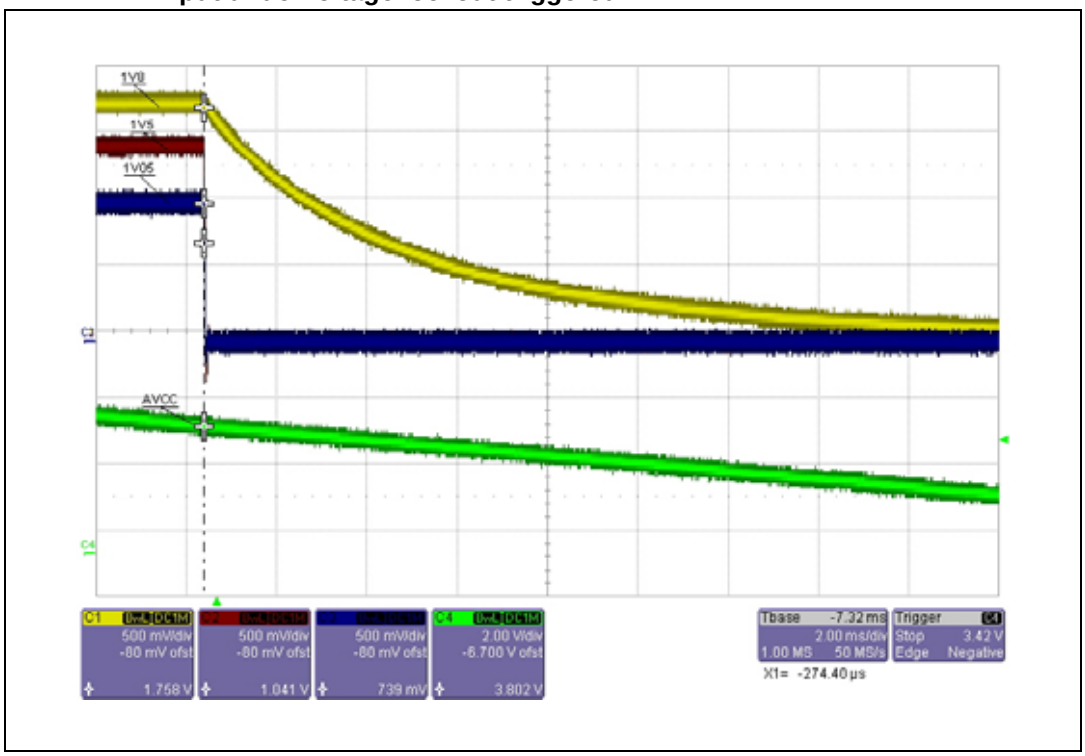
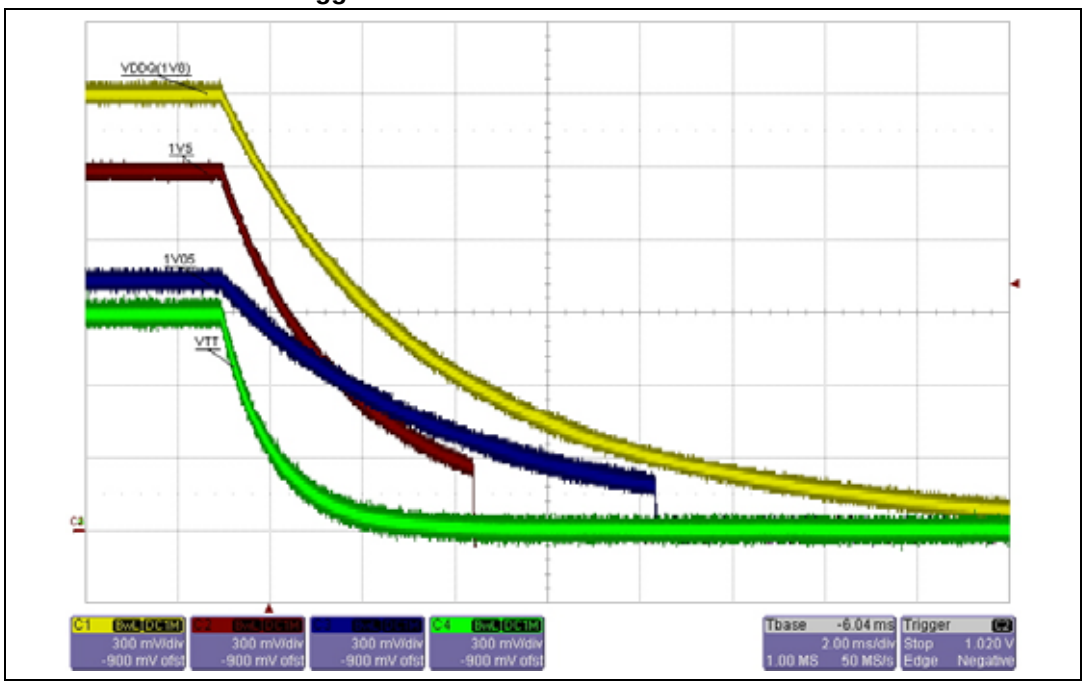


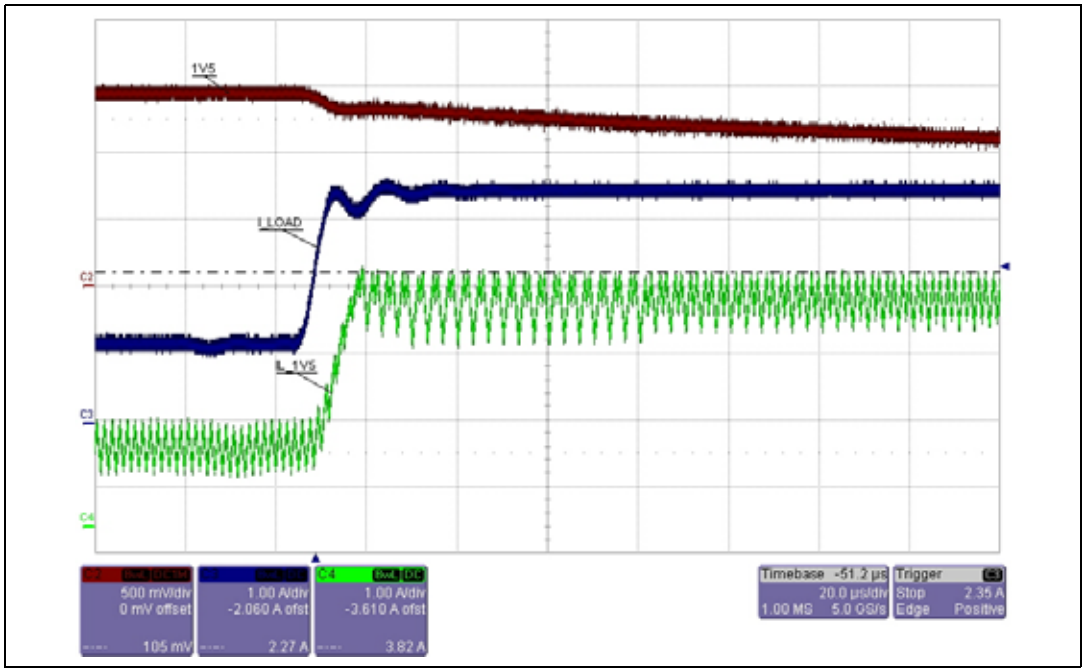
Figure 37. VDDQ (1.8 V), 1.5 V, 1.05 V and VTT rails output voltage, thermal shutdown triggered



10.8 SW regulators current limit

Cycle-by-cycle the high-side MOSFET current is monitored and if it's higher than the programmed current limit, the high-side MOSFET is immediately turned off.

Figure 38. 1.5 V rail output voltage, 1.5 V inductor current and output current, peak current limit reached



10.9 Soft-end

Each SW regulator, when turned off, performs the output voltage soft-end by turning off the power MOSFET and turning on the discharge MOSFET. When the output voltage is lower than about 300 mV, the low-side power MOSFET is turned on. VTTREF and VTT can track half of VDDQ also during the soft off.

These rails are allowed two different modes of discharge: tracking and nontracking discharge.

Figure 39. VDDQ(1.8 V), VTT and VTTREF rail output voltage, EN_1S8 and EN_VTT tied to AGND - soft off with tracking discharge

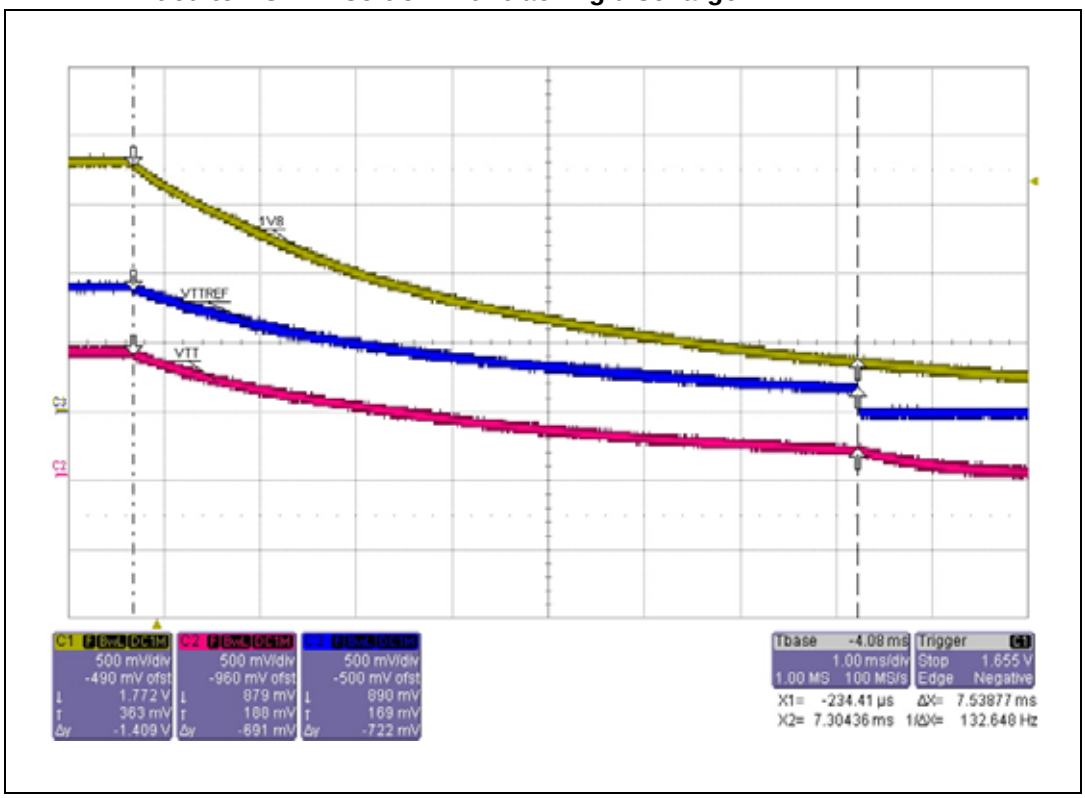
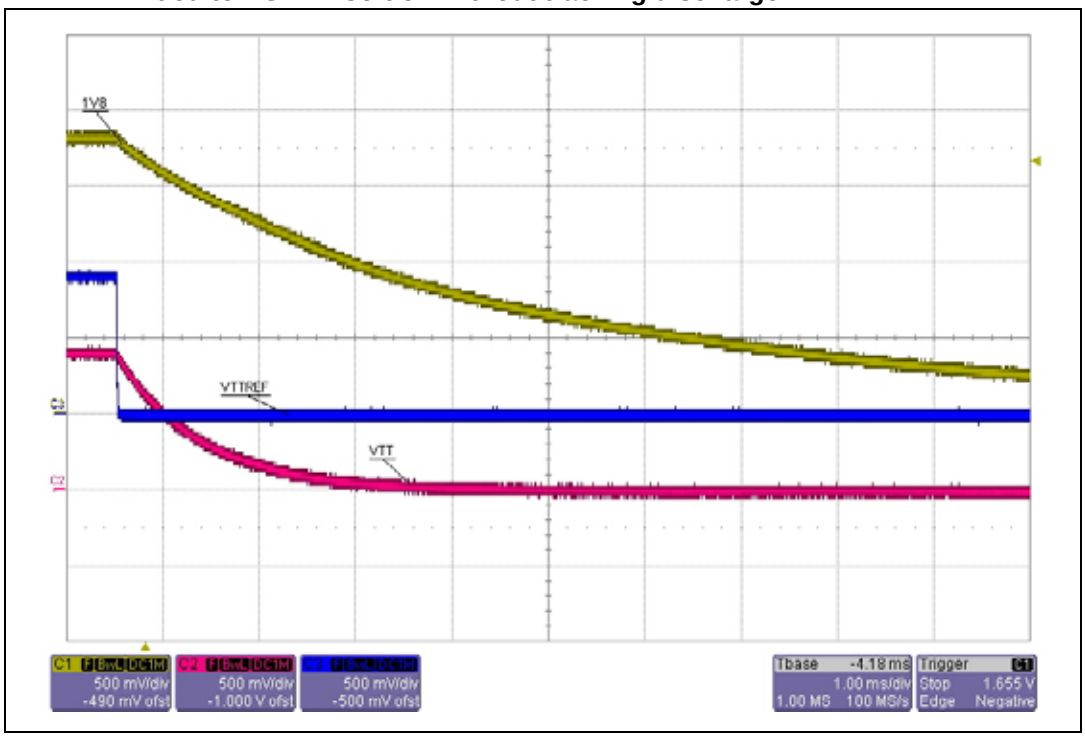


Figure 40. VDDQ(1.8 V), VTT and VTTREF rail output voltage. EN_1S8 and EN_VTT tied to AGND - soft off without tracking discharge



10.10 Thermal behavior

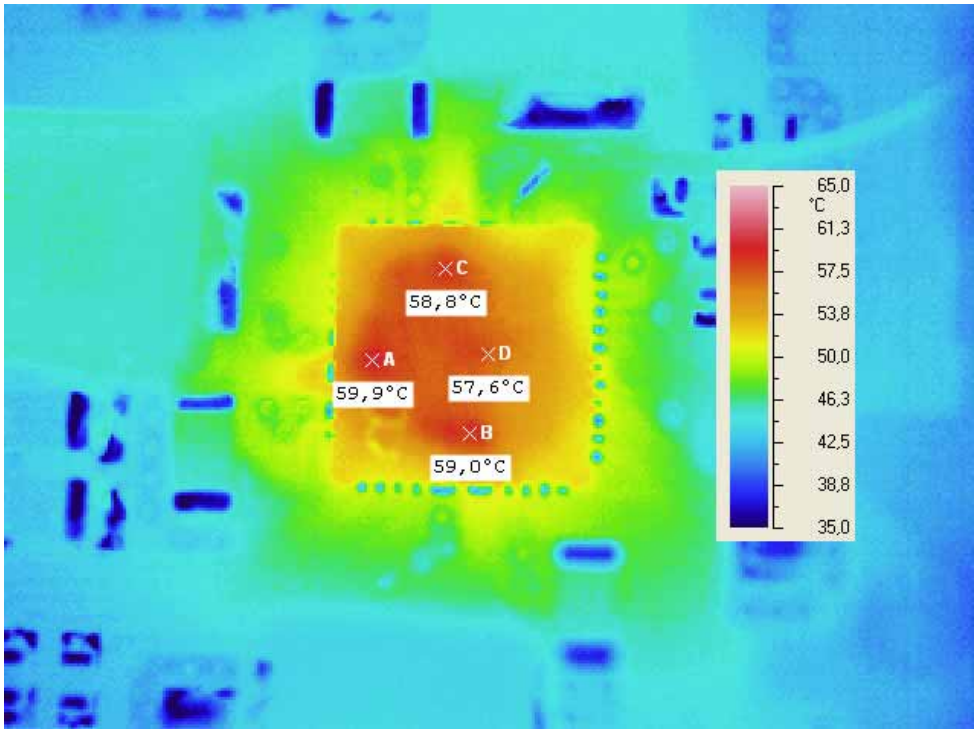
The device temperature is mainly influenced by LDO VTT current. The typical working currents are shown in *Table 3*.

Table 3. Average working currents for each rail

Rail	Current [A]
VDDQ (1.8 V)	1.35
1.5 V	1.25
1.05 V	1.75
VTT (0.9 V)	0.3

VTT is supplied by VDDQ and the device (average) temperature is 54.5 °C.

Figure 41. PM6641 demonstration board surface temperature when loaded with typical currents, T_{amb} = 23 °C, V_{IN} = 3.3 V, F_{SW} = 660 kHz



11 Revision history

Table 4. Document revision history

Date	Revision	Changes
05-Sep-2008	1	Initial release

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