Low Power, 8-Bit, 20Msps, Sampling A/D Converter

FEATURES

- **Low Power, 8-Bit, 20Msps ADC**
- **250MHz Internal Sample-and-Hold**
- **7 Effective Bits at 70MHz Input Frequency**
- **±1LSB DNL and INL Max**
- Single 5V Supply and 150mW Dissipation
- Power Down to 1µA
- True Differential Inputs Reject Common Mode Noise
- Accepts Single-Ended or Differential Input Signals
- ±1V Differential or 2V Single-Ended Input Span
- Analog Inputs Common Mode to V_{DD} and GND
- 24-Pin Narrow SSOP Package

APPLICATIONS

- Telecommunications
- Wireless Communications
- Digital Cellular Telephones
- CCDs and Image Scanners
- Video Digitizing and Digital Television
- Digital Color Copiers
- High Speed Undersampling
- Personal Computer Video
- High Speed Data Acquisition

DESCRIPTION

The LTC®1406 is a 20Msps, 8-bit, sampling A/D converter which draws only 150mW from a single 5V supply. This easy-to-use device includes a high dynamic range sample-and-hold with a 250MHz bandwidth.

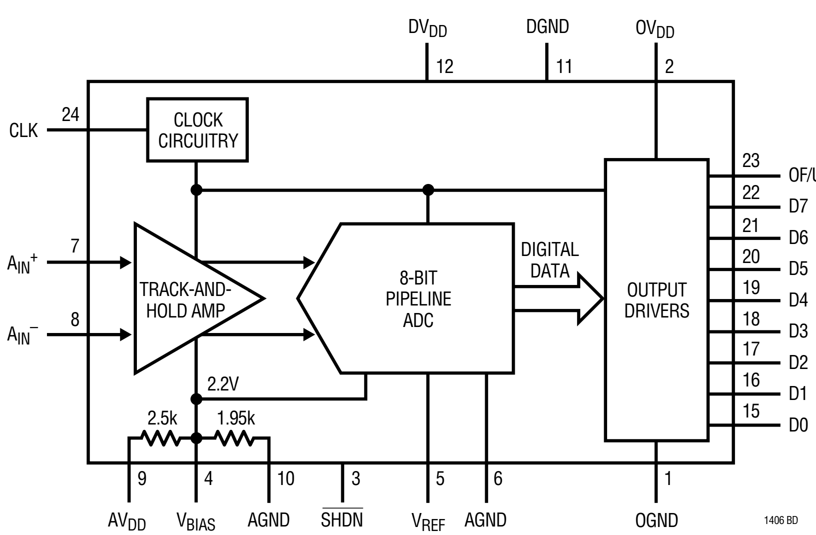
The LTC1406's full-scale input range is ±1V. The inputs can be driven differentially or one input can be tied to a fixed voltage and the other input driven with a ±1V bipolar input. Maximum DC specifications include ±1LSB DNL and INL over temperature. Outstanding AC performance includes 48.5dB S/(N + D) and 62dB THD with a 1MHz input; 47.5dB S/(N + D) and 59dB THD at the Nyquist input frequency of 10MHz.

The unique differential input sample-and-hold can acquire single-ended or differential input signals up to its 250MHz bandwidth. The 60dB common mode rejection allows users to eliminate ground loops and common mode noise by measuring signals differentially from the source.

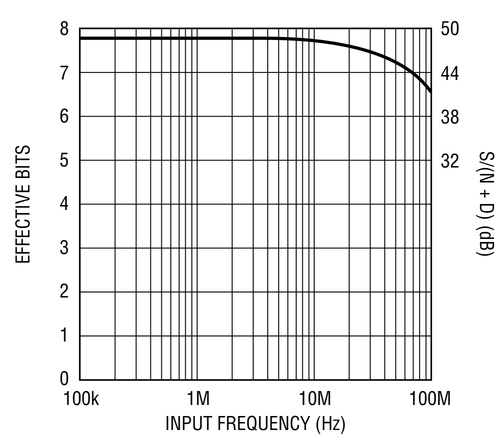
The ADC has an 8-bit parallel output port with separate power supply and ground allowing easy interface to 3V digital systems. The pipelined architecture has five clock cycles of data latency.

TYPICAL APPLICATION

Low Power, 20MHz, 8-Bit Sampling ADC



Effective Bits and Signal-to-Noise + Distortion vs Input Frequency



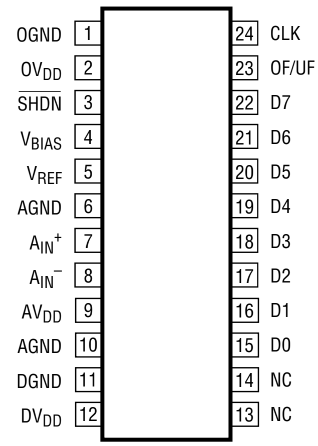
ABSOLUTE MAXIMUM RATINGS

AV_{DD} = OV_{DD} = DV_{DD} = V_{DD} (Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Analog Input Voltage (Note 3) .... – 0.3V to (V_{DD} + 0.3V)
Digital Input Voltage (Note 4) .... – 0.3V to 10V
Digital Output Voltage .... – 0.3V to (V_{DD} + 0.3V)
Power Dissipation 500mW
Ambient Operation Temperature Range
  LTC1406C .... 0°C to 70°C
  LTC1406I .... −40°C to 85°C
Storage Temperature Range .... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW



GN PACKAGE
24-LEAD PLASTIC SSOP
T_{JMAX} = 110°C, θ_{JA} = 85°C/W

ORDER PART NUMBER
LTC1406CGN LTC1406IGN

Consult factory for Military grade parts.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Notes 5, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	8			Bits
Integral Linearity Error	(Note 7)	●		±0.5	±1	LSB
Differential Linearity Error		●		±0.25	±1	LSB
Offset Error	(Note 8)	●		±1	±8	LSB
Gain Error	With External 2.5V Reference			±1	±5	LSB

ANALOG INPUT (Note 5)

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Span [(A_{IN}^+) – (A_{IN}^-)] (Note 9)	4.75V ≤ V_{DD} ≤ 5.25V	●		±1		V
	Input (A_{IN}^+ or A_{IN}^-) Range	Voltage On Either A_{IN}^+ or A_{IN}^-	●	0		V_{DD}	V
I_{IN}	Analog Input Leakage Current	CLK = 0	●			±5	µA
C_{IN}	Analog Input Capacitance	CLK = 1 CLK = 0			4 2		pF pF
	Input Bandwidth				250		MHz
t_{AP}	Sample-and-Hold Aperture Delay Time				3		ns
t_{jitter}	Sample-and-Hold Aperture Delay Time Jitter				5		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio	−2.5V < (A_{IN}^- = A_{IN}^+) < 2.5V			60		dB
V_{BIAS}	Internal Bias Voltage	No Load			2.2		V

DYNAMIC ACCURACY

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	1MHz Input Signal 10MHz Input Signal			48.5 47.5		dB dB
THD	Total Harmonic Distortion	1MHz Input Signal, First 5 Harmonics 10MHz Input Signal, First 5 Harmonics			–62 –59		dB dB
SFDR	Spurious Free Dynamic Range	1MHz Input Signal 10MHz Input Signal			63 60		dB dB
IMD	Intermodulation Distortion	f_{IN1} = 3.500977MHz, f_{IN2} = 3.598633MHz			60		dB

DIGITAL INPUTS AND OUTPUTS (Note 5)

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{DD} = 5.25V	●	2.4			V
V_{IL}	Low Level Input Voltage	V_{DD} = 4.75V	●			0.8	V
I_{IN}	Digital Input Current	V_{IN} = 0V to V_{DD}	●			±5	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	V_{DD} = 4.75V, I_O = –10µA V_{DD} = 4.75V, I_O = –200µA	 ●	 4.0	4.5 		V V
V_{OL}	Low Level Output Voltage	V_{DD} = 4.75V, I_O = 160µA V_{DD} = 4.75V, I_O = 1.6mA	 ●		0.05 0.10	 0.4	V V
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–20		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{DD}			30		mA

POWER REQUIREMENTS (Note 5)

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AV_{DD}	Analog Positive Supply Voltage	(Note 10)		4.75		5.25	V
DV_{DD}	Digital Positive Supply Voltage	(Note 10)		4.75		5.25	V
OV_{DD}	Output Positive Supply Voltage	(Note 10)		2.7		5.25	V
V_{BIAS}	Internal Bias Voltage	When Externally Driven (Note 10)		1.9	2.2	2.5	V
V_{REF}	Reference Voltage	(Note 10)		2	2.5	3	V
OGND	Output Ground	(Note 10)		0		2	V
I_{DD}	Positive Supply Current	AV_{DD} = DV_{DD} = OV_{DD} = 5V, f_{SMPL} = 20MHz (Note 13)	●		30	45	mA
P_D	Power Dissipation		●		150	225	mW
	Power Down Positive Supply Current	$\overline{SHDN}$ = 0V, CLK = V_{DD} or 0			1	10	µA
	Power Down Power Dissipation	$\overline{SHDN}$ = 0V, CLK = V_{DD} or 0			5	50	µW

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SMPL(MAX)}$	Maximum Sampling Frequency		●	20			MHz
t_1	Clock Period	(Notes 11, 12)	●	50			ns
t_2	Pulse Width High	(Notes 11, 12)	●	25			ns
t_3	Pulse Width Low	(Notes 11, 12)	●	25			ns
t_4	Output Delay	C_L = 15pF			15	25	ns
t_5	Pipeline Delay				5		Cycles
t_6	Aperture Delay				3		ns
	Aperture Jitter				5		ps_{RMS}

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground with DGND, OGND and AGND wired together (unless otherwise noted).

Note 3: When these pin voltages are taken below ground or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents greater than 100mA below ground or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below ground they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground without latchup. These pins are not clamped to V_{DD}.

Note 5: V_{DD} = 5V, f_{SMPL} = 20MHz and $t_r = t_f$ = 2ns unless otherwise specified.

Note 6: Linearity, offset and full-scale specifications apply for a single-ended A_{IN}^+ input with A_{IN}^- tied to V_{REF} = 2.5V.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Bipolar offset is the offset voltage measured from –0.5LSB when the output code flickers between 0111 1111 and 1000 0000.

Note 9: Guaranteed by design, not subject to test.

Note 10: Recommended operating conditions.

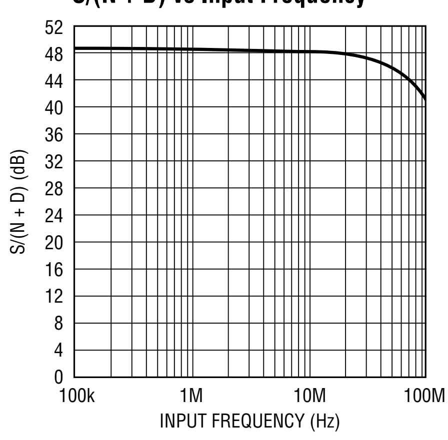
Note 11: The falling CLK edge starts a conversion.

Note 12: At the maximum conversion rate, deviation from a 50% duty cycle results in interstage settling times <25ns and performance may be affected.

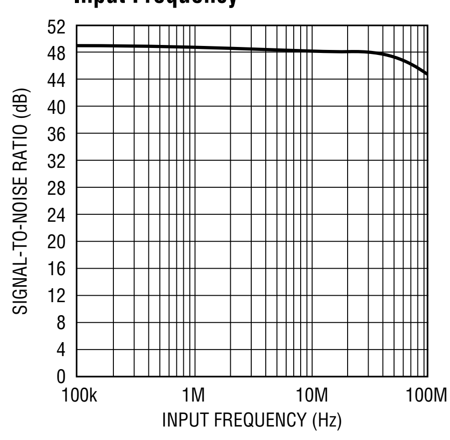
Note 13: V_{IN} = –Full Scale.

TYPICAL PERFORMANCE CHARACTERISTICS

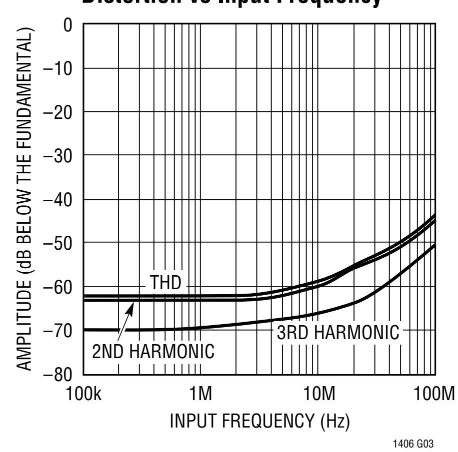
S/(N + D) vs Input Frequency



Signal-to-Noise Ratio vs Input Frequency

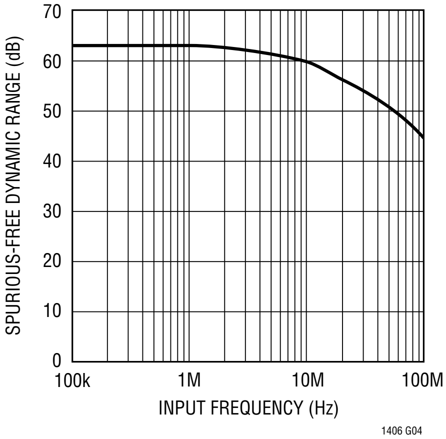


Distortion vs Input Frequency

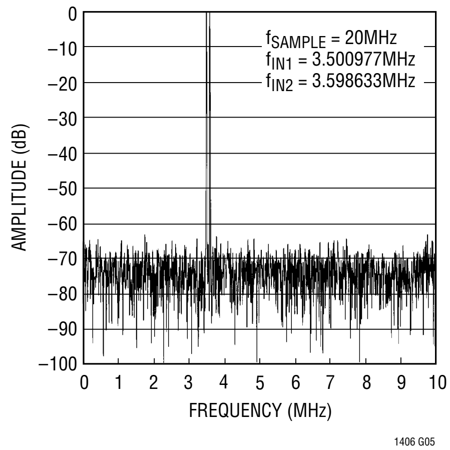


TYPICAL PERFORMANCE CHARACTERISTICS

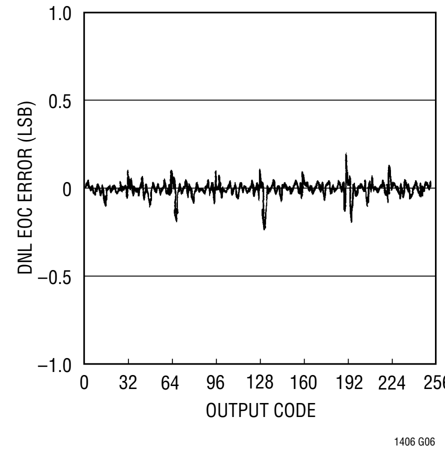
Spurious-Free Dynamic Range vs Input Frequency



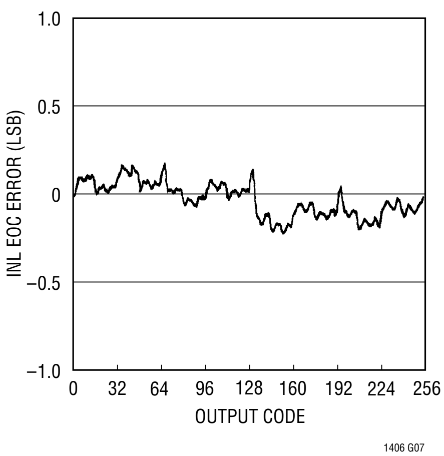
Intermodulation Distortion Plot



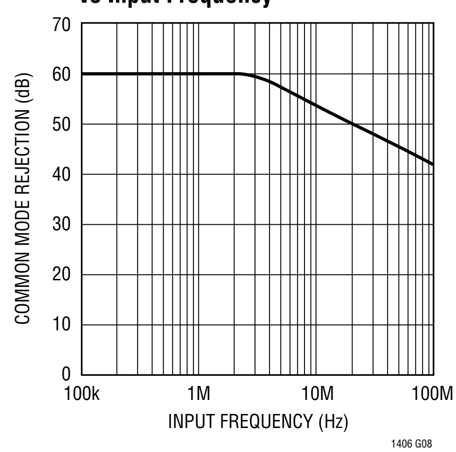
Differential Nonlinearity vs Output Code



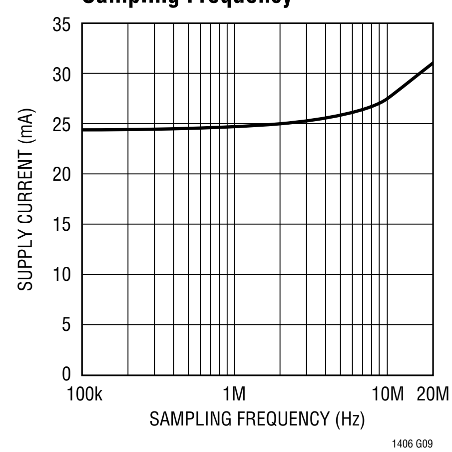
Integral Nonlinearity vs Output Code



Input Common Mode Rejection vs Input Frequency



Supply Current vs Sampling Frequency



PIN FUNCTIONS

OGND (Pin 1): Digital Data Output Ground. Tie to analog ground plane. May be tied to logic ground if desired.

OV_{DD} (Pin 2): Digital Data Output Supply. Normally tied to 5V, can be used to interface with 3V digital logic. Bypass to OGND with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

$\overline{\text{SHDN}}$ (Pin 3): Power Shutdown Input. Logic low selects shutdown.

V_{BIAS} (Pin 4): Internal Bias Voltage. Internally set to 2.2V. Bypass to analog ground plane with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

V_{REF} (Pin 5): External 2.5V Reference Input. Bypass to analog ground plane with 10µF tantalum in parallel with 0.1µF or 10µF ceramic.

AGND (Pin 6): Analog Ground. Tie to analog ground plane.

A_{IN}^+ (Pin 7): ±1V Input. The maximum output code occurs when $[(A_{IN}^+) – (A_{IN}^–)] = 1V$. The minimum output code occurs when $[(A_{IN}^+) – (A_{IN}^–)] = –1V$.

$A_{IN}^–$ (Pin 8): ±1V Input. The maximum output code occurs when $[(A_{IN}^+) – (A_{IN}^–)] = 1V$. The minimum output code occurs when $[(A_{IN}^+) – (A_{IN}^–)] = –1V$. For single-ended operation, tie $A_{IN}^–$ to a DC voltage (e.g., V_{REF}).

PIN FUNCTIONS

AV_{DD} (Pin 9): Analog 5V Positive Supply. Bypass to analog ground plane with 10μF tantalum in parallel with 0.1μF or 10μF ceramic.

AGND (Pin 10): Analog Ground. Tie to analog ground plane.

DGND (Pin 11): Digital Ground for Internal Logic. Tie to analog ground plane.

DV_{DD} (Pin 12): Digital 5V Positive Supply. Bypass to DGND with 10μF tantalum in parallel with 0.1μF or 10μF ceramic.

NC (Pins 13, 14): No Internal Connection.

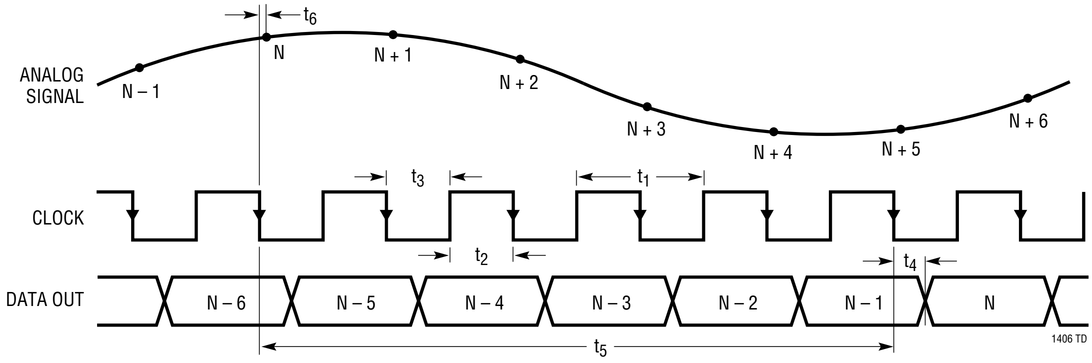
D7 to D0 (Pins 15 to 22): Digital Data Outputs. The outputs swing between OV_{DD} and OGND.

OF/UF (Pin 23): Overflow/Underflow Bit. OF/UF high with D7 to D0 all high indicates an overrange, OF/UF high with D7 to D0 all low indicates an underrange condition. OF/UF low indicates a conversion within the normal input range. The outputs swing between OV_{DD} and OGND.

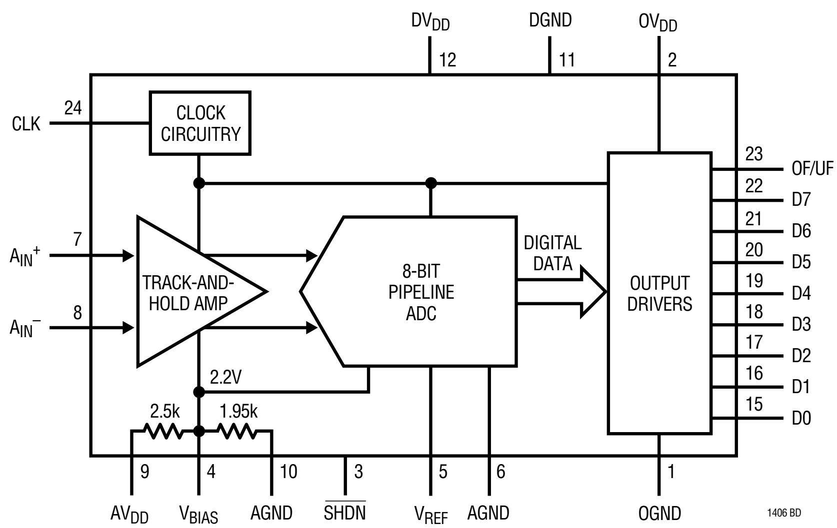
CLK (Pin 24): Clock Input. Internal sample-and-hold tracks the input signal when CLK is high and samples the input signal on the falling edge.

$AV_{DD} = DV_{DD} = V_{DD}$			NOMINAL (V)			ABSOLUTE MAXIMUM (V)	
PIN	NAME	DESCRIPTION	MIN	TYP	MAX	MIN	MAX
1	OGND	Ground for Output Drivers		0		−0.3	V_{DD} + 0.3
2	OV_{DD}	Supply for Output Drivers	2.7	3 or 5	5.25	−0.3	6
3	$\overline{SHDN}$	Shutdown Input, Active Low	0		V_{DD}	−0.3	10
4	V_{BIAS}	Internal Bias Voltage	1.9	2.2	2.5	−0.3	V_{DD} + 0.3
5	V_{REF}	External Reference Input	2	2.5	3	−0.3	V_{DD} + 0.3
6	AGND	Analog Ground, Clean Ground		0		−0.3	V_{DD} + 0.3
7	A_{IN}^+	Positive Analog Input, ±1V Span	0		V_{DD}	−0.3	V_{DD} + 0.3
8	A_{IN}^-	Negative Analog Input	0		V_{DD}	−0.3	V_{DD} + 0.3
9	AV_{DD}	Analog Supply	4.75	5	5.25	−0.3	6
10	AGND	Analog Ground, Substrate Ground		0		−0.3	V_{DD} + 0.3
11	DGND	Digital Ground		0		−0.3	V_{DD} + 0.3
12	DV_{DD}	Digital Supply	4.75	5	5.25	−0.3	6
13 to 14	NC	No Connect, No Internal Connection					
15 to 22	D7 to D0	Data Outputs	OGND		OV_{DD}	−0.3	V_{DD} + 0.3
23	OF/UF	Overflow/Underflow Output	OGND		OV_{DD}	−0.3	V_{DD} + 0.3
24	CLK	Clock Input	0		V_{DD}	−0.3	10

TIMING DIAGRAM



FUNCTIONAL BLOCK DIAGRAM



APPLICATIONS INFORMATION

Conversion Details

The LTC1406 uses an internal sample-and-hold circuit and a pipeline quantizing architecture to convert an analog signal to an 8-bit parallel output. With CLK high the input switches are closed and the analog input will be acquired on the input sampling capacitors C_S (see Figure 1).

On the falling edge of CLK the input switches open, capturing the input signal. The sampling capacitors are then shorted together and the charge is transferred to the hold capacitors C_H resulting in a differential DC voltage on the output of the track-and-hold amplifier that is proportional to the input signal. This differential voltage is fed into a comparator that determines the most significant bit and subtracts the result. The residue is then amplified by two and passed to the next stage via a similar sample-and-hold circuit. This continues down the eight pipeline stages. The comparator outputs are then combined in a digital error correction circuit. The 8-bit word is available at the output, five clock cycles after the sampling edge.

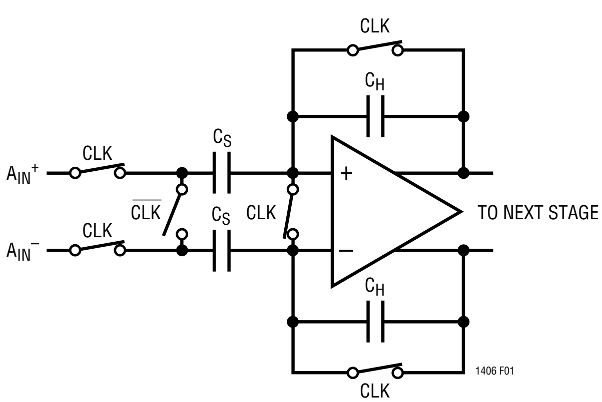


Figure 1. Input Sample-and-Hold Amplifier

Dynamic Performance

The LTC1406 has excellent wideband sampling capability. The sample-and-hold amplifier has a small-signal input bandwidth of 250MHz allowing the ADC to undersample input signals with frequencies well beyond the converter's Nyquist frequency. FFT (Fast Fourier Transform) test techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 2 shows a typical LTC1406 FFT plot.

APPLICATIONS INFORMATION

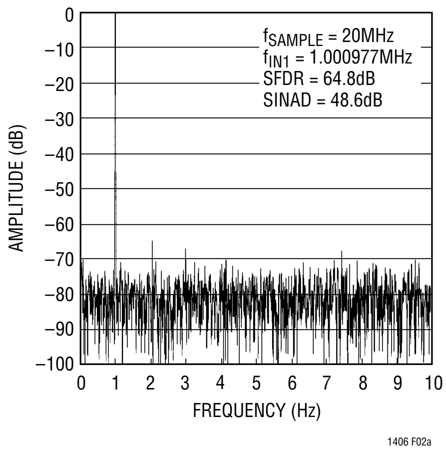


Figure 2a. Nonaveraged, 4096 Point FFT Input Frequency = 1MHz

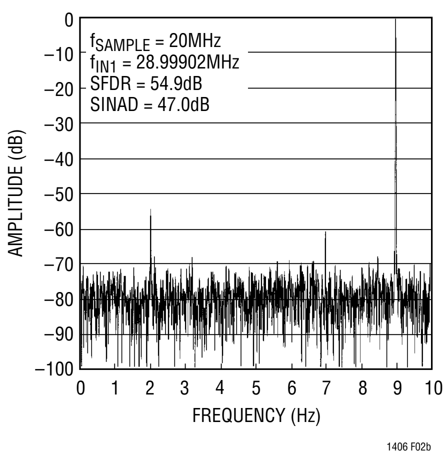


Figure 2b. Nonaveraged, 4096 Point FFT Input Frequency = 30MHz

Signal-to-Noise Ratio

The signal-to-noise plus distortion ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency. The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where ENOB is the effective number of bits and S/(N + D) is expressed in dB. At the maximum sampling rate of 20MHz the LTC1406 maintains near ideal ENOBs up to and beyond the Nyquist input frequency of 10MHz (see Figure 3).

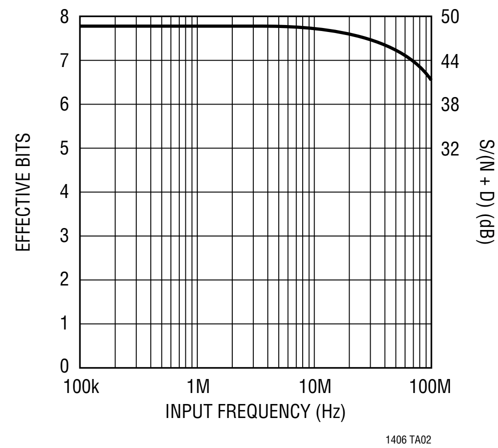


Figure 3. Effective Bits and Signal-to-(Noise + Distortion) vs Input Frequency

Total Harmonic Distortion

Total harmonic distortion is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency. THD is expressed as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots V_n^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_n are the amplitudes of the second through n^{th} harmonics. THD vs Input Frequency is shown in Figure 4. The LTC1406 has good distortion performance up to the Nyquist frequency and beyond.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency (see Figure 5).

APPLICATIONS INFORMATION

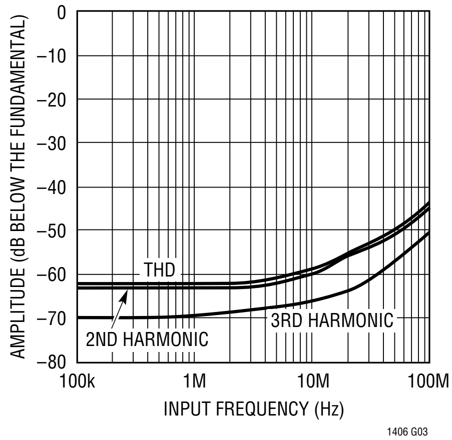


Figure 4. Distortion vs Input Frequency

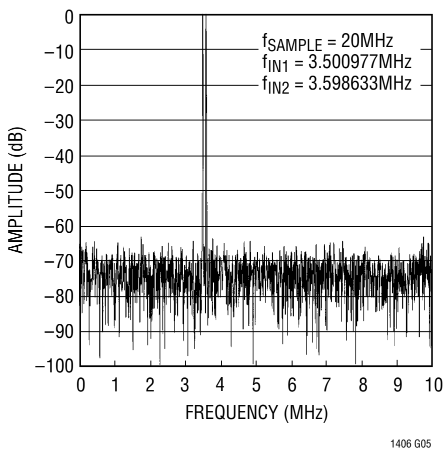


Figure 5. Intermodulation Distortion Plot

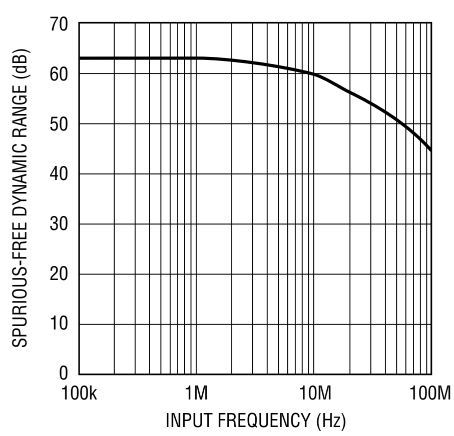


Figure 6. Spurious-Free Dynamic Range vs Input Frequency

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a \pm f_b)$. If the two input sine waves are equal in magnitude, the value (in decibels) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a \pm f_b\right) = 20 \log \frac{\text{Amplitude at } \left(f_a \pm f_b\right)}{\text{Amplitude at } f_a}$$

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in decibel relative to the RMS value of a full-scale input signal (see Figure 6).

Input Bandwidth

The input bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input signal. The LTC1406 has been designed for wide input bandwidth (250MHz), allowing the ADC to undersample input signals with frequencies above the converter's Nyquist frequency. The noise floor stays very low at high frequencies; S/(N + D) becomes dominated by distortion at frequencies far beyond Nyquist.

Analog Inputs

The LTC1406 has a unique differential sample-and-hold circuit that allows rail-to-rail inputs. The A_{IN}^+ and A_{IN}^- inputs are sampled at the same time and the ADC will always convert the difference of $[(A_{IN}^+) – (A_{IN}^-)]$ independent of the common mode voltage. Any unwanted signal that is common to both inputs will be rejected by the common mode rejection of the sample-and-hold circuit. The common mode rejection holds up to extremely high frequencies (see Figure 7).

The inputs can be driven differentially or single-ended. In differential mode, both inputs are driven ±0.5V out of phase with each other. In single-ended mode, the negative input is tied to a fixed voltage and A_{IN}^+ is used as the

APPLICATIONS INFORMATION

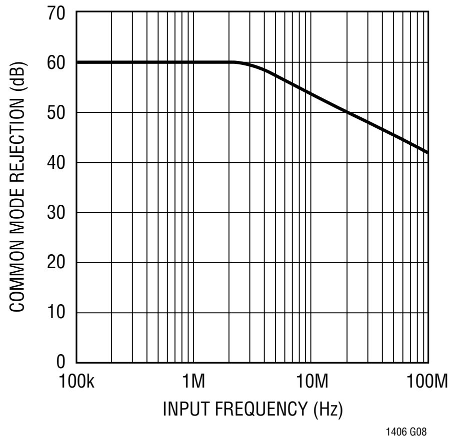


Figure 7. Common Mode Rejection vs Input Frequency

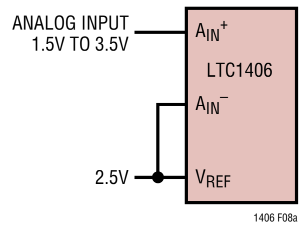


Figure 8a. DC Coupled

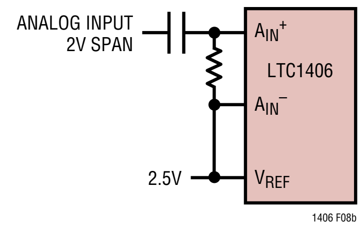


Figure 8b. AC Coupled

single input providing a ±1V bipolar input range centered around A_{IN}^-. Likewise, A_{IN}^+ can be tied to a fixed voltage and A_{IN}^- used as the single input. In any configuration the maximum output code (1111 1111) occurs when $[(A_{IN}^+) - (A_{IN}^-)] = 1V$ and the minimum output code (0000 0000) occurs when $[(A_{IN}^+) - (A_{IN}^-)] = -1V$.

Each analog input can swing from ground to V_{DD} but not beyond. Therefore, the input common mode voltage can range from 0.5V to 4.5V in differential mode and from 1V to 4V in single-ended mode.

As an example, with A_{IN}^- connected to the V_{REF} pin (2.5V) the input range will be 1.5V to 3.5V (see Figure 8a). To achieve other ranges the input may be capacitively coupled to achieve a 2V span with virtually any common mode voltage (see Figure 8b).

The 2V input span requires a 2.5V external reference be connected to the V_{REF} pin. The LT1460-2.5 micropower precision series reference is recommended. To achieve other input spans, the reference voltage (V_{REF}) can vary between 2V to 3V. The V_{REF} pin can also be driven with a DAC or other means. This is useful in applications where the peak input signal amplitude may vary. The input span of the ADC can then be adjusted to match the peak input signal, maximizing the signal-to-noise ratio.

The analog inputs of the LTC1406 are easy to drive. The inputs draw only one small current spike while charging the sample-and-hold capacitors following a rising CLK edge. While CLK is low the analog inputs draw only a small leakage current. If the source impedance of the driving circuit is low, then the LTC1406 inputs can be driven directly. As source impedance increases, so will acquisition time. For minimum acquisition time with high source impedance, a buffer amplifier should be used. The only requirement is that the amplifier driving the analog input(s) must settle after the small current spike before the next conversion starts (settling time must be 25ns for full throughput rate).

Choosing an Input Amplifier

Choosing an input amplifier is easy if a few requirements are taken into consideration. First, to limit the magnitude of the voltage spike seen by the amplifier from charging the sampling capacitor, choose an amplifier that has a low output impedance (<50Ω) at the closed-loop bandwidth frequency. For example, if an amplifier is used in a gain of 1 and has a unity-gain bandwidth of 50MHz, then the output impedance at 50MHz must be less than 50Ω. The second requirement is that the closed-loop bandwidth must be greater than 70MHz to ensure adequate small-signal settling for full throughput rate.

The following list is a summary of the op amps that are suitable for driving the LTC1406. More detailed information is available in the Linear Technology Databooks and on the LinearView™ CD-ROM.

LT®1223: 100MHz Video Current Feedback Amplifier. 6mA supply current. ±5V to ±15V supplies. Low noise.

LT1227: 140MHz Video Current Feedback Amplifier. 10mA supply current. ±5V to ±15V supplies. Low distortion. Low noise.

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LT1229/LT1230: Dual and Quad 100MHz Current Feedback Amplifiers. ±2V to ±15V supplies. Low noise. 6mA supply current each amplifier.

LT1259/LT1260: Dual and Triple 130MHz Current Feedback Amplifiers. ±2V to ±14V supplies. 5mA supply current. Low distortion. Low noise.

LT1363: 70MHz Voltage Feedback Amplifier. ±2.5V to ±15V supplies. 7.5mA supply current. Low distortion.

LT1364/LT1365: Dual and Quad 70MHz Voltage Feedback Amplifiers. ±2.5V to ±15V supplies. 7.5mA supply current per amplifier. Low distortion.

Input Filtering

The noise and the distortion of the input amplifier and other circuitry must be considered since they will add to the LTC1406 noise and distortion. The small-signal bandwidth of the sample-and-hold circuit is 250MHz. Any noise or distortion products that are present at the analog inputs will be summed over this entire bandwidth. Noisy input circuitry should be filtered prior to the analog inputs to minimize noise. A simple 1-pole RC filter is sufficient for many applications. For example, Figure 9 shows a 220pF capacitor from A_{IN}^+ to A_{IN}^- and a 75Ω source resistor to limit the input bandwidth to 9.6MHz. The 220pF capacitor also acts as a charge reservoir for the input sample-and-hold and isolates the ADC input from sampling glitch sensitive circuitry. Larger value capacitors may be substituted to further limit the input bandwidth. High quality capacitors and resistors should be used since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can also generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input/Output Characteristics

Figure 10 shows the ideal input/output characteristics for the LTC1406. The code transitions occur midway between successive integer LSB values (i.e., –FS + 0.5LSB, –FS + 1.5LSB, –FS + 2.5LSB...FS – 1.5LSB, FS – 0.5LSB). The output is straight binary with 1LSB = FS – (–FS)/256 = 2V/256 = 7.8125mV. The OF/UF bit indicates that the input has exceeded full scale and can be used to detect an overrange or underrange condition. A logic high output on the OF/UF pin with an output code of 0000 0000 indicates the input is less than the negative full scale. A logic high output on the OF/UF pin with an output code of 1111 1111 indicates that the input is greater than the positive full scale. A logic low output on the OF/UF pin indicates the input is within the full-scale range of the converter.

In applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Offset error must be adjusted before full-scale error. Zero offset is achieved by adjusting the offset applied to the A_{IN}^- input. For zero offset error, apply a voltage equal to the input

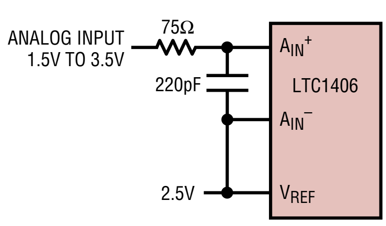

Figure 9. RC Input Filter

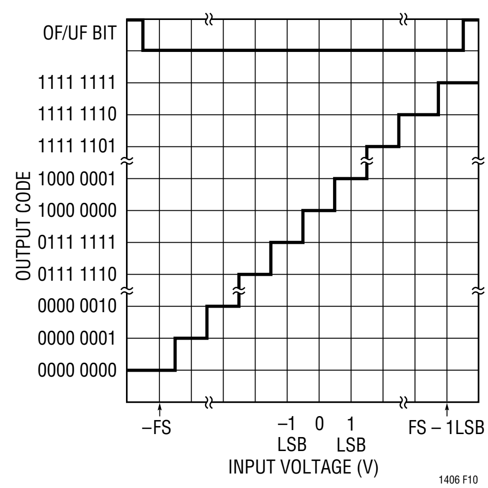

Figure 10. Transfer Characteristics

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common mode voltage minus 3.90625mV (i.e., –0.5LSB) and adjust the offset at the A_{IN}^- input until the output code flickers between 0111 1111 and 1000 0000. For full-scale adjustment, an input voltage equal to the input common mode voltage plus 988.28125mV (i.e., FS – 1.5LSBs) is applied to A_{IN}^+ and the V_{REF} input is adjusted until the output code flickers between 1111 1110 and 1111 1111.

Digital Inputs and Outputs

The LTC1406 is designed to easily interface with either 3V or 5V logic. The digital input pins, $\overline{SHDN}$ and CLK, have thresholds of nominally 1.9V and will accept a 3V or 5V logic input. The data output pins, including OF/UF, are connected to a separate supply and ground (OV_{DD} and OGND respectively). OV_{DD} is normally connected to DV_{DD} but can be connected to an external supply as low as 2.7V. OGND is normally connected to DGND but can be connected to an external ground or an external voltage source as high as 2V.

Clock

The LTC1406 requires a 50% duty cycle clock. The duty cycle should be timed from the nominal threshold of the CLK input which is 1.9V. At conversion speeds below the maximum conversion rate of 20MHz, the duty cycle can deviate from 50% with no degradation in performance as long as each clock phase is at least 25ns long. At the maximum conversion rate, deviation from a 50% duty cycle clock results in interstage settling times of <25ns and performance may be affected.

With the CLK pin high, the ADC will track the difference of the two analog inputs. On the falling edge of CLK the input is sampled and the conversion begins. At the end of five clock cycles (on the fifth falling CLK edge following the start of conversion) the data from the conversion will be available at the digital outputs until the next falling CLK edge. Each falling edge of CLK starts a new conversion so successive conversion results are available on successive falling CLK edges.

While the falling edge starts the conversion, both rising and falling edges are used internally during the conversion. It is therefore important to provide a clock signal that has low jitter and fast rise and fall times (<2ns). Much of the internal circuitry operates dynamically limiting the minimum conversion rate to 10kHz. To ensure proper operation after power is first applied, or the clock stops for more than 100µs, typically 20 clock cycles must be performed at a sample rate above 10kHz before the output data will be valid.

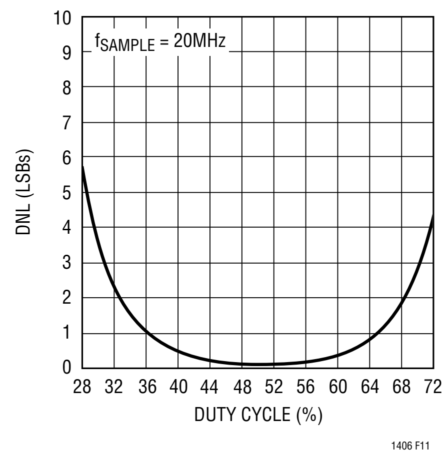

Figure 11. Typical DNL vs Duty Cycle

Power Shutdown

The quiescent power of the LTC1406 can be further reduced between conversions by taking the $\overline{SHDN}$ pin low. This powers down all of the internal amplifiers and bias circuitry and the part draws only a small quiescent current of 1µA from the 5V supply. There is a nominally 4k internal resistor between V_{REF} and AGND that will continue to draw current during shutdown as long as V_{REF} is driven. It should also be noted that the data output drivers are not three-state devices and do not go into a high impedance state during shutdown. If the data output pins will remain connected to a load during shutdown, current may be drawn through the OV_{DD} supply pin. This can be prevented by including a FET switch in series with OV_{DD} or OGND controlled by $\overline{SHDN}$. If the data bus will remain active during

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shutdown. It may also be desirable to isolate the data output pins from the bus to reduce the load capacitance. To resume normal operation the $\overline{SHDN}$ pin must be brought high and typically 20 clock cycles must be performed at a sample rate above 10kHz before the output data will be valid.

Board Layout and Bypassing

Wire wrap boards are not recommended for high resolution or high speed A/D converters. To obtain the best performance from the LTC1406, a printed circuit board with ground plane is required. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

An analog ground plane separate from the logic system ground should be established under and around the ADC. Pin 1 (OGND), Pin 6 (AGND), Pin 10 (AGND) and Pin 11 (DGND) and all other analog grounds should be connected to this single analog ground point. The V_{CM}, V_{REF}, DV_{DD} and OV_{DD} bypass capacitors should also be connected to this analog ground plane. No other digital grounds should be connected to this analog ground plane. In some applications it may be desirable to connect the OV_{DD} to the logic system supply and OGND to the logic system ground. In these cases OV_{DD} should be bypassed to OGND instead of the analog ground plane.

Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC and the foil width for these tracks should be as wide as possible. In applications where the ADC data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get errors in the conversion results. These errors are due to feedthrough from the microprocessor to the comparators. The problem can be eliminated by forcing the microprocessor into a wait state during conversion or by using three-state buffers to isolate the ADC data bus.

The LTC1406 has differential inputs to minimize noise coupling. Common mode noise on the A_{IN}^+ and A_{IN}^- leads will be rejected by the input CMRR. The LTC1406 will hold and convert the difference voltage between A_{IN}^+ and A_{IN}^-. The leads to A_{IN}^+ (Pin 7) and A_{IN}^- (Pin 8) should be kept as short as possible. In applications where this is not possible, the A_{IN}^+ and A_{IN}^- traces should be run side by side to equalize coupling.

Supply Bypassing

High quality, low series resistance ceramic, 10μF bypass capacitors should be used at the V_{DD}, V_{CM} and V_{REF} pins as shown in the Typical Application on the first page of this data sheet. Surface mount ceramic capacitors such as Murata GRM235Y5V106Z016 provide excellent bypassing in a small board space. Alternatively, 10μF tantalum capacitors in parallel with 0.1μF ceramic capacitors can be used. Bypass capacitors must be located as close to the pins as possible. The traces connecting the pins and the bypass capacitors must be kept short and should be made as wide as possible.

Example Layout

Figures 12a, 12b, 12c and 12d show the schematic and layout of an evaluation board. The layout demonstrates the proper use of decoupling capacitors and ground plane with a 2-layer printed circuit board.

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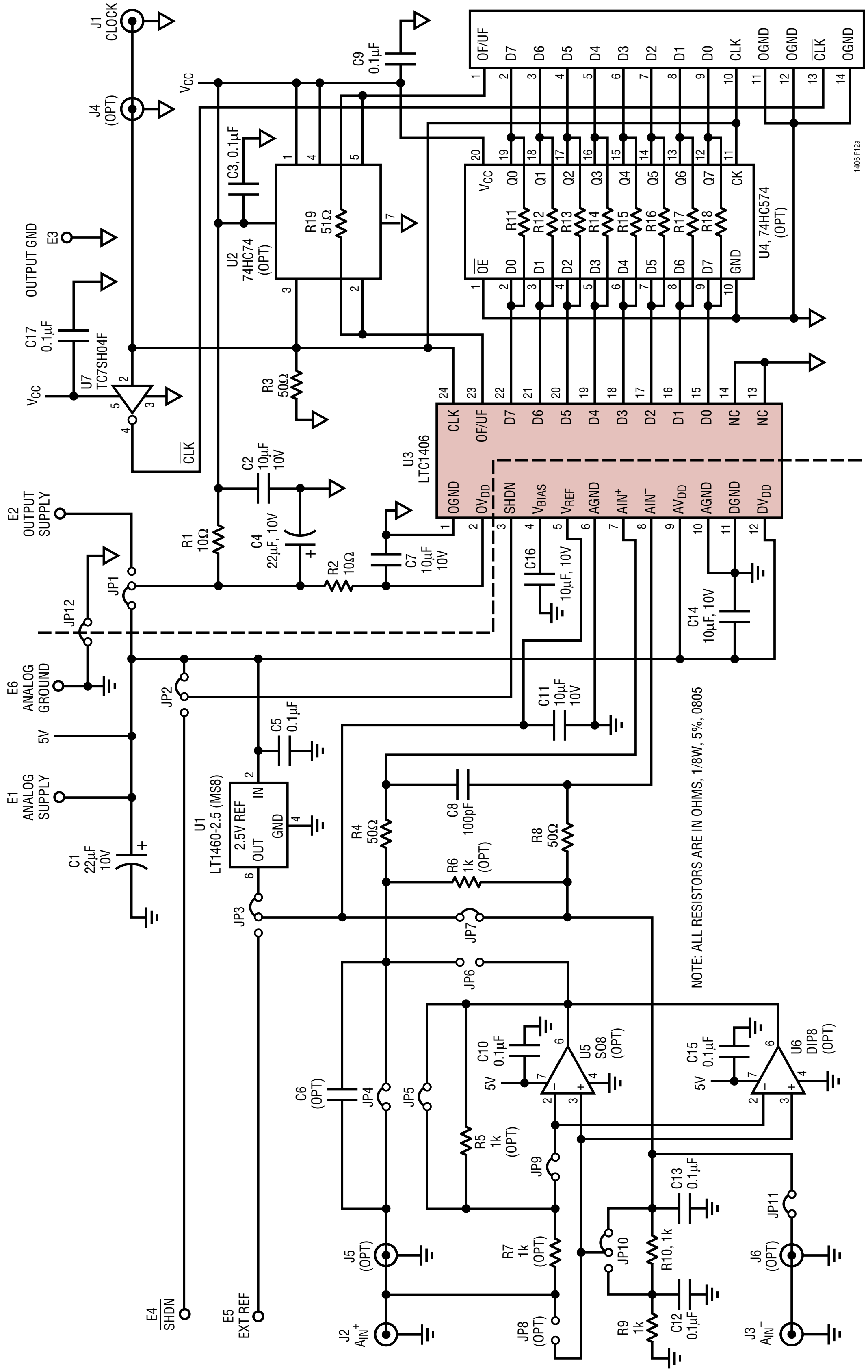

Figure 12a. Suggested Evaluation Circuit Schematic

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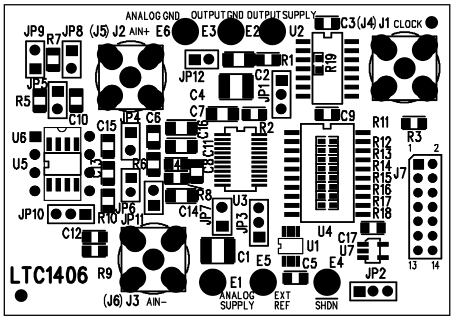


Figure 12b. Suggested Evaluation Circuit Board—Component Side Silkscreen

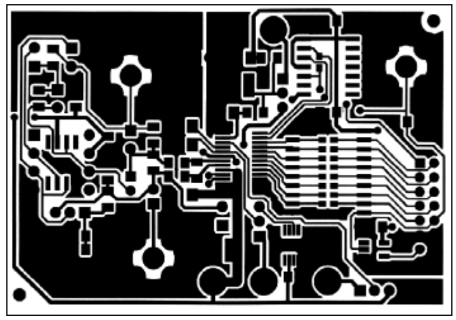


Figure 12c. Suggested Evaluation Circuit Board—Component Side Layout

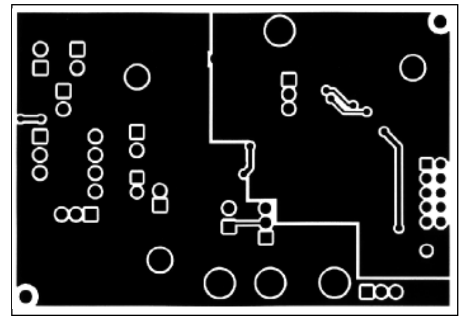
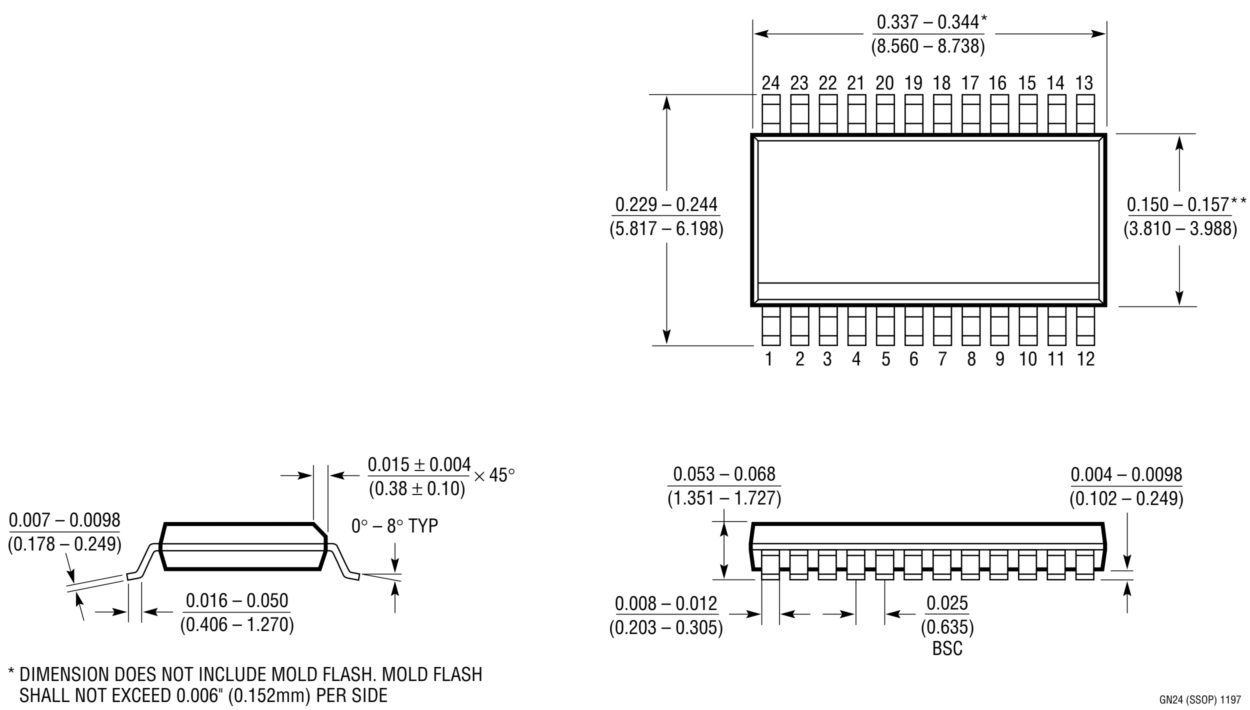


Figure 12d. Suggested Evaluation Circuit Board—Solder Side Layout

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
24-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)

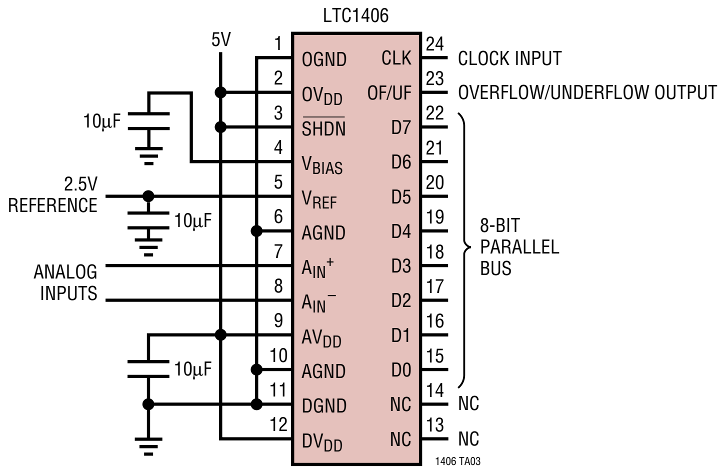


* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

Low Power, 20MHz, 8-Bit Sampling ADC



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1196/LTC1198	Single Supply, 8-Bit, 1Msps/750ksps ADCs	Single 3V or 5V Supply, Low Power, Serial Interface, SO-8 Package
LTC1197/LTC1199	Single Supply, 10-Bit, 500ksps/450ksps ADCs	Single 3V or 5V Supply, Low Power, Serial Interface, SO-8 Package
LTC1410	12-Bit, 1.25Msps Sampling ADC with Shutdown	Best Dynamic Performance, THD = 84dB and SINAD = 71dB at Nyquist
LTC1415	Single 5V, 12-Bit, 1.25Msps ADC	Single Supply 55mW Dissipation
LTC1419	14-Bit, 800ksps Sampling ADC with Shutdown	81.5dB SINAD, 150mW from ±5V Supplies
LTC1604	16-Bit, 333ksps ADC	90dB SINAD, 100dB THD, 250mW Dissipation
LTC1605	Single 5V, 16-Bit, 100ksps ADC	Low Power, ±10V Inputs
DACs		
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package	LTC1446: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1448	Dual 12-Bit Rail-to-Rail Output DAC in SO-8 Package	V_{CC} = 2.7V to 5.5V, Output Swings from GND to REF, REF Input Can Be Tied to V_{CC}
LTC1458/LTC1458L	Quad 12-Bit Rail-to-Rail Output DACs	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V

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