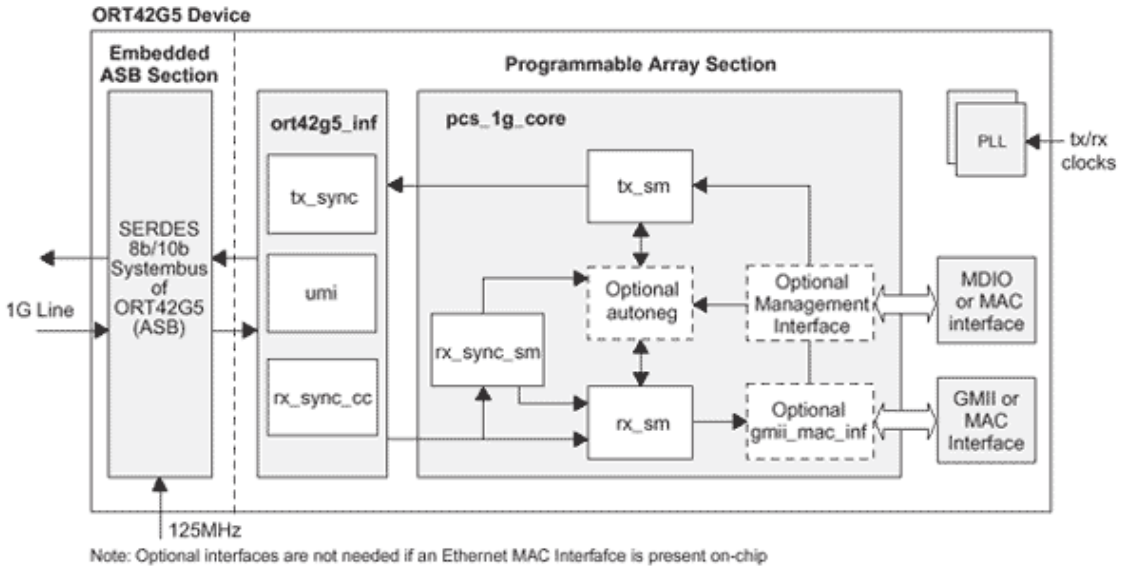
1GbE PCS

Overview

The GbE PCS Intellectual Property (IP) Core targets the programmable array section of the ORCA ORT42G5 FPSC and provides the PCS (Physical Coding Sub-layer) function.



Note: Optional interfaces are not needed if an Ethernet MAC Interfafce is present on-chip

Features

Complete 1Gb Ethernet Physical Coding Sublayer Solution Based on the ORCA® ORT42G5 Device

IP Targeted to the ORT42G5 Programmable Array Section Implements Functionality Conforming to IEEE 803.2-2002

- Encoding/decoding for GMII data octets
- Optional Auto-negotiation function with management registers and interface
- External GMII interface or internal interface to single chip MAC and PCS implementation

Ethernet Functionality Supported by the Embedded Section of the ORT42G5, including:

- Support for 8b/10b encoding/decoding
- Serialization/deserialization of code groups for transmit/receive
- Clock recovery from encoded data stream

Simulation Models and Test Benches

Evaluation Configuration

Evaluation Configuration Table

Configuration	1gbe_pcs_o4_1_001
PFUs	157
Block RAM	4
PLL	2
LUTs	622
Registers	605

fMAX	125 MHz tx_clk rx_clk

Ordering Information

Part Numbers:
For ORCA 4 FPSC: 1GBE-PCS-O4-N1

To find out how to purchase the 1GbE PCS IP Core, please contact your **local Lattice Sales Office**.