# Serial RapidIO - Physical Layer Interface

**Documents & Downloads**

- Downloadable IP
- Downloadable Software
- Tutorials
- User Manuals
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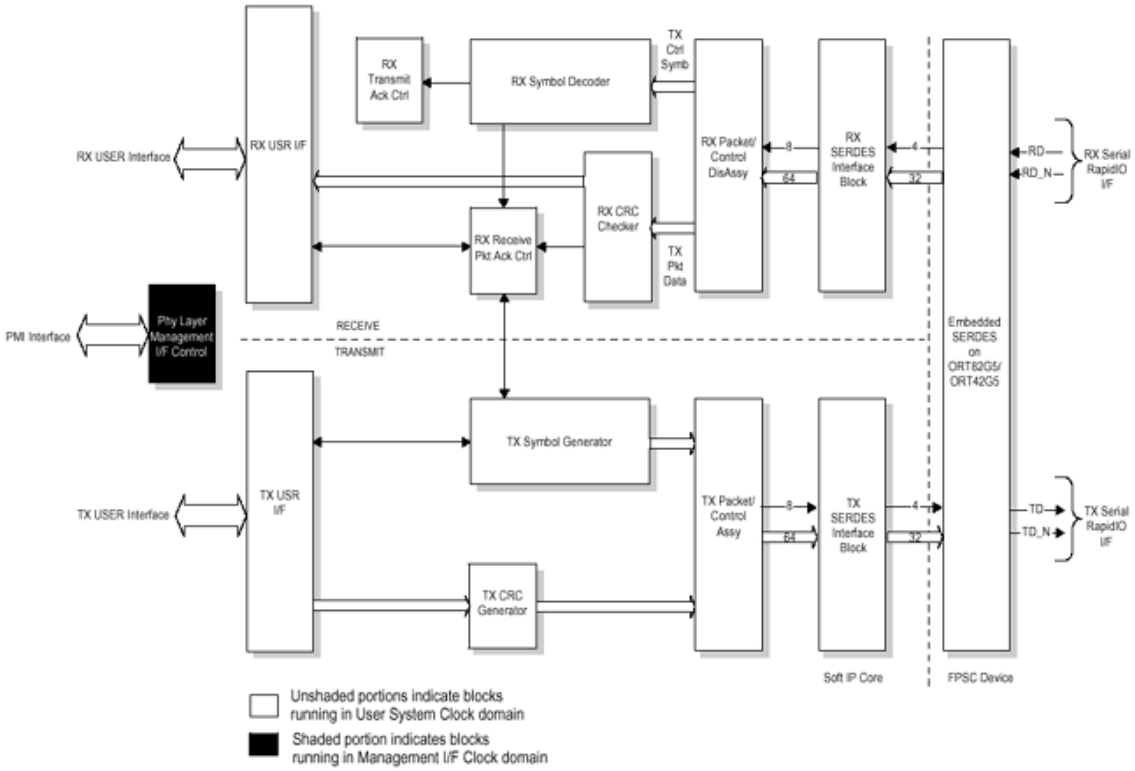
**See Also**

- IP and Reference Design Forum

## Overview

The Serial RapidIO core supports the physical layer specification as defined in the RapidIO Specification Rev 1.2. The Serial RapidIO Physical Layer defines a protocol for packet delivery between Serial RapidIO devices and other devices, including packet transmission, flow control, error management and link maintenance protocols. The core supports one-lane high speed (1x mode) running at 1.0, 2.0 Gbps or a maximum of 2.5 Gbps. This Serial RapidIO core is optimized to support ORT82G5/ORT42G5 FPSCs.




## Features

- Supports High Speed 1x Mode (up to 2.5 Gbps)
- 8B/10B Encoding and Decoding
- Clock and Data Recovery (CDR)
- Lane Synchronization
- CRC Generation and Checking
- Error Detection
- Packet/Control Symbol Assembly and De-assembly
- Simple User Interface for Easy Integration into User Logic
- Targets ORT82G5/ORT42G5 FPSC

## Evaluation Configurations

**Performance and Utilization for ORCA 4[1]**

| Name of Parameter File | rio_seri_t42g5_1_001.lpc |
|---|---|
| ORCA 4[2] PFUs | 996 |
| LUTs[2] | 4386 |

| | |
|---|---|
| **Registers[2]** | 4232 |
| **EBR** | 23 |
| **PIO[2]** | 178 |
| **$f_{MAX}$ sys_clk and pmi_usr_clk (MHz)** | 39.0625 |

[1] Performance and utilization characteristics are generated using an ORT42G5-2BM484 in Lattice's ispLEVER v.3.1 software. When using this IP core in a different density, package, speed, or grade within ORCA 4 family, performance and utilization may vary.

[2] Performance and utilization characteristics are counted based on the utilization of the top level module which includes rios_smi module.

## Ordering Information

**Part Numbers:**

For ORCA 4 FPSC: RIO-SERI-T42G5-N1

To find out how to purchase the 32 Bit PCI Target IP Core, please contact your **local Lattice Sales Office**.