RoHS Pb SP724 Lead-Free

The SP724 is a quad array of transient voltage clamping circuits designed to suppress ESD and other transient over-voltage events. The SP724 is used to help protect sensitive digital or analog input circuits on data, signal, or control lines operating on power supplies up to 20VDC.

The SP724 is comprised of bipolar SCR/diode structures to protect up to four independent lines by clamping transients of either polarity to the power supply rails. The SP724 offers very low leakage (1nA Typical) and low input capacitance (3pF Typical). Additionally, the SP724 is rated to withstand the IEC 61000-4-2 ESD specification for both contact and air discharge methods to level 4.

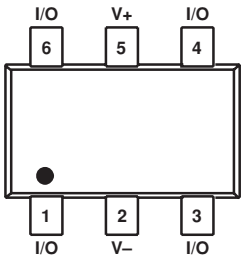
The SP724 is connected to the sensitive input line and its associated power supply lines. Clamping action occurs during the transient pulse, turning on the diode and fast triggering SCR structures when the voltage on the input line exceeds one V_{BE} threshold above the V+ supply (or one V_{BE} threshold below the V- supply). Therefore, the SP724P operation is unaffected by poor power supply regulation or voltage fluctuations within its operating range.

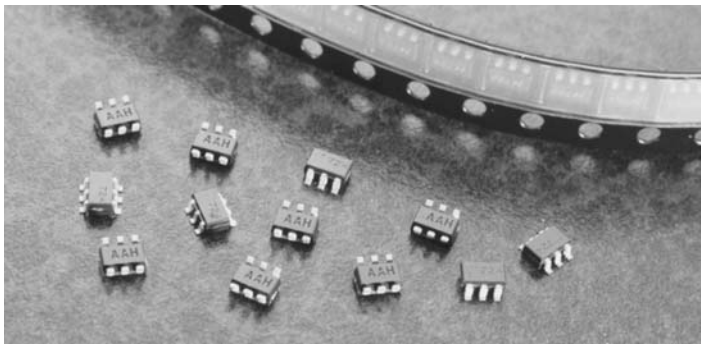
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	Marking	Min. Order Qty.
SP724AHTP	-40 to 105	Tape and Reel	724P	3000

Pinout

SP724
(SOT-23)
TOP VIEW





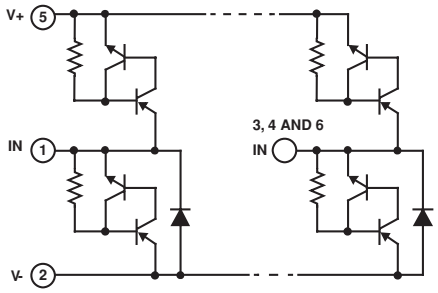
Features

- An Array of 4 SCR/Diode Pairs in 6-Lead SOT-23
- ESD Capability per HBM Standards
  - IEC 61000-4-2, Direct Discharge . . . . . 8kV (Level 4)
  - IEC 61000-4-2, Air Discharge . . . . . 15kV (Level 4)
  - MIL STD 3015.7 . . . . . >8kV
- Input Protection for Applications with Power Supplies Up to +20V (Single-Ended Voltage), and ±10V (Differential Voltage)
- Peak Current Capability
  - IEC 61000-4-5 (8/20µs) . . . . . ±3A
  - Single Pulse, 100µs Pulse Width . . . . . ±2.2A
- Low Input Leakage . . . . . 1nA Typical
- Low Input Capacitance . . . . . 3pF Typical
- Operating Temperature Range . . . . . -40°C to 105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Functional Block Diagram



NOTES:

1. The design of the SP724 SCR/Diode ESD Protection Arrays are covered by Littelfuse patent 4567500.
2. The full ESD capability of the SP724 is achieved when wired in a circuit that includes connection to both the V+ and V- pins. When handling individual devices, follow proper procedures for electrostatic discharge.

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Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-). . . . . +20V

Forward Peak Current, I_{IN} to V_{CC} , GND
(Refer to Figure 6). . . . . ±2.2A, 100µs

ESD Ratings and Capability - See Figure 1, Table 1

Thermal Information

Thermal Resistance (Typical, Note 3) θ_{JA} (°C/W)
SOT Package 220

Maximum Storage Temperature Range. . . . . -65°C to 150°C

Maximum Junction Temperature . . . . . 150°C

Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOT - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications T_A = -40°C to 105°C, V_{IN} = 0.5V_{CC} , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)] (Notes 4, 5)	V_{SUPPLY}		1	-	20	V
Forward Voltage Drop IN to V-	V_{FWDL}	I_{IN} = 1A (Peak Pulse)	-	2	-	V
IN to V+	V_{FWDH}		-	2	-	V
Input Leakage Current	I_{IN}		-10	1	10	nA
Quiescent Supply Current	$I_{QUIESCENT}$	V+ = 20V, V- = GND	-	-	100	nA
Equivalent SCR ON Threshold		(Note 6)	-	1.1	-	V
Equivalent SCR ON Resistance		V_{FWD}/I_{FWD} (Note 6)	-	1.0	-	Ω
Input Capacitance	C_{IN}		-	3	-	pF

NOTES:

4. In automotive and other battery charging systems, the SP724 power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- Pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the external supply and the SP724 supply pins to limit reverse battery current to within the rated maximum limits.
5. Bypass capacitors of typically 0.01µF or larger should be connected closely between the V+ and V- Pins for all applications.
6. Refer to the Figure 3 graph for definitions of equivalent "SCR ON Threshold" and "SCR ON Resistance". These characteristics are given here for information to determine peak current and dissipation under EOS conditions.

ESD Rating

ESD rating is dependent on the defined test standard. The evaluation results for various test standards and methods based on Figure 1 are shown in Table 1.3

The SP724 has a Level 4 rating when tested to the IEC 61000-4-2 Human Body Model (HBM) standard and connected in a circuit in which the V+ and V- pins have a return path to ground. Level 4 specifies a required capability greater than 8kV for direct discharge and greater than 15kV for air discharge.

The "Modified" MIL-STD-3015.7 condition is defined as an "in-circuit" method of ESD testing, the V+ and V- pins have a return path to ground.The SP724 ESD capability is greater than 8kV with 100pF discharged through 1.5kΩ. By strict definition of the standard MIL-STD-3015.7 method using "pin-to-pin" device testing, the ESD voltage capability is greater than 2kV.

For the SP724 EIAJ IC121 Machine Model (MM) standard, the ESD capability is typically greater than 1.8kV with 200pF discharged through 0kΩ.

The Charged Device model is based upon the self-capacitance of the SOT-23 package through 0kΩ.

TABLE 1. ESD TEST CONDITIONS

STANDARD	TYPE/MODE	R_D	C_D	±V_D
IEC 61000-4-2 (Level 4)	HBM, Air Discharge	330Ω	150pF	15kV
	HBM, Direct Discharge	330Ω	150pF	8kV
MIL-STD-3015.7	Modified HBM	1.5kΩ	100pF	8kV†
	Standard HBM	1.5kΩ	100pF	2kV
EIAJ IC121	Machine Model	0kΩ	200pF	400V
US ESD DS 5.3	Charged Device Model	0kΩ	NA	3kV

†Upper limit of laboratory test set.

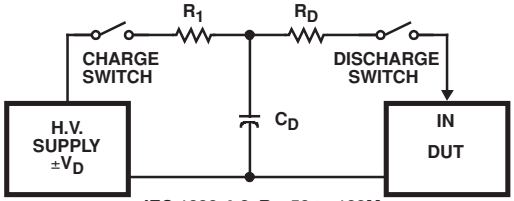

FIGURE 1. ELECTROSTATIC DISCHARGE TEST

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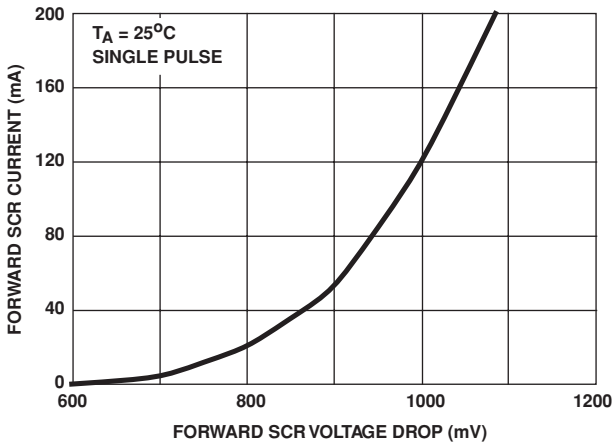

FIGURE 2. LOW CURRENT SCR FORWARD VOLTAGE DROP CURVE

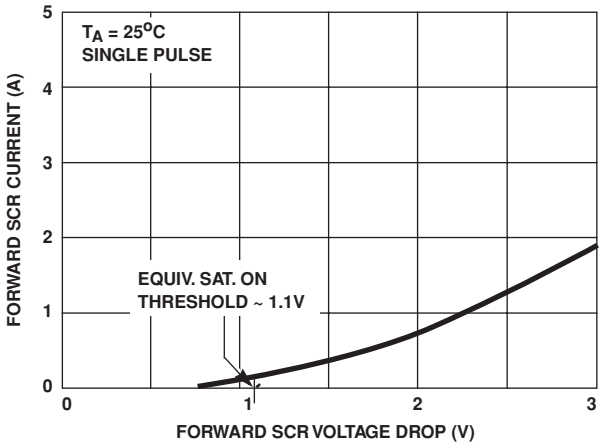

FIGURE 3. HIGH CURRENT SCR FORWARD VOLTAGE DROP CURVE

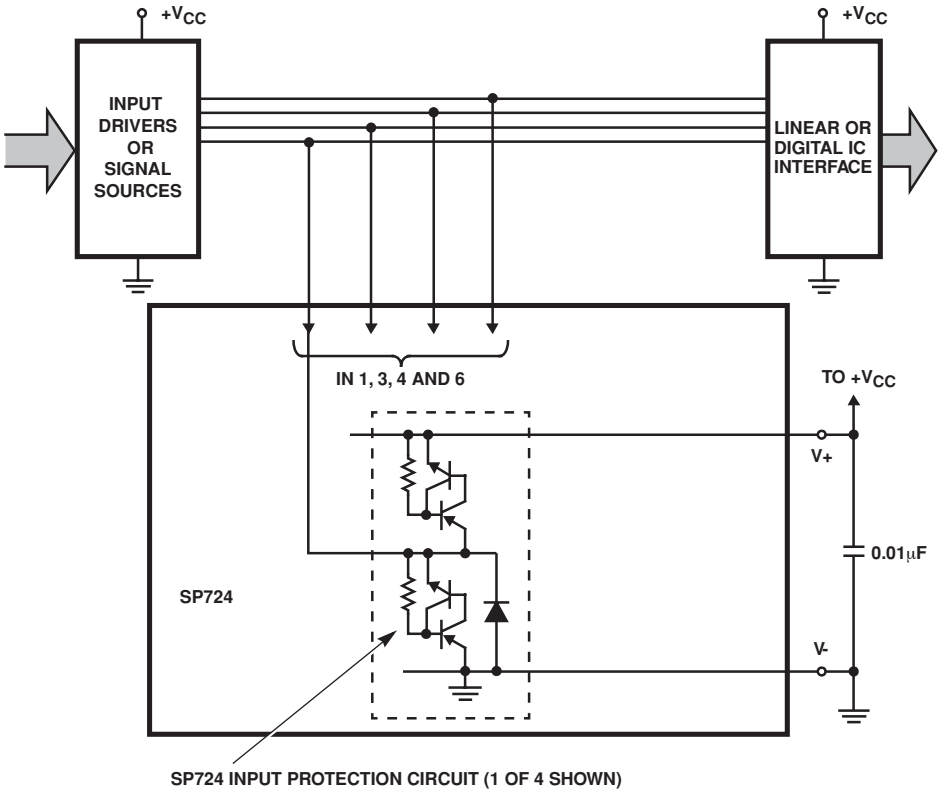

FIGURE 4. TYPICAL APPLICATION OF THE SP724 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN 1V_{BE} ABOVE V+ OR LESS THAN -1V_{BE} BELOW V-

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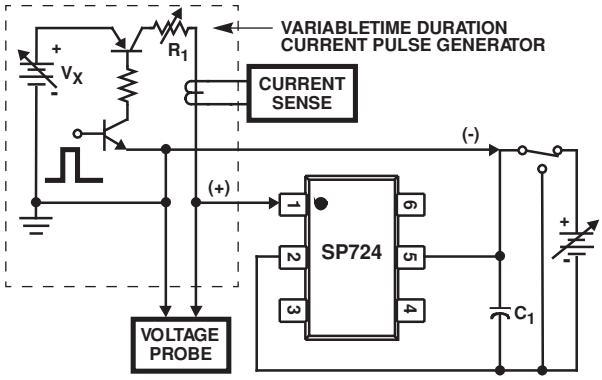
Peak Transient Current Capability for Long Duration Surges

The peak transient current capability is inversely proportional to the width of the current pulse. Testing was done to fully evaluate the SP724's ability to withstand long duration current pulses using the circuit of Figure 5. Figure 6 shows the point of overstress as defined by increased leakage in excess of the data sheet published limits. The safe operating range of the transient peak current should be limited to no more than 75% of the measured overstress level for any given pulse width as shown in the curve of Figure 6.

The test circuit of Figure 5 is shown with a positive pulse input. For a negative pulse input, the (-) current pulse input goes to an SP724 'IN' input pin and the (+) current pulse input goes to the SP724 V- pin. The V+ to V- supply of the SP724 must be allowed to float. (i.e., It is not tied to the ground reference of the current pulse generator.)

Note that two input pins of the SP724 may be paralleled to improve current (and ESD) capability. The sustained peak current capability is increased to nearly twice that of a single pin.



R_1 ~ 10Ω TYPICAL
V_X ADJ. 10V/A TYPICAL
C_1 ~ 100μF

FIGURE 5. TYPICAL SP724 PEAK CURRENT TEST CIRCUIT WITH A VARIABLE PULSE WIDTH INPUT

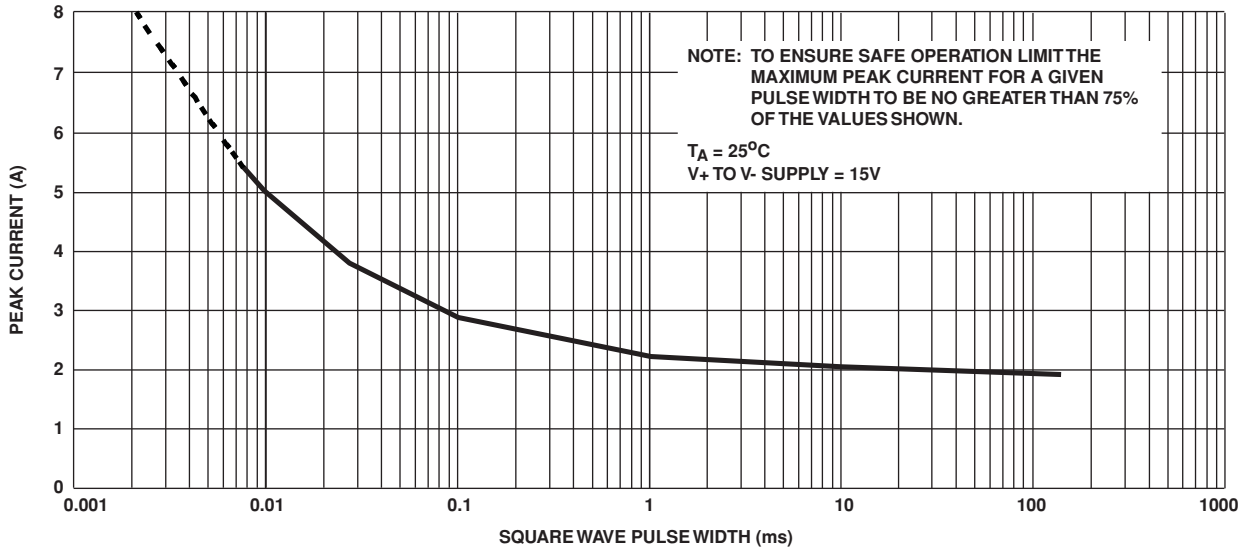


FIGURE 6. SP724 TYPICAL NONREPETITIVE PEAK CURRENT PULSE CAPABILITY

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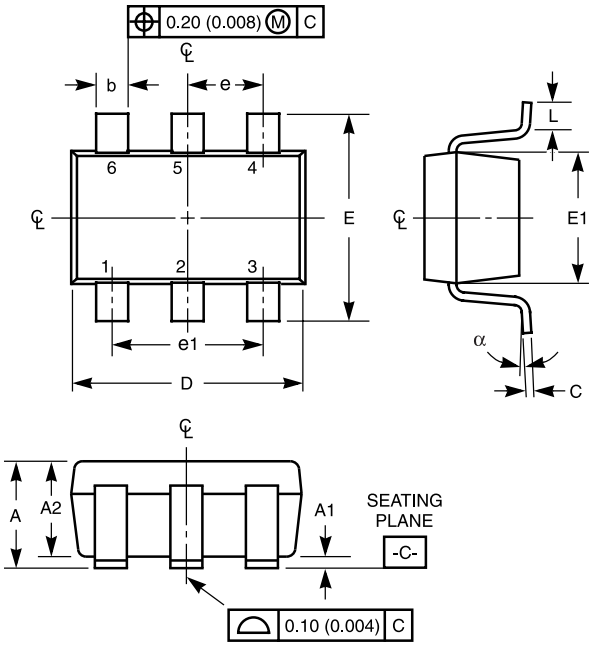
Small Outline Transistor Plastic Packages (SOT23-6)



NOTES:

1. Dimensioning and tolerances per ANSI 14.5M-1982.
2. Package conforms to EIAJ SC-74 (1992).
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to seating plane.
5. "L" is the length of flat foot surface for soldering to substrate.
6. "N" is the number of terminal positions.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

SOT23-6

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.0138	0.0196	0.35	0.50	-
C	0.0036	0.0078	0.09	0.20	-
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.068	1.50	1.75	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.90 Ref		-
L	0.004	0.023	0.10	0.60	4, 5
N	6		6		6
α	0°	10°	0°	10°	-

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Package Information

Mechanical Specifications	
Lead Plating	Matte Tin
Lead Material	Copper Alloy
Lead Coplanarity	0.102mm (0.004 inches)
Subsitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL94-V-0

Notes:
1. All dimensions are in millimeters.
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. All specifications comply to JEDEC SPEC MO-203 ISSUE A.
5. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
6. Package surface matte finish VDI 11-13.

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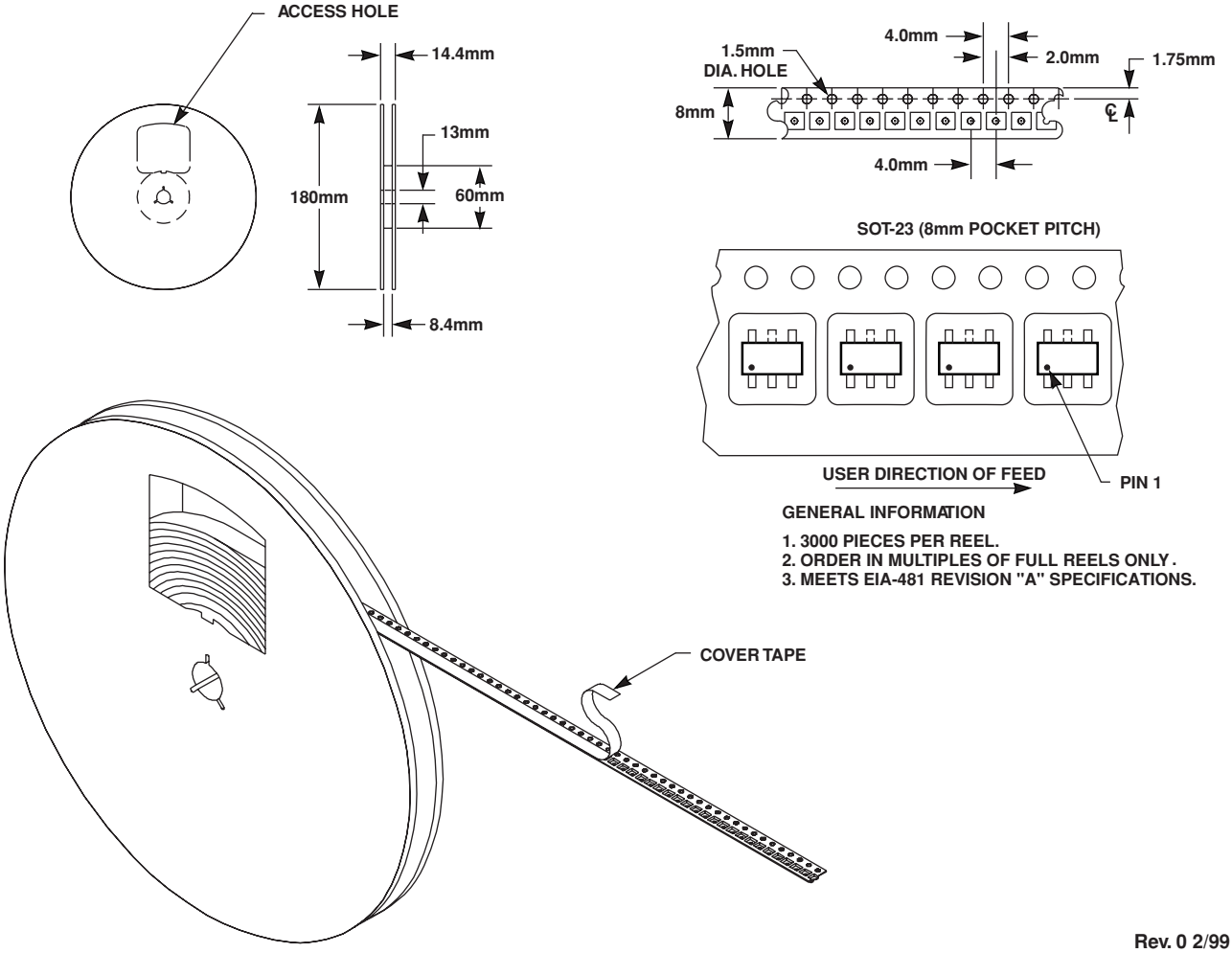
SOT23-6

8mm TAPE AND REEL



GENERAL INFORMATION

1. 3000 PIECES PER REEL.
2. ORDER IN MULTIPLES OF FULL REELS ONLY.
3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

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