DS26519DK
16-Port T1/E1/J1 Transceiver Demo Kit

www.maxim-ic.com

GENERAL DESCRIPTION

The DS26519DK is an easy-to-use evaluation board for the DS26519 16-port T1/E1/J1 transceiver. The DS26519DK is a stand-alone system. The board comes complete with a transceiver, transformers, termination resistors, configuration jumpers, network connectors, processor, RS-232 interface, and power adapter. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs support GPIO pins to indicate status, and FPGAs provide for multiple clock and signal routing configurations.

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DEMO KIT CONTENTS

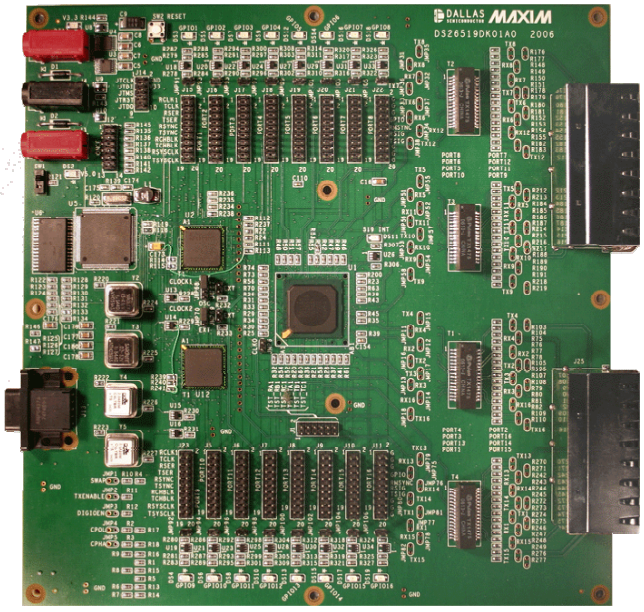
DS26519DK Board
CD_ROM Including:
- ChipView Software
- DS26519 Definition Files
- DS26519DK Definition File
- DS26519DK Data Sheet
- DS26519 Data Sheet

FEATURES

- **Demonstrates Key Functions of DS26519 T1/E1/J1 SCT**
- **Network Connectors, Transformers, and Termination Ease Connectivity**
- **Careful Layout Provides Signal Integrity**
- **On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS26519 Register Set**
- **Software-Controlled (Register Mapped) Configuration Switches Facilitate Clock and Signal Routing**
- **All System-Side Framer Pins are Easily Accessible for External Data Source/Sink**
- **LEDs Programmed via GPIO Pins Provide Status**
- **Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs**

ORDERING INFORMATION

PART	DESCRIPTION
DS26519DK	Demo kit for DS26519



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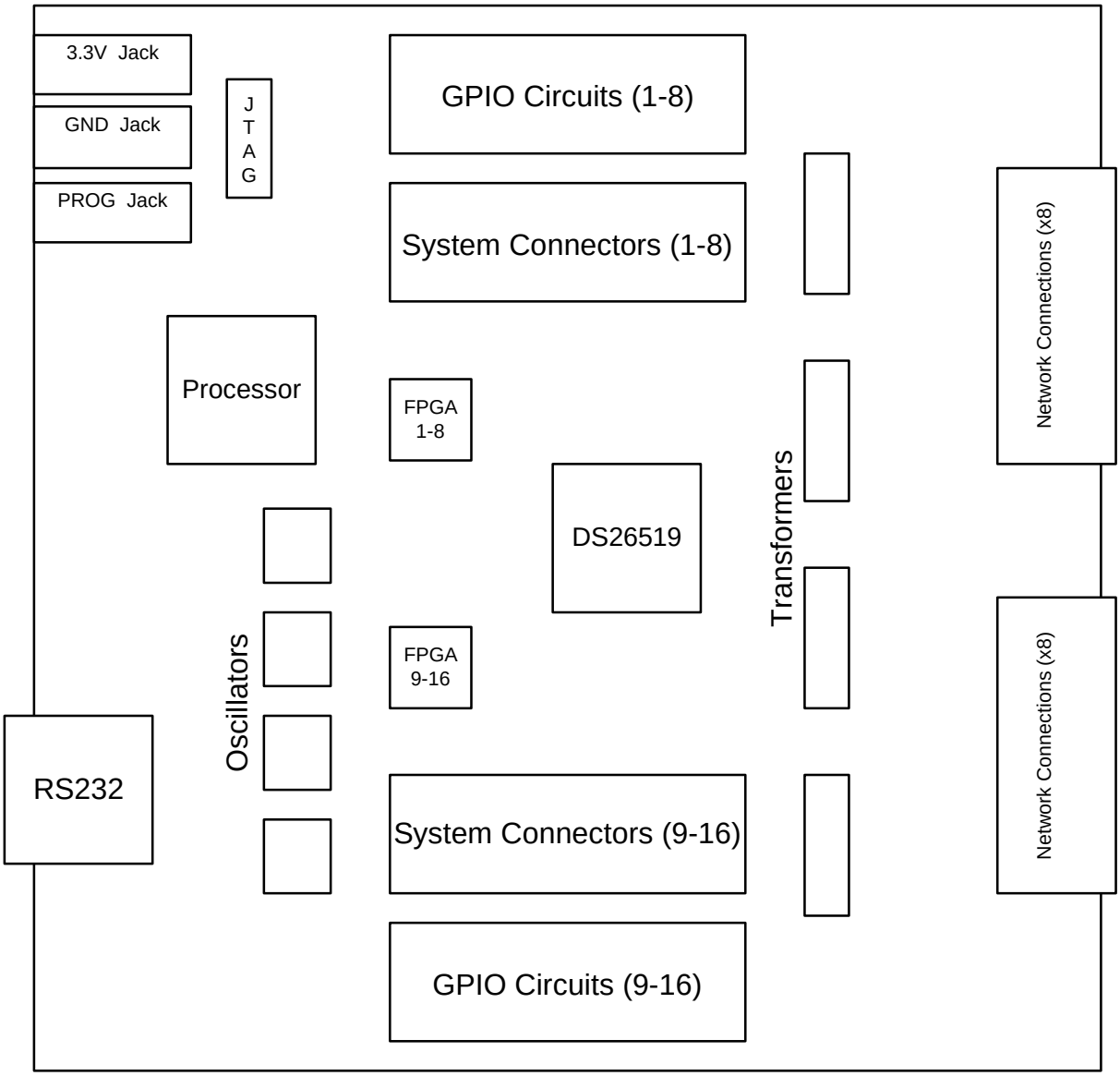
1. BOARD FLOORPLAN

Figure 1 shows the floor plan of the DS26519DK. The DS26519 is near the center of the board. The network connections are provided on the right side of the board, which includes transformers and stacked RJ48 connectors. Toward the center of the board are two FPGAs that provide muxes for control of system-side connections via memory-mapped registers. Above and below the DS26519 are headers that provide access to all system-side signals. The GPIO circuits next to the system connectors provide an interface to the GPIO pins via a header and an LED for each GPIO. The power-supply connections, microprocessor, and JTAG connection are all in the top left quadrant of the board. The power-supply section has three banana jacks for 3.3V, ground, and programming (used at the factory). The bottom left quadrant of the board houses a serial port connector for interface to a computer and clock distribution circuitry.

Figure 1-1. DS26519DK Board Floorplan



2. CLOCK JUMPERS

Jumpers JMP68 and JMP70 (middle left of board) select the main clock source for ports 1–8 and ports 9–16, respectively. The source can be external via JMP67 (ports 1–8) or JMP69 (ports 9–16) or on-board oscillators Y2 (ports 1–8) and Y3 (ports 9–16). Oscillators Y4 and Y5 are auxiliary oscillators for ports 1–8 and ports 9–16, respectively. The clock sources are muxed to the DS26519DK oscillators via FPGAs (see the *ADDRESS MAP* section for details).

3. LINE-SIDE CONNECTIONS

The DS26519DK provides four octal transformers, two stacked RJ48 connectors, and test points to support all 16 ports. The test points are clearly labeled on both sides of the transformers with port numbers.

4. SYSTEM CONNECTORS

System-side signals can be accessed from 16 headers. The headers are clearly labeled with port and signal information.

5. MICROCONTROLLER

The microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS26519 and the FPGAs.

6. POWER-SUPPLY CONNECTORS

Connect a 3.3V power supply across the red J2 and black J4 (GND) banana jacks for normal operation. Banana jack J3 is used by the factory for application of programming voltage for the microcontroller. Diodes D1 and D2 provide protection against power connection reversal. The LED DS1 provides indications that a 3.3V supply is connected properly. The 3.3V supply is regulated to supply proper voltages to various circuits on the board.

7. CONNECTING TO A COMPUTER

Connect a standard DB-9 serial cable between the serial port on the DS26519DK and an available serial port on the host computer. The host computer must be a Windows-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

8. INSTALLING AND RUNNING THE SOFTWARE

ChipView is a general-purpose program that supports a number of Dallas Semiconductor demo kits. To install the ChipView software, run SETUP.EXE from the disk included in the DS26519DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS26519DK.

After installation, run the ChipView program with the DS26519DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Dallas evaluation platforms. In the active subwindow, select the 26519T1.DEF (or 26519E1.DEF) definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS26519's register map. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

9. ADDRESS MAP

Address space begins at 0x81000000. All offsets given in the following tables are relative to 0x81000000.

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named “DS26519DK.DEF.”

Table 9-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000	FPGA	Board identification and clock/signal routing
0X4000	DS26519	DS26519 registers

9.1 FPGA Register Map

Table 9-2. FPGA Register Map for FPGA 0 (U2)

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0100	BID	Read only	Board ID
0X0102	XBIDH	Read only	High Nibble Extended Board ID
0X0103	XBIDM	Read only	Middle Nibble Extended Board ID
0X0104	XBIDL	Read only	Low Nibble Extended Board ID
0X0105	BREV	Read only	Board FAB Revision
0X0106	AREV	Read only	Board Assembly Revision
0X0107	PREV	Read only	FPGA Revision
0X0108	PNUM	Read only	FPGA number
0x010a 0x010b 0x010c 0x010d 0x010e 0x010f 0x0110 0x0111	TCLKnSRC	Control	DS26519 TCLKn Source , Ports 1–8
0X0112	TSERSRC1	Control	DS26519 TSER Source, Ports 1–4
0x0113	TSERSRC2	Control	DS26519 TSER Source, Ports 5–8
0X0114	TSYNCIO	Control	DS26519 TSYNC IO, Ports 1–8
0X0115	RSYNCIO	Control	DS26519 RSYNC IO, Ports 1–8
0x0116	TSYNCSRC1	Control	DS26519 TSYNC Source, Ports 1–4
0x0117	TSYNCSRC2	Control	DS26519 TSYNC Source, Ports 5–8
0x0118	RSYNCSRC1	Control	DS26519 RSYNC source, Ports 1–4
0x0119	RSYNCSRC2	Control	DS26519 RSYNC source, Ports 5–8
0x011a	CLKDIVIDE	Control	Local sync clock divider
0x011b	SYNCSRC	Control	Sync source/Local sync clock source
0x011c	TSYSCLKSRC1	Control	DS26519 TSYSCLK Source, Ports 1–4
0x011d	TSYSCLKSRC2	Control	DS26519 TSYSCLK Source, Ports 5–8
0x011e	RSYSCLKSRC1	Control	DS26519 RSYSCLK Source, Ports 1–4
0X011f	RSYSCLKSRC2	Control	DS26519 RSYSCLK Source, Ports 5–8

Table 9-3. FPGA Register Map for FPGA 1 (U12)

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0000	BID	Read only	Board ID
0X0002	XBIDH	Read only	High Nibble Extended Board ID
0X0003	XBIDM	Read only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read only	Low Nibble Extended Board ID
0X0005	BREV	Read only	Board FAB Revision
0X0006	AREV	Read only	Board Assembly Revision
0X0007	PREV	Read only	FPGA Revision
0X0008	PNUM	Read only	FPGA number
0x000a 0x000b 0x000c 0x000d 0x000e 0x000f 0x0010 0x0011	TCLKnSRC	Control	DS26519 TCLKn Source , Ports 9–16
0X0012	TSERSRC1	Control	DS26519 TSER Source, Ports 9–12
0x0013	TSERSRC2	Control	DS26519 TSER Source, Ports 13–16
0X0014	TSYNCIO	Control	DS26519 TSYNC IO, Ports 9–16
0X0015	RSYNCIO	Control	DS26519 RSYNC IO, Ports 9–16
0x0016	TSYNCSRC1	Control	DS26519 TSYNC Source, Ports 9–12
0x0017	TSYNCSRC2	Control	DS26519 TSYNC Source, Ports 13–16
0x0018	RSYNCSRC1	Conrol	DS26519 RSYNC source, Ports 9–12
0x0019	RSYNCSRC2	Conrol	DS26519 RSYNC source, Ports 13–16
0x001a	CLKDIVIDE	Control	Local sync
0x001b	SYNCSRC	Control	Sync source/Local sync clock source
0x001c	TSYSCLKSRC1	Control	DS26519 TSYSCLK Source, Ports 9–12
0x001d	TSYSCLKSRC2	Control	DS26519 TSYSCLK Source, Ports 13–16
0x001e	RSYSCLKSRC1	Control	DS26519 RSYSCLK Source, Ports 9–12
0X001f	RSYSCLKSRC2	Control	DS26519 RSYSCLK Source, Ports 13–16

Note: The following register descriptions are specific to FPGA0 (U2) but pertain to FPGA1 (U12). The ports that are referenced in the descriptions change from ports 1–8 to ports 9–12. CLOCK1 references change to CLOCK2 (except in the RSYSCLKSRCn and TSYSCLKSRCn register, where CLOCK2 is used as a source in both FPGAs). BPCLK1 reference changes to BPCLK2.

9.2 ID Registers

BID: BOARD ID (Offset = 0X0000)

BID is read-only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)

XBIDH is read-only with a value of 0x0.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)

XBIDM is read-only with a value of 0x2.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)

XBIDL is read-only with a value of 0xa.

BREV: BOARD FAB REVISION (Offset = 0X0005)

BREV is read-only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)

AREV is read-only and displays the current assembly revision.

PREV: FPGA REVISION (Offset = 0X0007)

PREV is read-only and displays the current FPGA code revision.

PNUM: FPGA NUMBER (Offset = 0X0008)

PNUM is read-only and displays the active FPGA number (0 or 1).

9.3 Control Registers

Register Name: **TCLK1SRC**
Register Description: **TCLK1 SOURCE**
Register Offset: **0x010a**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK1 to OSC1_1544. An 0x0F written to this register connects TCLK1 to CLOCK1. A one written to bit RCLKn connects TCLK1 to RCLKn.

Register Name: **TCLK2SRC**
Register Description: **TCLK2 SOURCE**
Register Offset: **0x010b**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK2 to OSC1_1544. An 0x0F written to this register connects TCLK2 to CLOCK1. A one written to bit RCLKn connects TCLK2 to RCLKn.

Register Name: **TCLK3SRC**
Register Description: **TCLK3 SOURCE**
Register Offset: **0x010c**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK3 to OSC1_1544. An 0x0F written to this register connects TCLK3 to CLOCK1. A one written to bit RCLKn connects TCLK3 to RCLKn.

Register Name: **TCLK4SRC**
Register Description: **TCLK4 SOURCE**
Register Offset: **0x010d**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK4 to OSC1_1544. An 0x0F written to this register connects TCLK4 to CLOCK1. A one written to bit RCLKn connects TCLK4 to RCLKn.

Register Name: **TCLK5SRC**
Register Description: **TCLK5 SOURCE**
Register Offset: **0x010e**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK5 to OSC1_1544. An 0x0F written to this register connects TCLK5 to CLOCK1. A one written to bit RCLKn connects TCLK5 to RCLKn.

Register Name: **TCLK6SRC**
Register Description: **TCLK6 SOURCE**
Register Offset: **0x010f**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK6 to OSC1_1544. An 0x0F written to this register connects TCLK6 to CLOCK1. A one written to bit RCLKn connects TCLK6 to RCLKn.

Register Name: **TCLK7SRC**
Register Description: **TCLK7 SOURCE**
Register Offset: **0x0110**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK7 to OSC1_1544. An 0x0F written to this register connects TCLK7 to CLOCK1. A one written to bit RCLKn connects TCLK7 to RCLKn.

Register Name: **TCLK8SRC**
Register Description: **TCLK8 SOURCE**
Register Offset: **0x0111**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

Note: An 0xF0 written to this register connects TCLK8 to OSC1_1544. An 0x0F written to this register connects TCLK81 to CLOCK1. A one written to bit RCLKn connects TCLK8 to RCLKn.

Register Name: **TSERSRC1**
Register Description: **TSER SOURCE 1**
Register Offset: **0x0112**

Bit #	7	6	5	4	3	2	1	0
Name	RSER4	RSER4	RSER3	RSER3	RSER2	RSER2	RSER1	RSER1
Default	0	0	0	0	0	0	0	0

Note: A one written to either bit labeled RSER4, RSER3, RSER2, RSER1 connects TSERn with the respective RSERn pin. If both RSERn bits are written a one, TSERn is driven to a one. If both RSERn bits are written a zero, TSERn is pulled low. For example, 0x03 will drive TSER1 to a one.

Register Name: **TSERSRC2**
Register Description: **TSER SOURCE 2**
Register Offset: **0x0113**

Bit #	7	6	5	4	3	2	1	0
Name	RSER8	RSER8	RSER7	RSER7	RSER6	RSER6	RSER5	RSER5
Default	0	0	0	0	0	0	0	0

Note: A one written to either bit labeled RSER8, RSER7, RSER26, RSER5 connects TSERn with the respective RSERn pin. If both RSERn bits are written a one, TSERn is driven to a one. If both RSERn bits are written a zero, TSERn is pulled low. For example, 0x03 will drive TSER1 to a one.

Register Name: **TSYNCIO**
Register Description: **TSYNC I/O SELECT**
Register Offset: **0x0114**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC8	TSYNC7	TSYNC6	TSYNC5	TSYNC4	TSYNC3	TSYNC2	TSYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit TSYNCn makes the TSYNCn pin an output (driven by TSYNCnO). A zero written to bit TSYNCn makes TSYNCn an input.

Register Name: **RSYNCIO**
Register Description: **RSYNC I/O SELECT**
Register Offset: **0x0115**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC8	RSYNC7	RSYNC6	RSYNC5	RSYNC4	RSYNC3	RSYNC2	RSYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit RSYNCn makes the RSYNCn pin an output (driven by RSYNCnO). A zero written to bit RSYNCn makes RSYNCn an input.

Register Name: **TSYNCSRC1**
Register Description: **TSYNC SOURCE 1**
Register Offset: **0x0116**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC4	SYNC4	RSYNC3	SYNC3	RSYNC2	SYNC2	RSYNC1	SYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects TSYNCnO to a common internal SYNC net. A one written to RSYNCn connects RSYNCn to TSYNCnO. If both RSYNCn and SYNCn are written a one, TSYNCnO is driven to a logic 1. If both RSYNCn and SYNCn are written a zero, TSYNCnO is held at zero.

Register Name: **TSYNCSRC2**
Register Description: **TSYNC SOURCE 2**
Register Offset: **0x0117**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC8	SYNC8	RSYNC7	SYNC7	RSYNC6	SYNC6	RSYNC5	SYNC5
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects TSYNCnO to a common internal SYNC net. A one written to RSYNCn connects RSYNCn to TSYNCnO. If both RSYNCn and SYNCn are written a one, TSYNCnO is driven to a logic 1. If both RSYNCn and SYNCn are written a zero, TSYNCnO is held at zero.

Register Name: **RSYNCSRC1**
Register Description: **RSYNC SOURCE 1**
Register Offset: **0x0118**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC4	SYNC4	TSYNC3	SYNC3	TSYNC2	SYNC2	TSYNC1	SYNC1
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects RSYNCnO to a common internal SYNC net. A one written to TSYNCn connects TSYNCn to RSYNCnO. If both TSYNCn and SYNCn are written a one, RSYNCnO is driven to a logic 1. If both TSYNCn and SYNCn are written a zero, RSYNCnO is held at zero.

Register Name: **RSYNCSRC2**
Register Description: **RSYNC SOURCE 2**
Register Offset: **0x0119**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC8	SYNC8	TSYNC7	SYNC7	TSYNC6	SYNC6	TSYNC5	SYNC5
Default	0	0	0	0	0	0	0	0

Note: A one written to bit SYNCn connects RSYNCnO to a common internal SYNC net. A one written to TSYNCn connects TSYNCn to RSYNCnO. If both TSYNCn and SYNCn are written a one, RSYNCnO is driven to a logic 1. If both TSYNCn and SYNCn are written a zero, RSYNCnO is held at zero.

Register Name: **CLKDIVIDE**
Register Description: **SYNC CLOCK DIVIDER**
Register Offset: **0x011a**

Bit #	7	6	5	4	3	2	1	0
Name	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

Note: The SYNC SOURCE clock is divided by the value in this register to provide a local sync. For instance, for T1 a divisor of 193 is appropriate (C1H)

Register Name: **SYNCSRC**
Register Description: **LOCAL SYNC CLOCK SOURCE AND NET SYNC SOURCE**
Register Offset: **0x011b**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC1	RSYNC1	LOCAL	LOCAL	BPCLK1	OSC1	CLOCK1	CLOCK1
Default	0	0	0	0	0	0	0	0

Note: A one written to the upper nibble connects internal net (sync) to respective source. A one written lower nibble connects local sync generator to respective clock. Bit named LOCAL is a locally generated sync.

Register Name: **TSYSCLKSRC1**
Register Description: **TSYSCLK SOURCE 1**
Register Offset: **0x011c**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to TSYSCLK4, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to TSYSCLK3, TSYSCLK2, and TSYSCLK1, respectively. CLOCK2 comes from FPGA1.

Register Name: **TSYSCLKSRC2**
Register Description: **TSYSCLK SOURCE 2**
Register Offset: **0x011d**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to TSYSCLK8, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to TSYSCLK7, TSYSCLK6, and TSYSCLK5, respectively. CLOCK2 comes from FPGA1.

Register Name: **RSYSCLKSRC1**
Register Description: **RSYSCLK SOURCE 1**
Register Offset: **0x011e**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to RSYSCLK4, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to RSYSCLK3, RSYSCLK2, and RSYSCLK1, respectively. CLOCK2 comes from FPGA1.

Register Name: **RSYSCLKSRC2**
Register Description: **RSYSCLK SOURCE 2**
Register Offset: **0x011f**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

Note: A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to RSYSCLK8, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to RSYSCLK7, RSYSCLK6, and RSYSCLK5, respectively. CLOCK2 comes from FPGA1.

10. ADDITIONAL INFORMATION/RESOURCES

10.1 DS26519 Information

For more information about the DS26519, refer to the DS26519 data sheet at www.maxim-ic.com/DS26519.

10.2 DS26519DK Information

For more information about the DS26519DK including software downloads, refer to the DS26519DK Quick View page at www.maxim-ic.com/DS26519DK.

10.3 Technical Support

For additional technical support, go to www.maxim-ic.com/support.

11. COMPONENT LIST

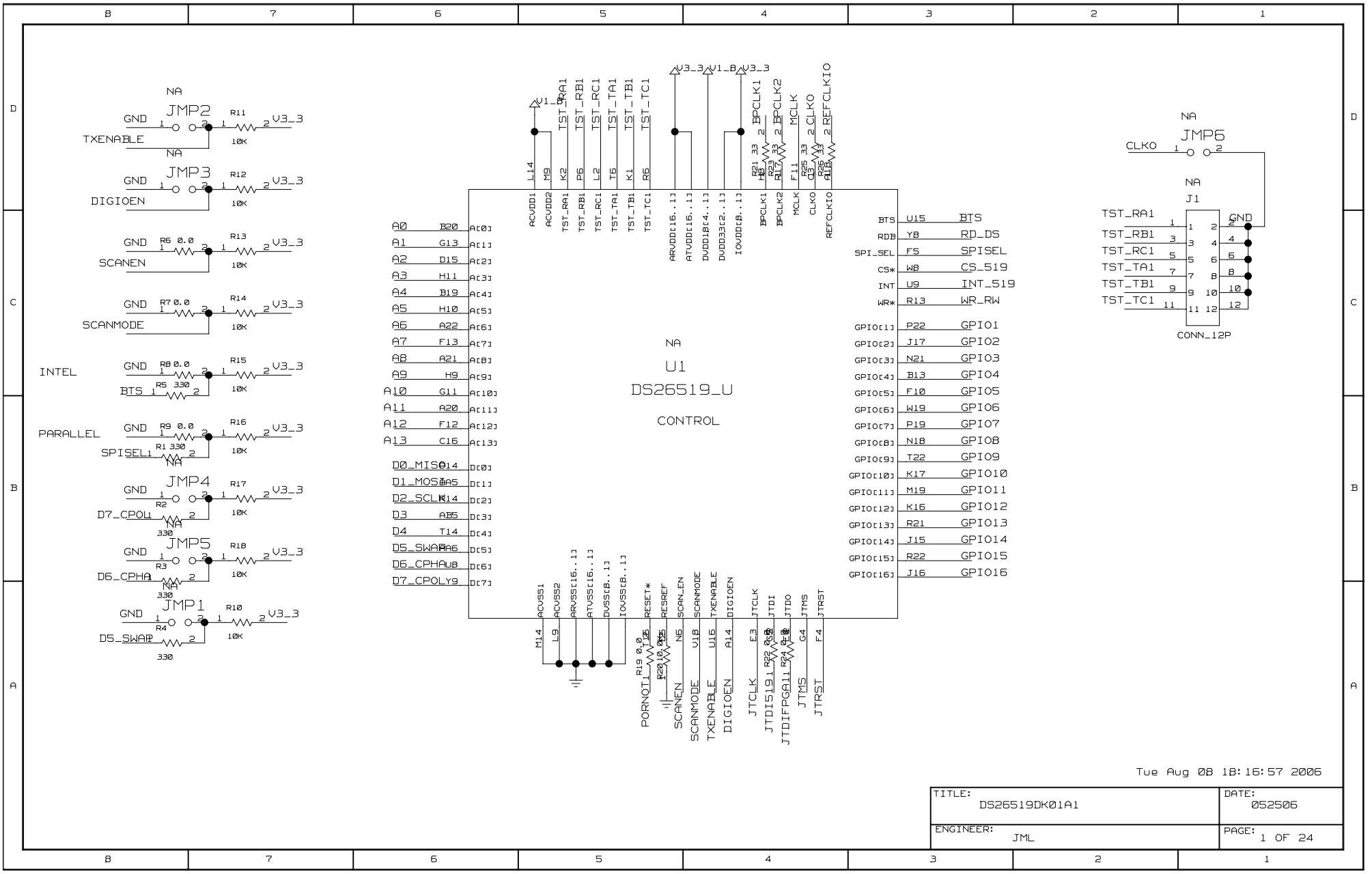
DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C174, C175	2	L_0603 CERAM 22pF 25V 5% NPO	AVX	06033A220JAT
C19, C20, C21, C24–C30, C32–C73, C75–C78, C80–C97, C99–C102, C104–C172, C193–C195	150	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
Y2–Y5	4	SOCKET, OSCILLATOR, HALF SIZE, 4-PIN THROUGH-HOLE	ARI	110880
J4	1	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	MSR	164-6218
J2, J3	2	SOCKET, BANANA PLUG, HORIZONTAL, RED	MSR	164-6219
D1, D2	2	DIODE 1A 50V GEN PURPOSE SILICON	GEN	1N4001
J13	1	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
R6–R9, R19, R22, R24, R75–R90, R95–R115, R134, R143, R144, R146, R148–R163, R168–R199, R204–R223, R237–R257, R262–R277	153	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F
U6, U7	2	IC, SRAM, 128K X 8, 32 PIN SOIC	CYP	CY62128VL-70SC
U11	1	DUAL RS232 XMITR/RCVR 16 PIN SOIC (300 MIL)	DAL	DS232AS
Y1	1	XTAL, LOW PROFILE, 8.000MHZ	ECL	EC1-8.000M
C1–C4, C181–C192	16	0805 CERAM 560pF 50V 5% NPO	PAN	ECJ-2VC1H561K
C7,C8	2	1206 CERAM 6.8uF 6.3V 10% X5R	PAN	ECJ-3YB0J685K
C10–C18, C22, C23, C31, C74, C79, C98, C103, C176–C180	21	L_1206 CERAM 10uF 10V 20%	PAN	ECJ-3YB1A106M
C5,C6	2	1206 CERAM 4.7uF 25V 10% X5R	PAN	ECJ-3YB1E475K
C9	1	L_D CASE TANT 68uF 16V 20%	PAN	ECS-T1CD686R
C173	1	L_B CASE TANT 10uF 16V 20%	PAN	ECS-T1CX106R
R20	1	RES 0603 10.0K Ohm 1/16W 1%	PAN	ERJ-3EKF1002V
R91–R94, R164–R167, R200–R203, R258–R261	16	RES 0603 121 Ohm 1/16W 1%	PAN	ERJ-3EKF1210V
R120	1	RES 0603 33.2 Ohm 1/16W 1%	PAN	ERJ-3EKF33R2V
R232, R233	2	L_RES 0603 51.1 Ohm 1/16W 1%	PAN	ERJ-3EKF51R1V
R119, R278, R280, R284, R286, R290, R292, R296, R298, R302, R304, R310, R312, R316, R318, R322, R324	17	L_RES 0603 1.0K Ohm 1/16W 5%	PAN	ERJ-3GEYJ102V
R10–R18, R118, R121–R132, R135–R138, R140–R142, R145, R279, R281, R285, R287, R291, R293, R297, R299, R303, R305, R306, R311, R313, R317, R319, R323, R325	47	L_RES 0603 10K Ohm 1/16W 5%	PAN	ERJ-3GEYJ103V

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R139	1	RES 0603 1.0M Ohm 1/16W 5%	PAN	ERJ-3GEYJ105V
R21, R23, R25, R26, R28–R74, R224–R231, R328	60	L_RES 0603 33 Ohm 1/16W 5%	PAN	ERJ-3GEYJ330V
R1–R5, R116, R117, R282, R283, R288, R289, R294, R295, R300, R301, R307–R309, R314, R315, R320, R321, R326, R327	24	L_RES 0603 330 Ohm 1/16W 5%	PAN	ERJ-3GEYJ331V
R234	1	RES 0603 3.3K Ohm 1/16W 5%	PAN	ERJ-3GEYJ332V
R235, R236	2	RES 0603 4.7K Ohm 1/16W 5%	PAN	ERJ-3GEYJ472V
SW2	1	L_SWITCH MOM 4PIN SINGLE POLE	PAN	EVQPAE04M
J12	1	HEADER, 14 PIN, DUAL ROW, VERT	STC	HDR-TSW-107-14-T-D
J5–J11, J15–J23	16	HEADER, 20 PIN, DUAL ROW, VERT	STC	HDR-TSW-110-14-T-D
DS1, DS2	2	LED, RED, SMD	PAN	LN1251C
DS3–DS19	17	L_LED, RED, SMD	PAN	LN1251C
U3	1	L_IC, LINEAR REGULATOR, 1.5W, 1.8V OR ADJ, 1A, 16 PIN TSSOP-EP	MAX	MAX1793EUE-18
U4	1	IC, LINEAR REGULATOR, 1.5W, 2.5V OR ADJ, 1A, 16 PIN TSSOP-EP	MAX	MAX1793EUE-25
U9	1	IC, OPEN DRAIN MICROPROCESSOR RESET CKT, 3.08V 140MS, 4PIN SOT143	MAX	MAX6315US31D3-T
U10	1	MICROPROCESSOR RESET CIRCUITS, 3.08V RESET, 3 PIN SC70	MAX	MAX803TEXR-T
U8	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	MAX	MAX811TEUS-T
U5	1	IC, MCORE MICROCONTROLLER, 144 PIN LQFP	MOT	MMC2107PV
JMP7–JMP66, JMP71–JMP106	96	DO NOT PLACE, OPEN 2PIN TH JUMPER	NA	NA
R133, R147	2	RES 0603 DO NOT POPULATE	NA	NA
TP1–TP28, TP37–TP48, TP50	41	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U13–U16, U18–U34	21	L_TINYLOGIC HIGH SPEED 2-INPUT OR GATE, 5 PIN SOT23	FAI	NC7SZ32M5
J1	1	L_CONN, 12 PIN, DUAL ROW, VERT	SUL	PTC06DAAN
J24, J25	2	CONNECTOR, STACKED OCTAL JACK, 64-PIN, SHIELDED	MOL	SD-44520-001
U1	1	SOCKET, SURFACE MOUNT, BGA, 484P, 1MM	IRO	SG-BGA-6120
SW1	1	L_SWITCH, SPDT SLIDE, 3PIN TH	TYC	SSA12
JMP1–JMP6, JMP67, JMP69	8	L_2 PIN HEADER, .100 CENTERS, VERTICAL	STC	TSW-102-07-T-S
JMP68, JMP70	2	L_HEADER, 3-PIN, .100 CENTERS, VERTICAL	STC	TSW-103-07-T-S
J14	1	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	STC	TSW-105-07-T-D
T1–T4	4	XFMR, XMIT/RCV, 1 TO 2 AND 1 TO 1, SMT 32 PIN	PUL	TX1475

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
L1	1	INDUCTOR 1.0uH 2PIN SMT 20%	COT	UP1B-1R0
U2, U12	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	XIL	XC2S50-5FG256C
U17	1	IC, PLATFORM FLASH IN-SYS PROG CONFIG PROM, 2MBIT, 20 PIN TSSOP	XIL	XCF02SVO20C

12. SCHEMATICS

The schematics are featured in the following pages.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JMP3
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V3_3
GND
R6 0.0
SCANEN
R13
10K
V3_3
GND
R7 0.0
SCANMODE
R14
10K
V3_3
INTEL
GND
R8 0.0
BTS
R5 330
R15
10K
V3_3
PARALLEL
GND
R9 0.0
SPISEL
R1 330
NA
R16
10K
V3_3
JMP4
GND
R2
D7_CPOL
NA
330
R17
10K
V3_3
JMP5
GND
R3
D6_CPHA
NA
330
R18
10K
V3_3
JMP1
GND
R4
D5_SWAP
330
R10
10K
V3_3
V1_8
V3_3
TST_RA1
TST_RB1
TST_RC1
TST_TA1
TST_TB1
TST_TC1
BPCLK1
BPCLK2
MCLK
CLKO
REFCLKIO
ACVDD1
ACVDD2
ARVDDt16..1]
ATVDDt16..1]
DVDD18t4..1]
DVDD33t2..1]
IOVDDt8..1]
BPCLK1
BPCLK2
MCLK
CLKO
REFCLKIO
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
D0_MISO
D1_MOSI
D2_SCLK
D3
D4
D5_SWAP
D6_CPHA
D7_CPOL
NA
U1
DS26519_U
CONTROL
BTS
RDB
SPI_SEL
CS*
INT
WR*
GPIO[1]
GPIO[2]
GPIO[3]
GPIO[4]
GPIO[5]
GPIO[6]
GPIO[7]
GPIO[8]
GPIO[9]
GPIO[10]
GPIO[11]
GPIO[12]
GPIO[13]
GPIO[14]
GPIO[15]
GPIO[16]
BTS
RD_DS
SPISEL
CS_519
INT_519
WR_RW
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
ACVSS1
ACVSS2
ARVSSt16..1]
ATVSSt16..1]
DVSSt8..1]
IOVSSt8..1]
RESET*
RESREF
SCAN_EN
SCANMODE
TXENABLE
DIGIOEN
JTCLK
JTDI519
JTDIFPGA
JTDO
JTMS
JTRST
PORNOT
R19 0.0
R20 10.0K
SCANEN
R22 0.0
R24 0.0
NA
JMP6
CLKO
NA
J1
TST_RA1
TST_RB1
TST_RC1
TST_TA1
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TST_TC1
GND
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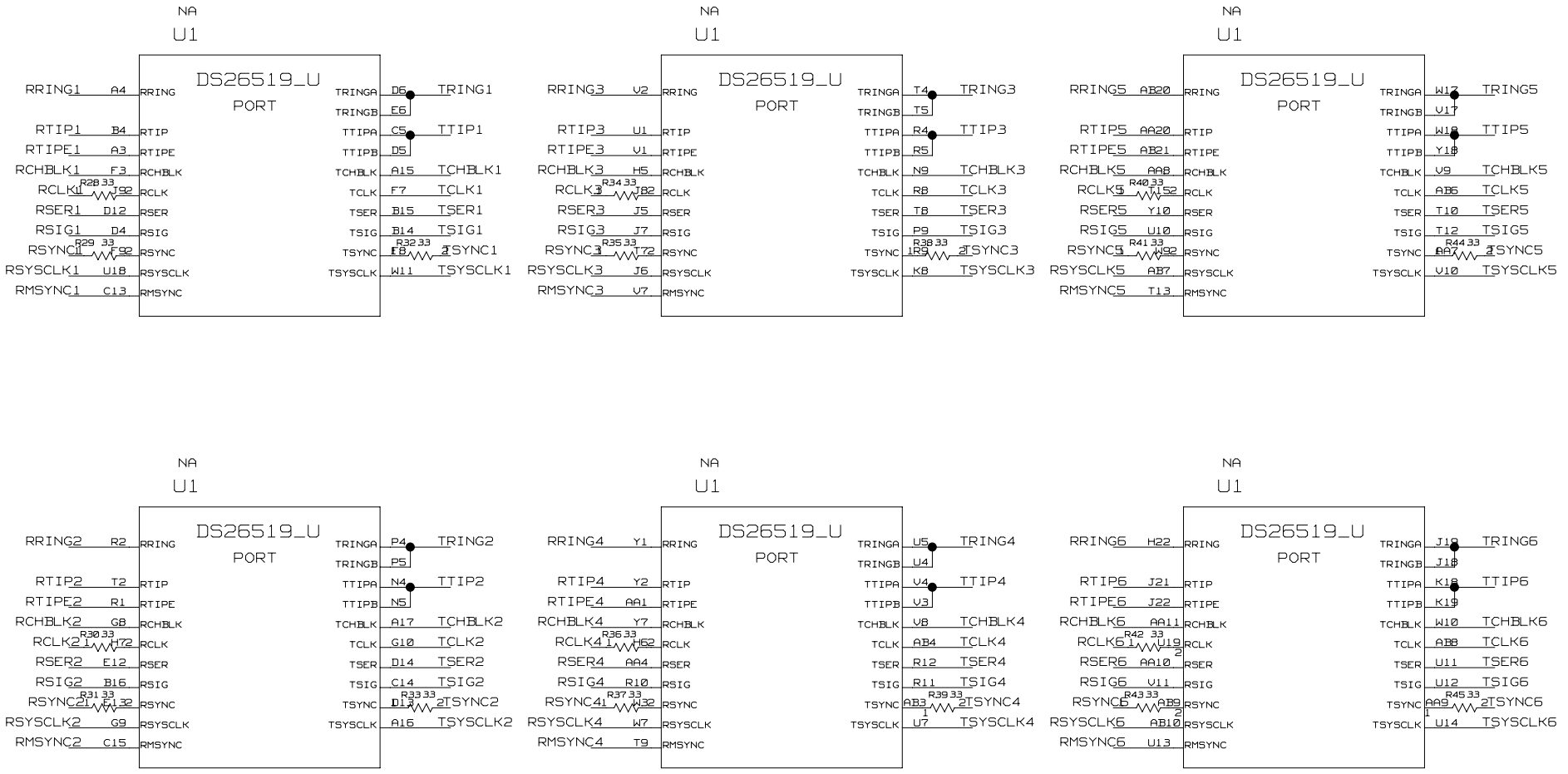

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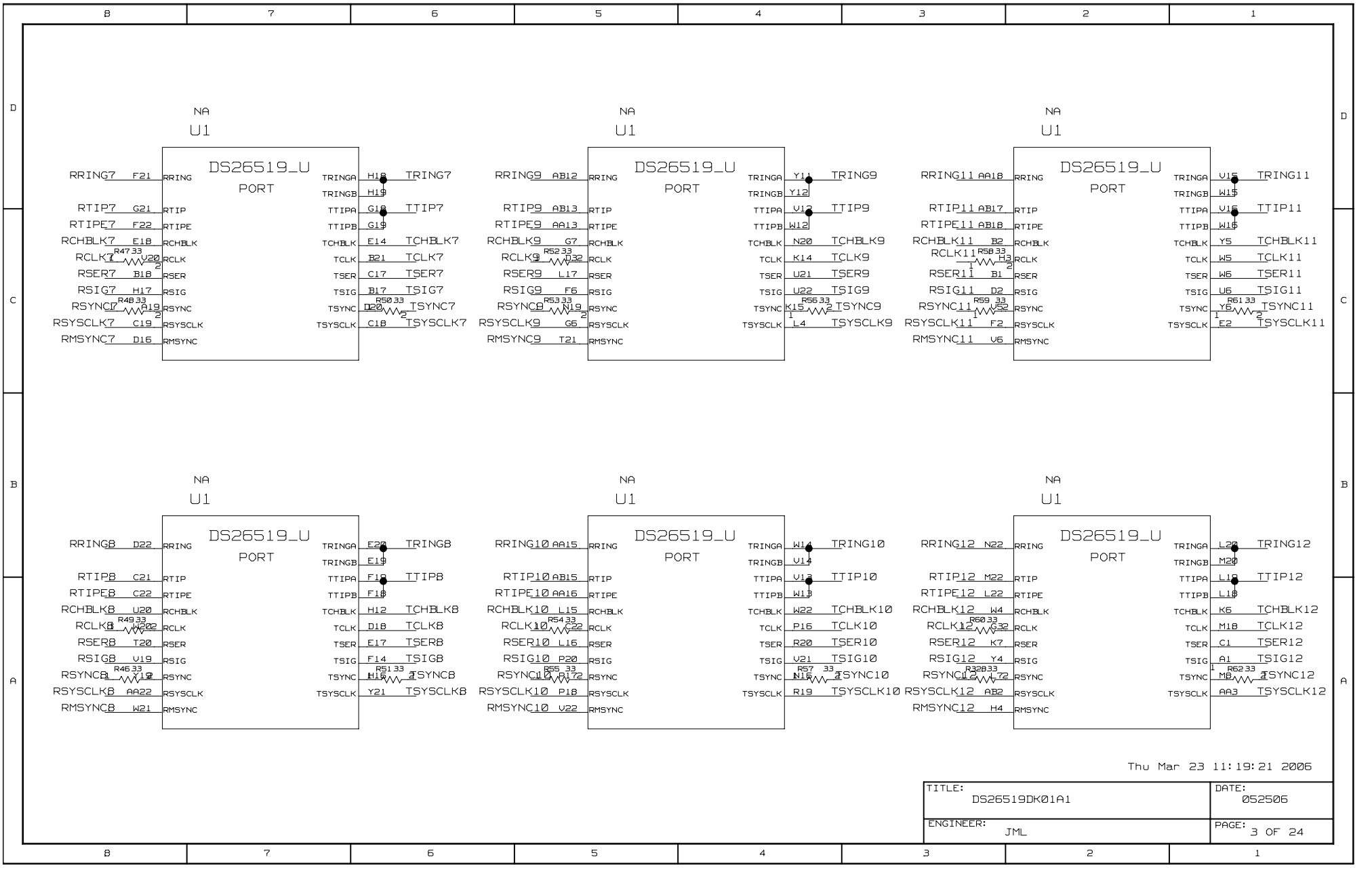
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RTIP7 G21 RTIP
RTIPE7 F22 RTIPE
RCHBLK7 E18 RCHBLK
RCLK7 R47 33 V20 RCLK
RSER7 B18 RSER
RSIG7 H17 RSIG
RSYNC7 R48 33 A19 RSYNC
RSYSCLK7 C19 RSYSCLK
RMSYNC7 D16 RMSYNC
TRINGA H18 TRING7
TRINGB H19
TTIPA G18 TTIP7
TTIPB G19
TCHBLK E14 TCHBLK7
TCLK B21 TCLK7
TSER C17 TSER7
TSIG B17 TSIG7
TSYNC R50 33 D20 TSYNC7
TSYSCLK C18 TSYSCLK7
NA
U1
DS26519_U
PORT
RRING9 AB12 RRING
RTIP9 AB13 RTIP
RTIPE9 AA13 RTIPE
RCHBLK9 G7 RCHBLK
RCLK9 R52 33 J3 RCLK
RSER9 L17 RSER
RSIG9 F6 RSIG
RSYNC9 R53 33 N19 RSYNC
RSYSCLK9 G5 RSYSCLK
RMSYNC9 T21 RMSYNC
TRINGA Y11 TRING9
TRINGB Y12
TTIPA V13 TTIP9
TTIPB W12
TCHBLK N20 TCHBLK9
TCLK K14 TCLK9
TSER U21 TSER9
TSIG U22 TSIG9
TSYNC R56 33 K15 TSYNC9
TSYSCLK L4 TSYSCLK9
NA
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DS26519_U
PORT
RRING11 AA18 RRING
RTIP11 AB17 RTIP
RTIPE11 AB18 RTIPE
RCHBLK11 B2 RCHBLK
RCLK11 R58 33 H3 RCLK
RSER11 B1 RSER
RSIG11 D2 RSIG
RSYNC11 R59 33 J2 RSYNC
RSYSCLK11 F2 RSYSCLK
RMSYNC11 V6 RMSYNC
TRINGA V15 TRING11
TRINGB W15
TTIPA V16 TTIP11
TTIPB W16
TCHBLK Y5 TCHBLK11
TCLK W5 TCLK11
TSER W6 TSER11
TSIG U6 TSIG11
TSYNC R61 33 Y6 TSYNC11
TSYSCLK E2 TSYSCLK11
NA
U1
DS26519_U
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RTIP8 C21 RTIP
RTIPE8 C22 RTIPE
RCHBLK8 U20 RCHBLK
RCLK8 R49 33 W20 RCLK
RSER8 T20 RSER
RSIG8 V19 RSIG
RSYNC8 R46 33 Y19 RSYNC
RSYSCLK8 AA22 RSYSCLK
RMSYNC8 W21 RMSYNC
TRINGA E20 TRING8
TRINGB E19
TTIPA F18 TTIP8
TTIPB F18
TCHBLK H12 TCHBLK8
TCLK D18 TCLK8
TSER E17 TSER8
TSIG F14 TSIG8
TSYNC R51 33 H15 TSYNC8
TSYSCLK Y21 TSYSCLK8
NA
U1
DS26519_U
PORT
RRING10 AA15 RRING
RTIP10 AB15 RTIP
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RCLK10 R54 33 C22 RCLK
RSER10 L16 RSER
RSIG10 P20 RSIG
RSYNC10 R55 33 P17 RSYNC
RSYSCLK10 P18 RSYSCLK
RMSYNC10 V22 RMSYNC
TRINGA W14 TRING10
TRINGB V14
TTIPA V18 TTIP10
TTIPB W13
TCHBLK W22 TCHBLK10
TCLK P16 TCLK10
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TSIG V21 TSIG10
TSYNC R57 33 N16 TSYNC10
TSYSCLK R19 TSYSCLK10
NA
U1
DS26519_U
PORT
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RTIP12 M22 RTIP
RTIPE12 L22 RTIPE
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RSER12 K7 RSER
RSIG12 Y4 RSIG
RSYNC12 R328 33 L72 RSYNC
RSYSCLK12 AB2 RSYSCLK
RMSYNC12 H4 RMSYNC
TRINGA L20 TRING12
TRINGB M20
TTIPA L18 TTIP12
TTIPB L18
TCHBLK K6 TCHBLK12
TCLK M18 TCLK12
TSER C1 TSER12
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TSYNC R62 33 M8 TSYNC12
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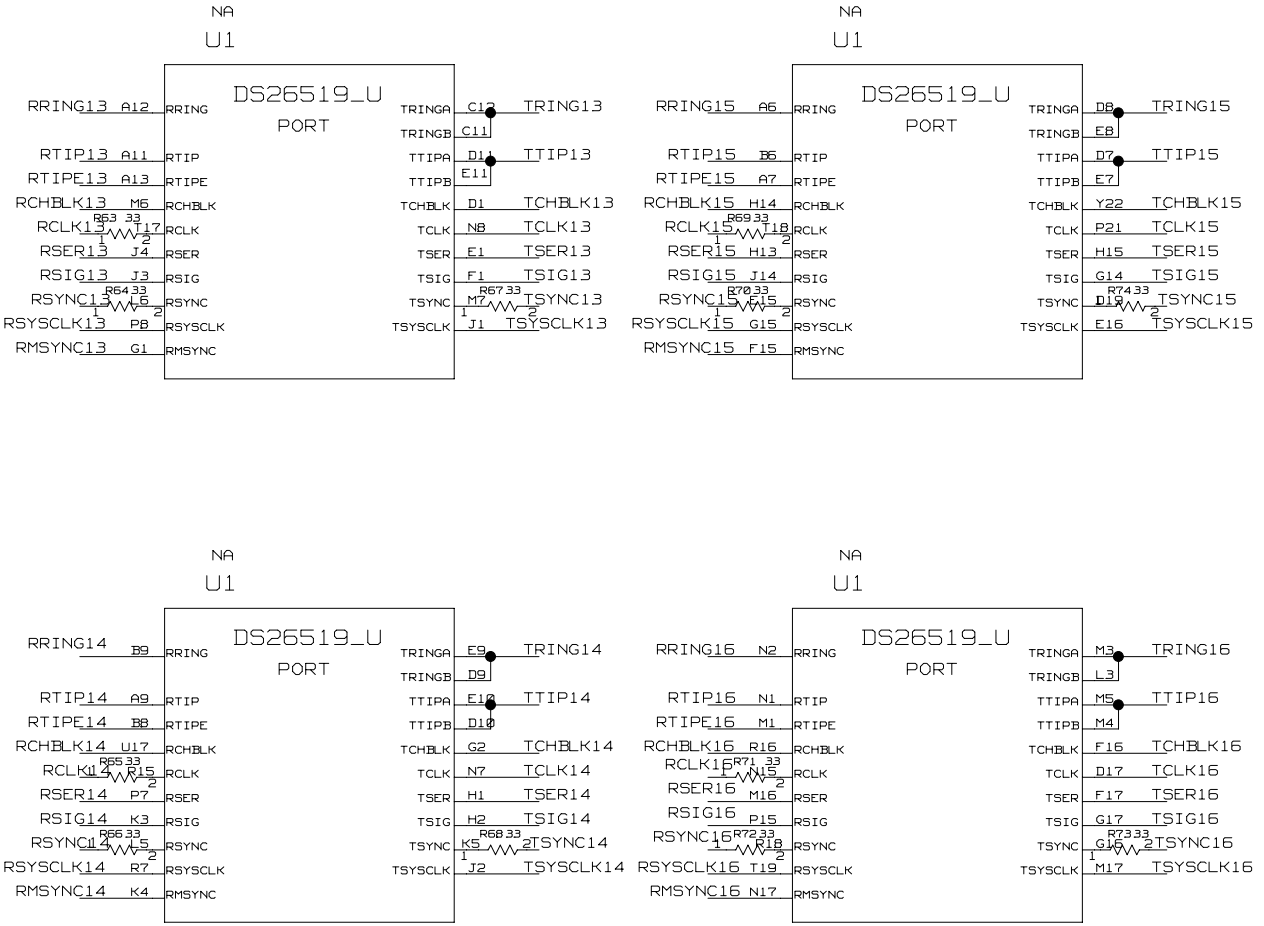

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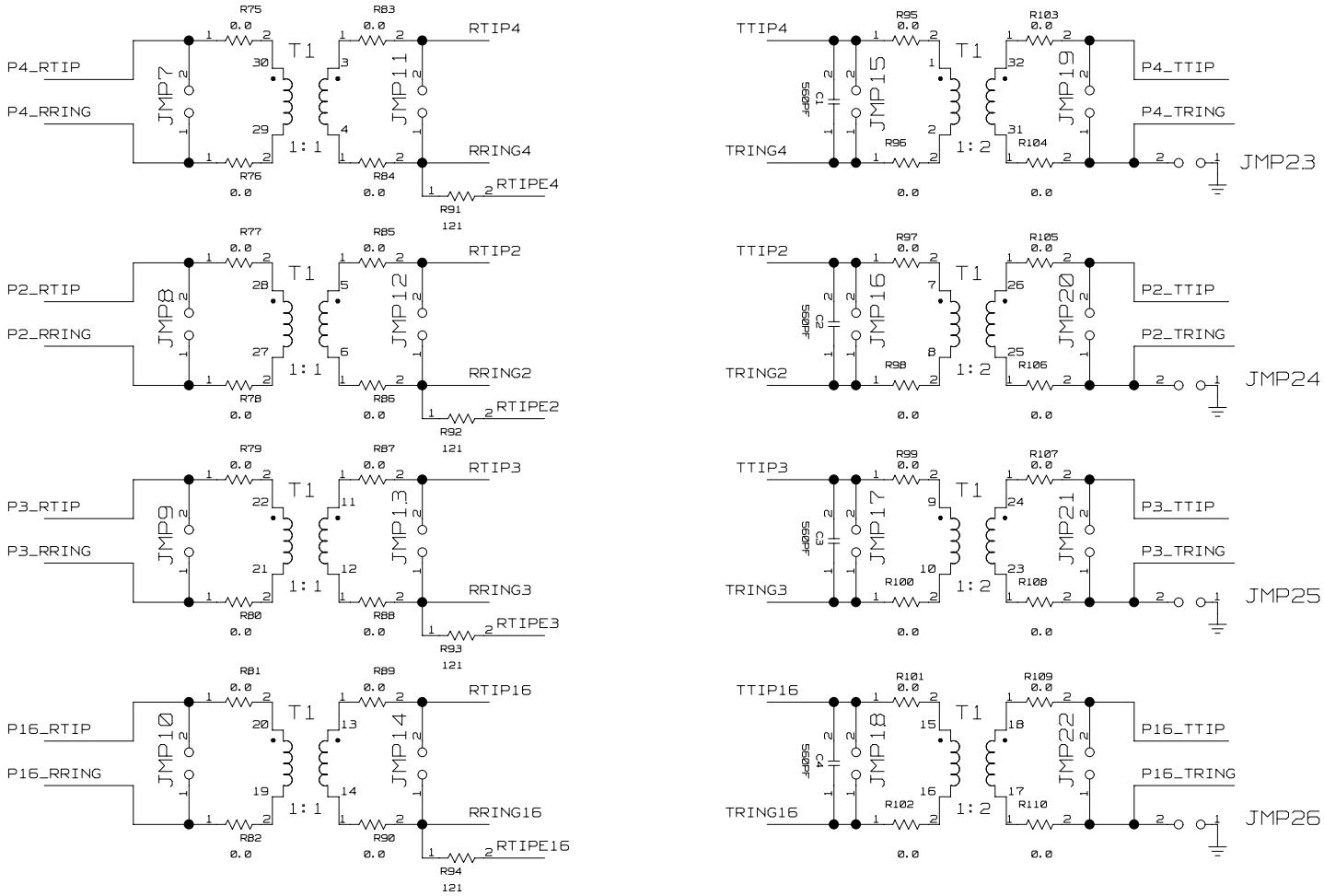

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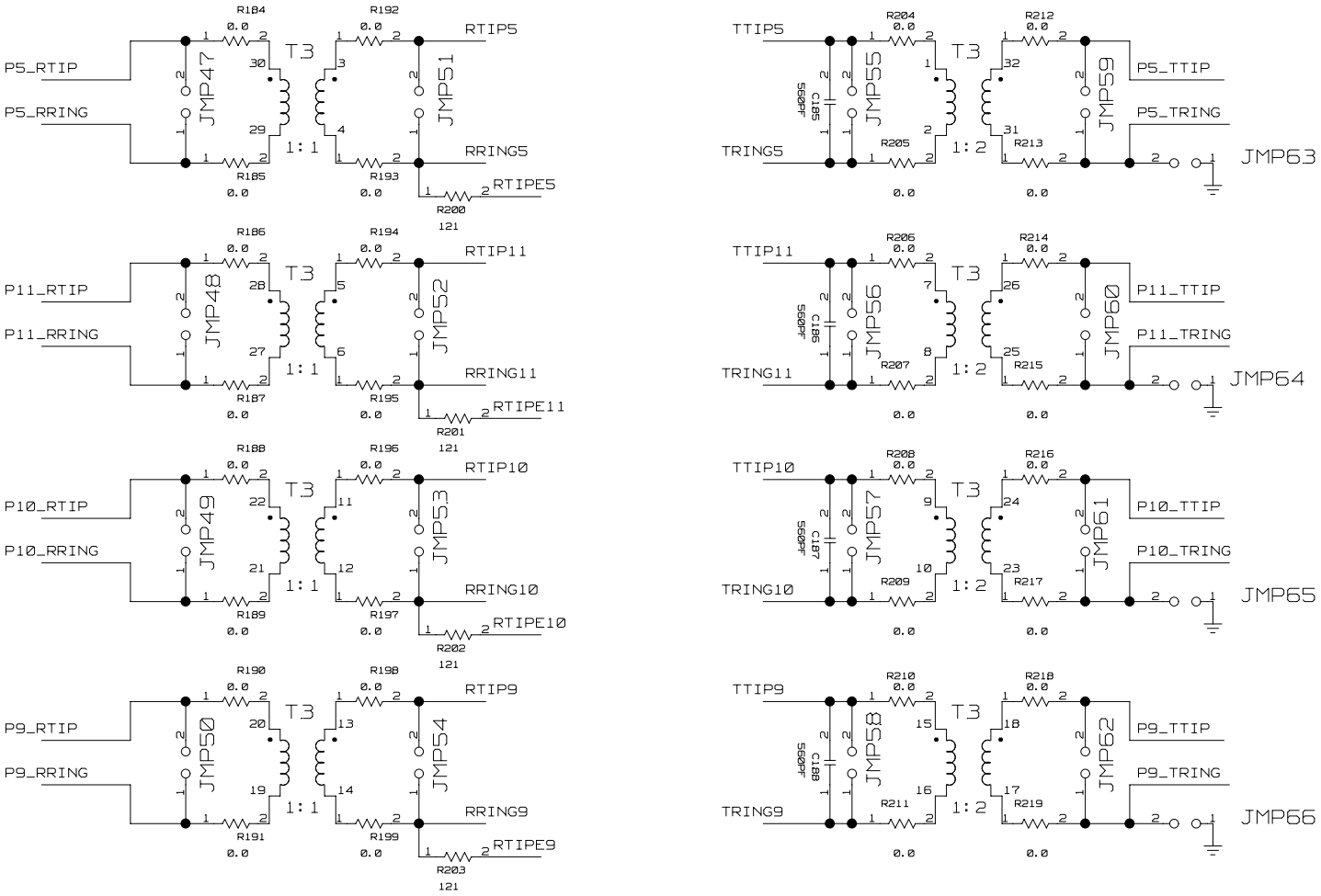

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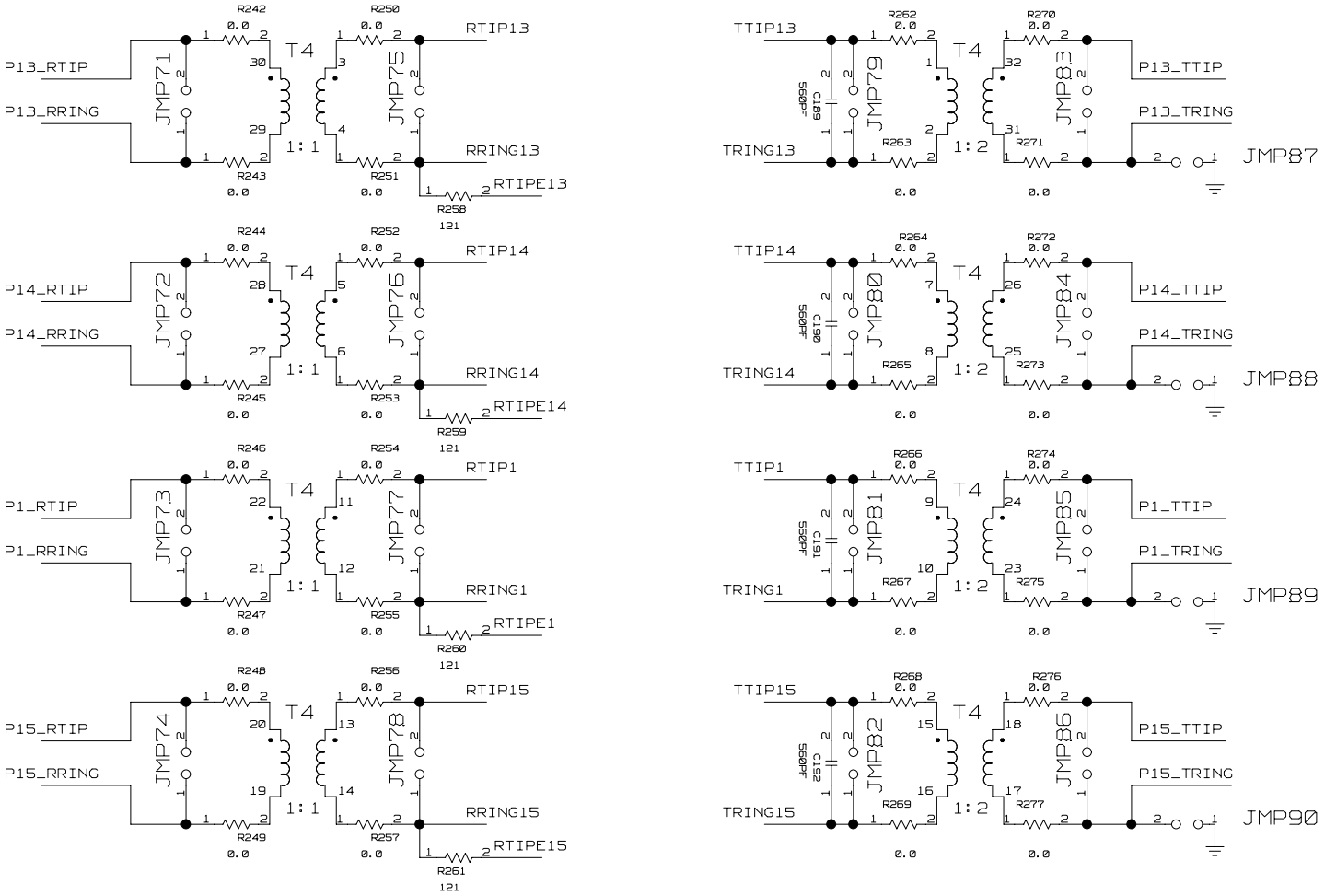

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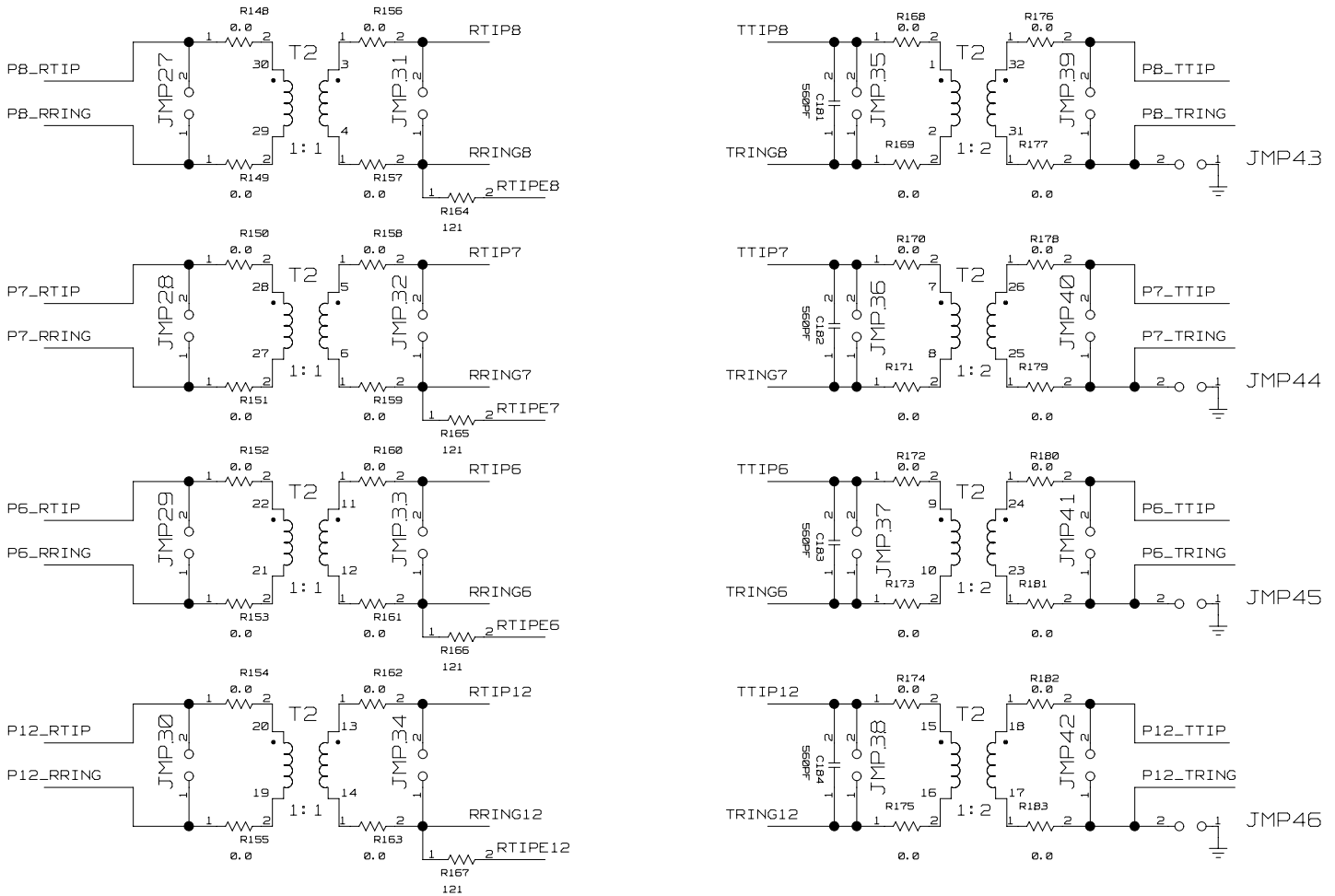

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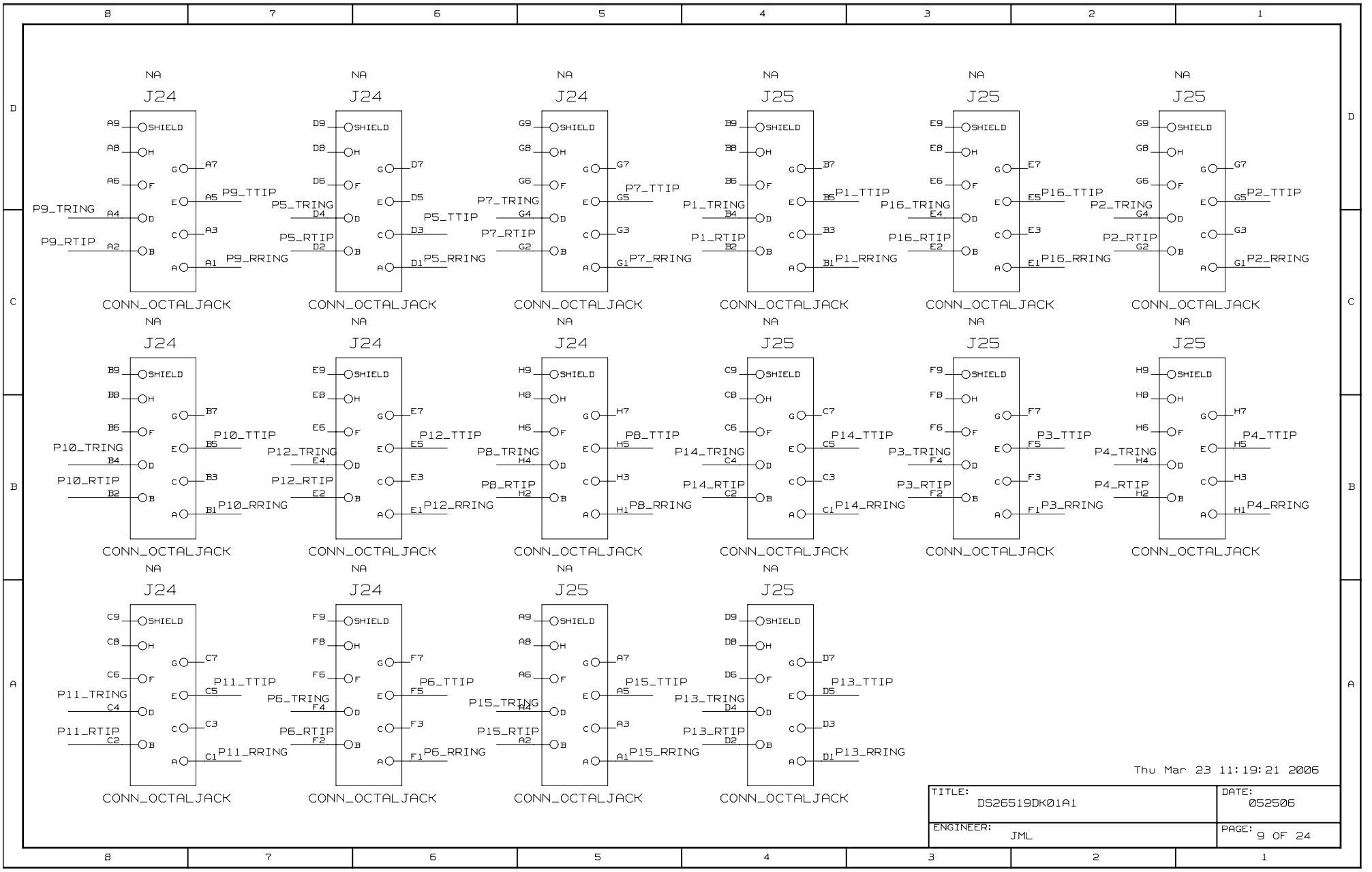

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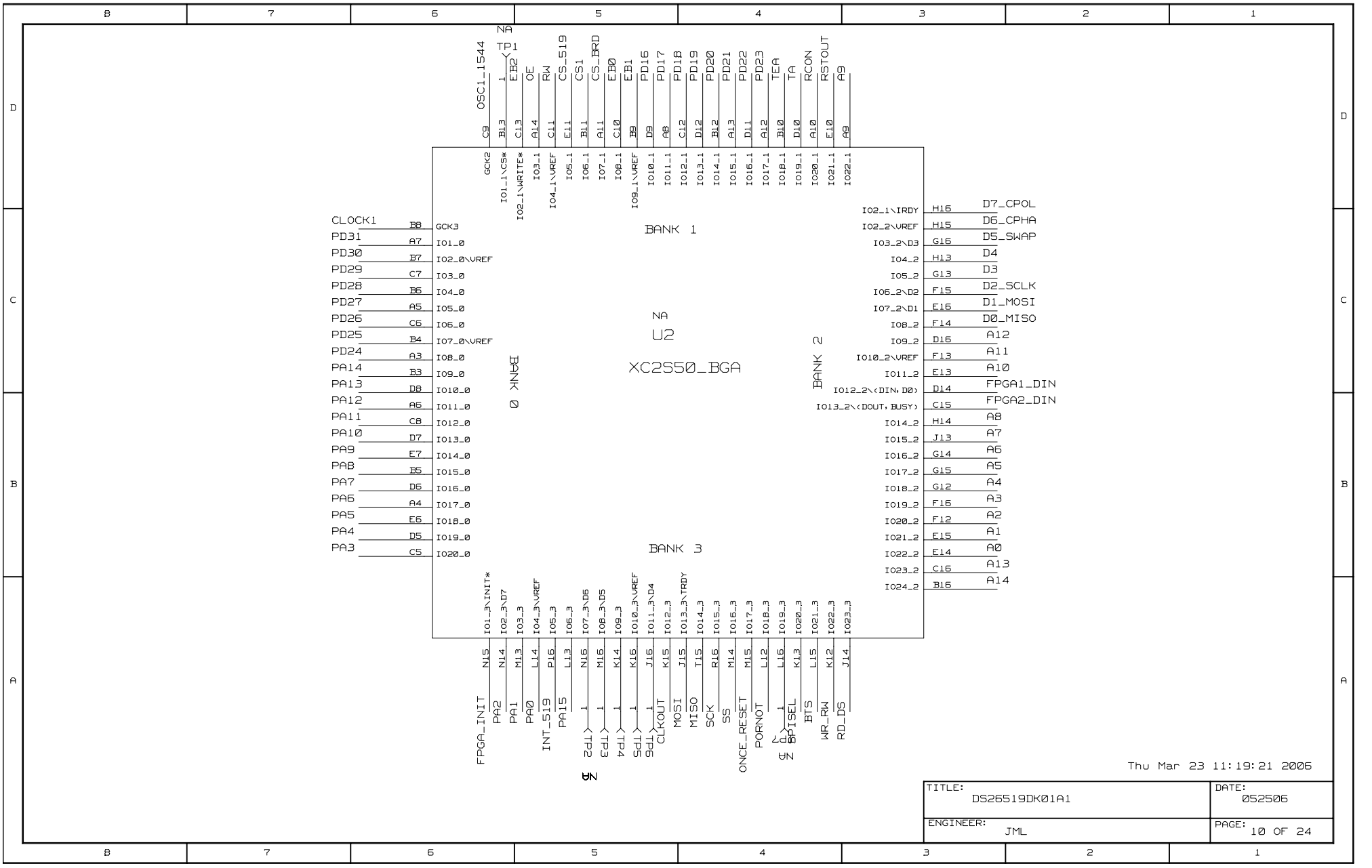

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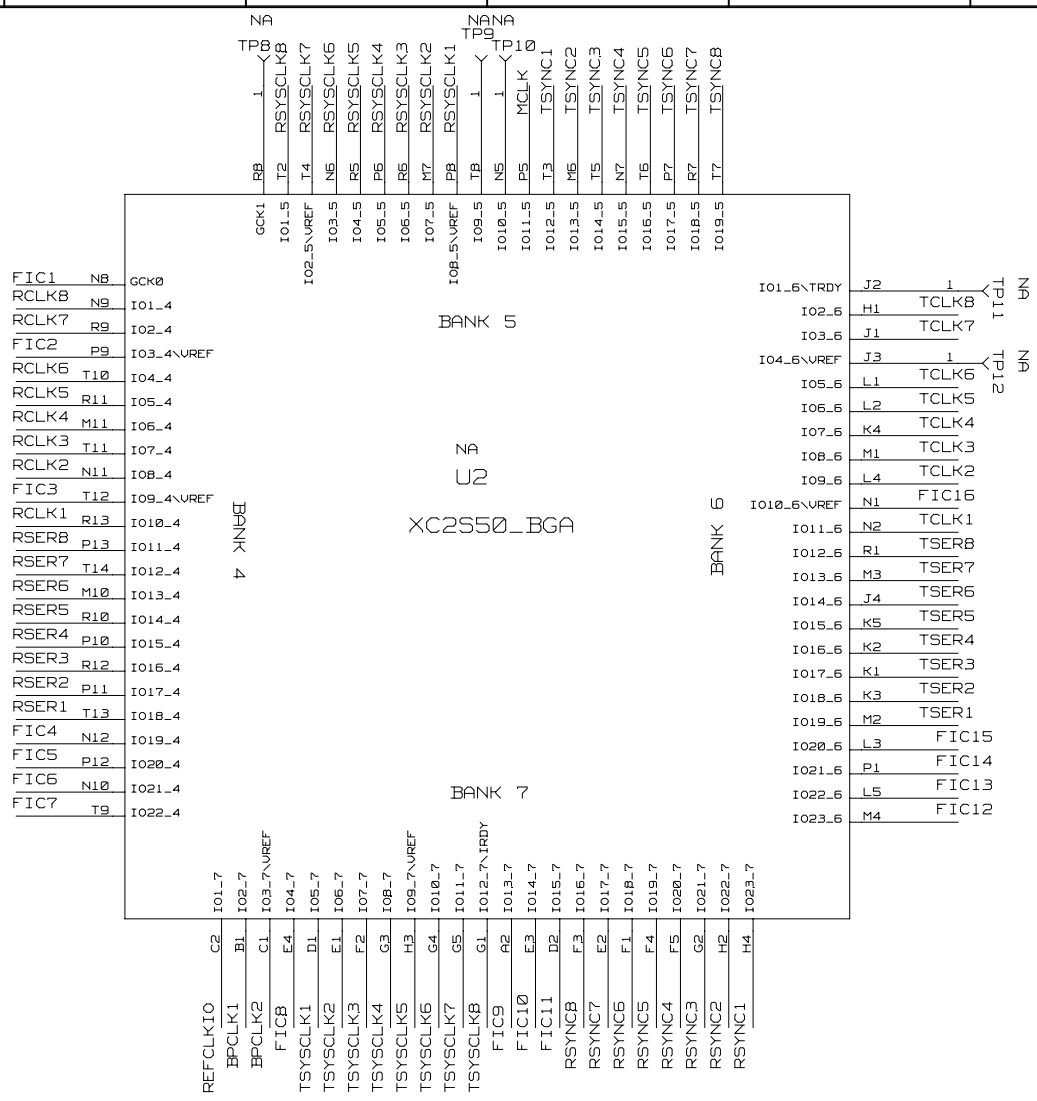

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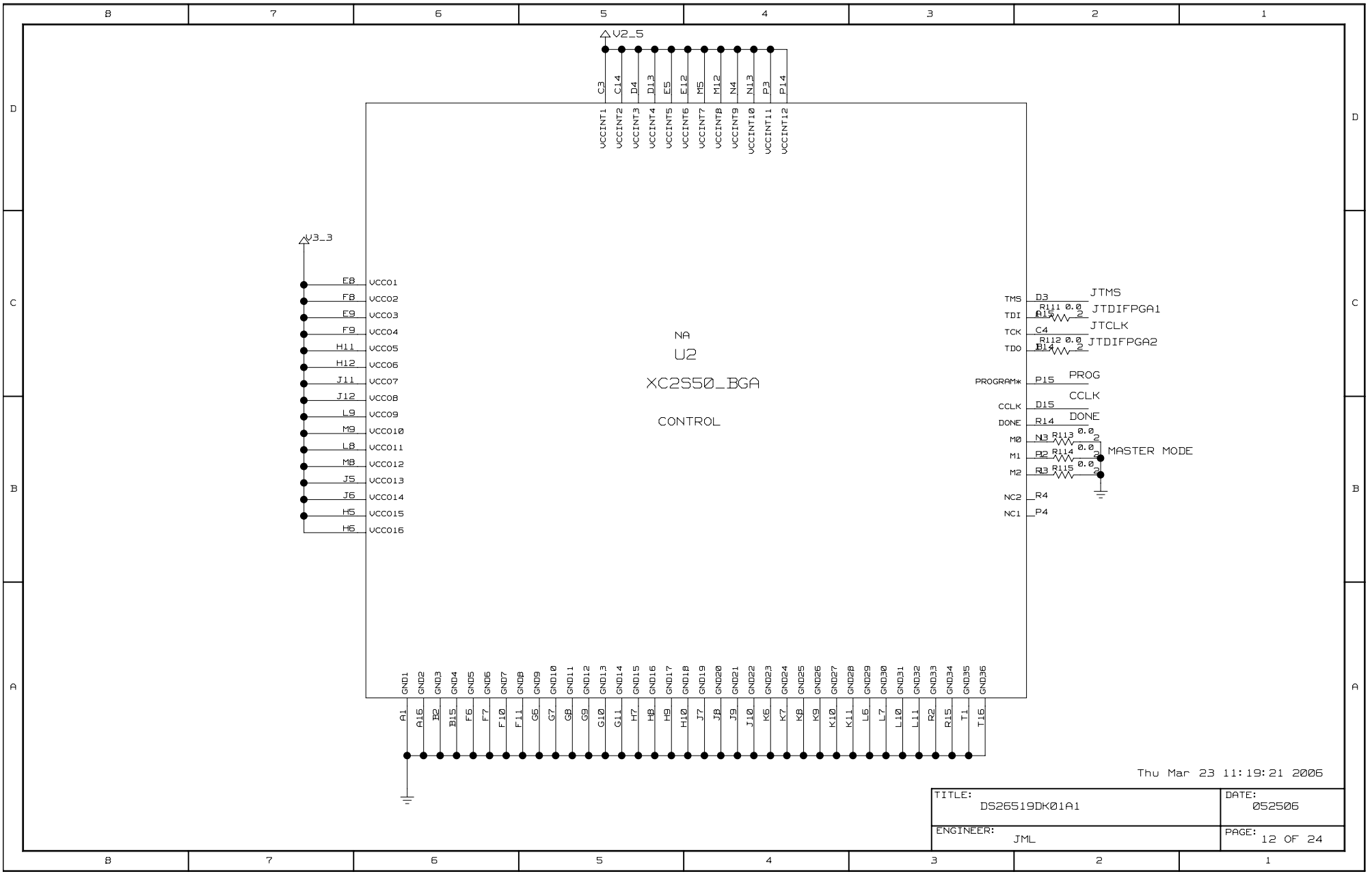

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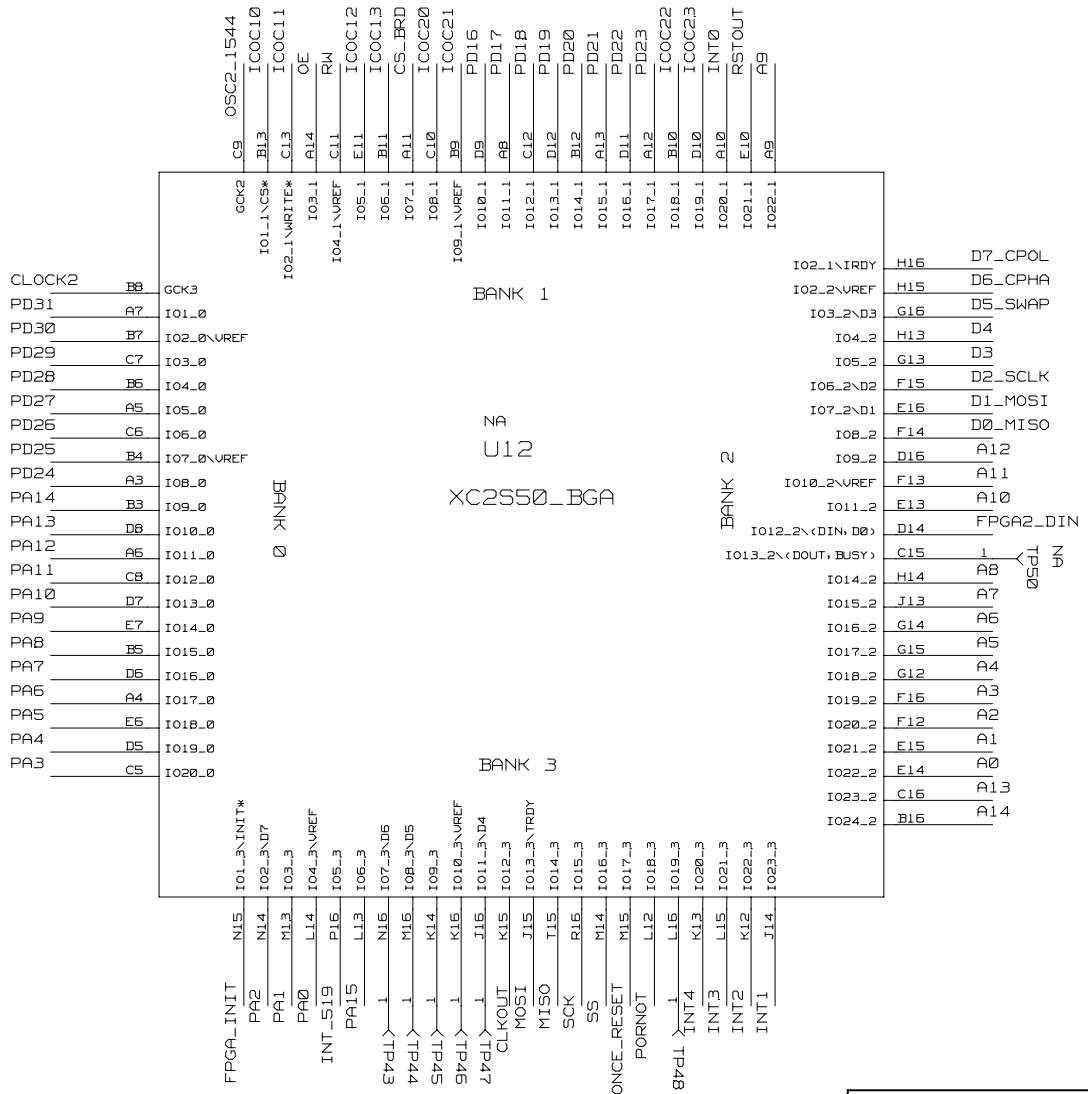

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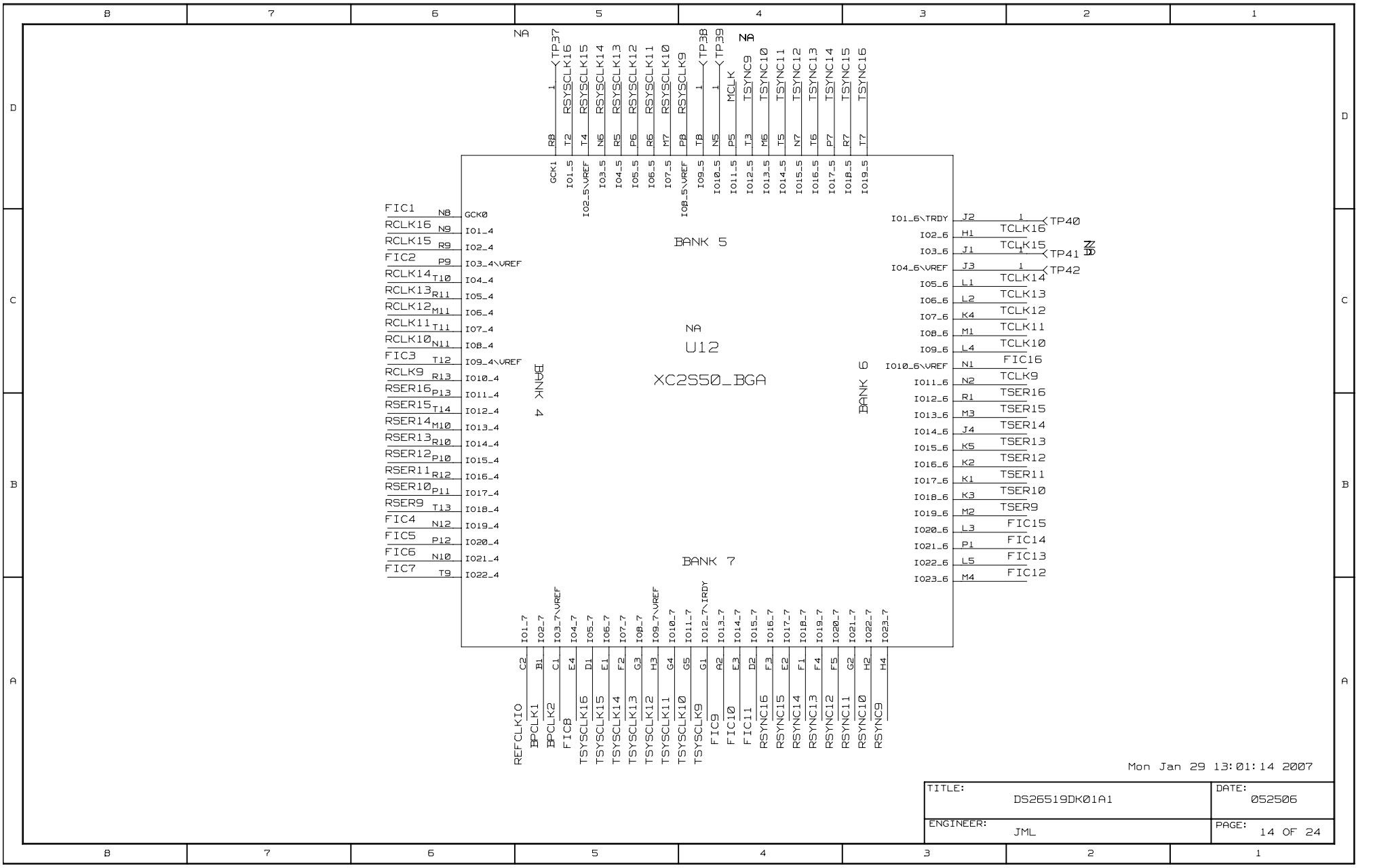

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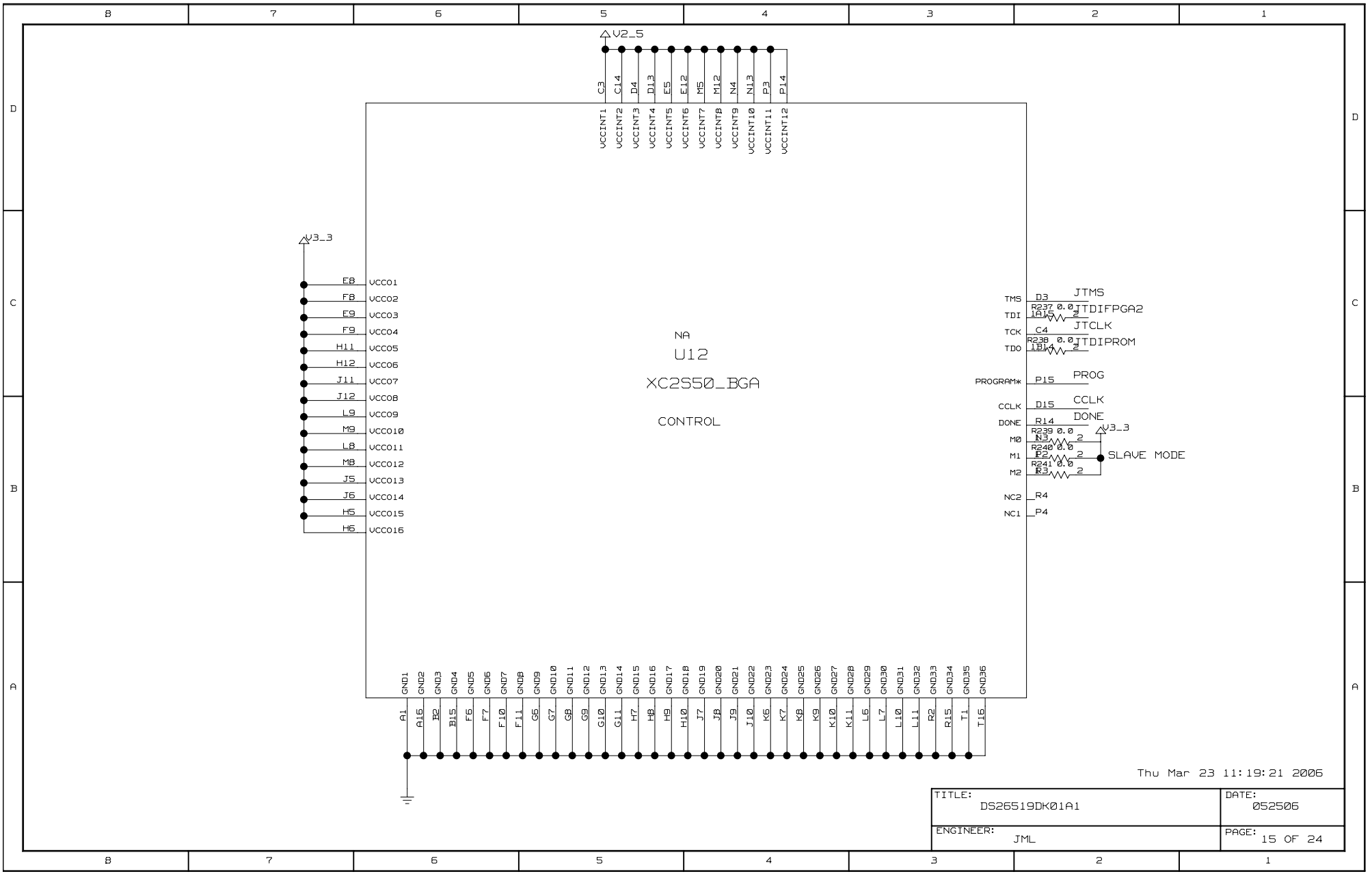

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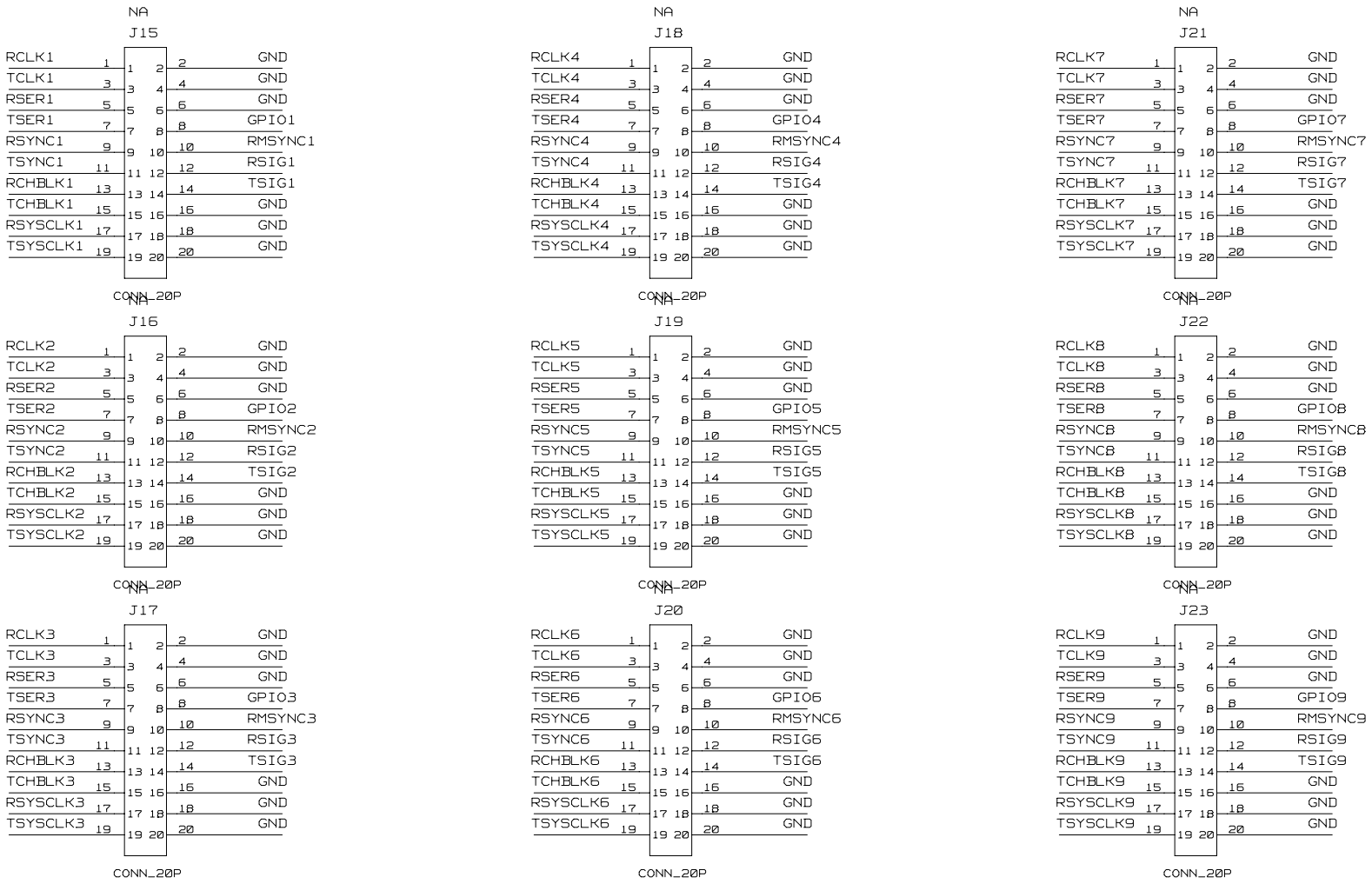

SYSTEM CONNECTORS

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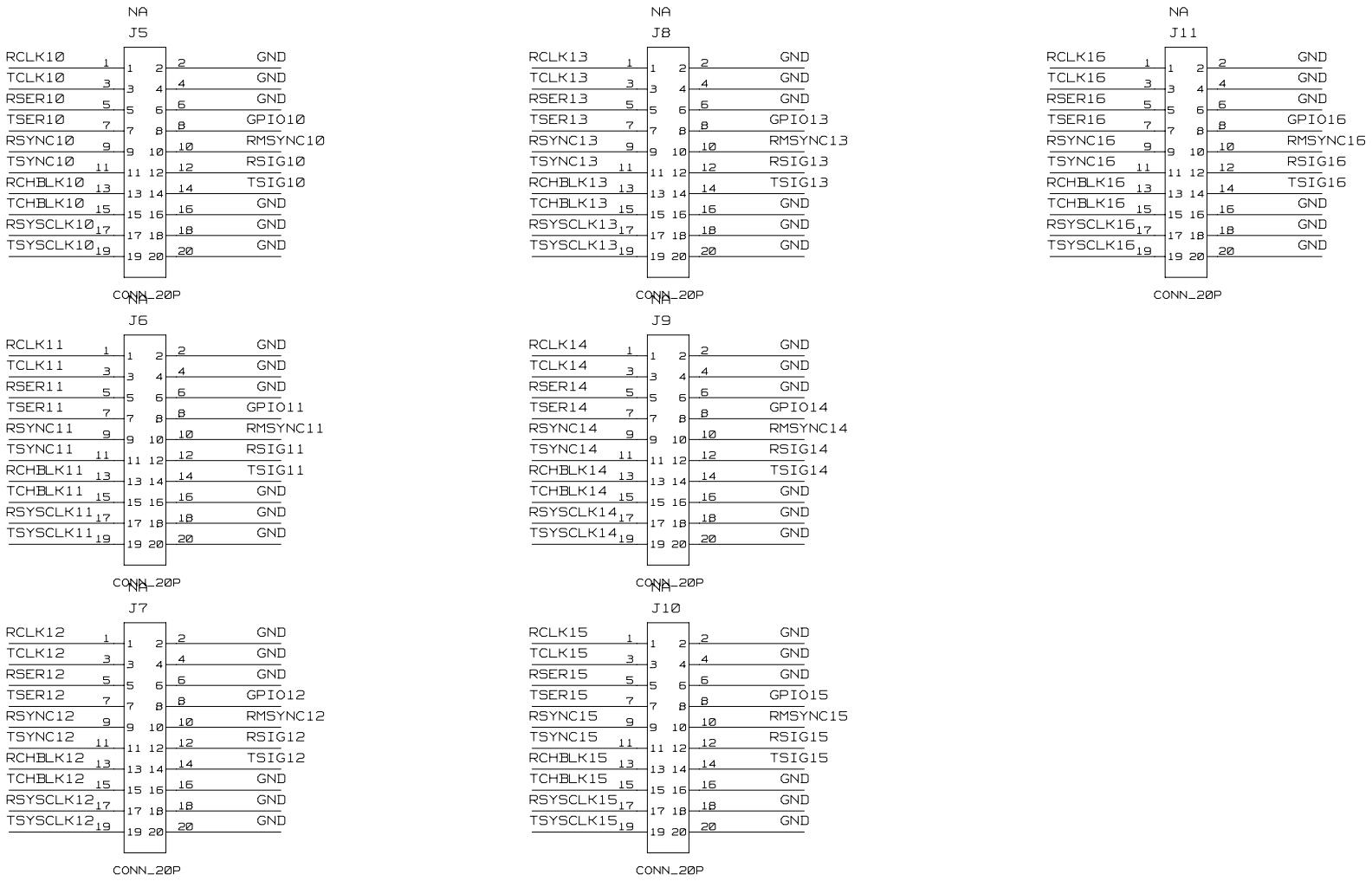

SYSTEM CONNECTORS

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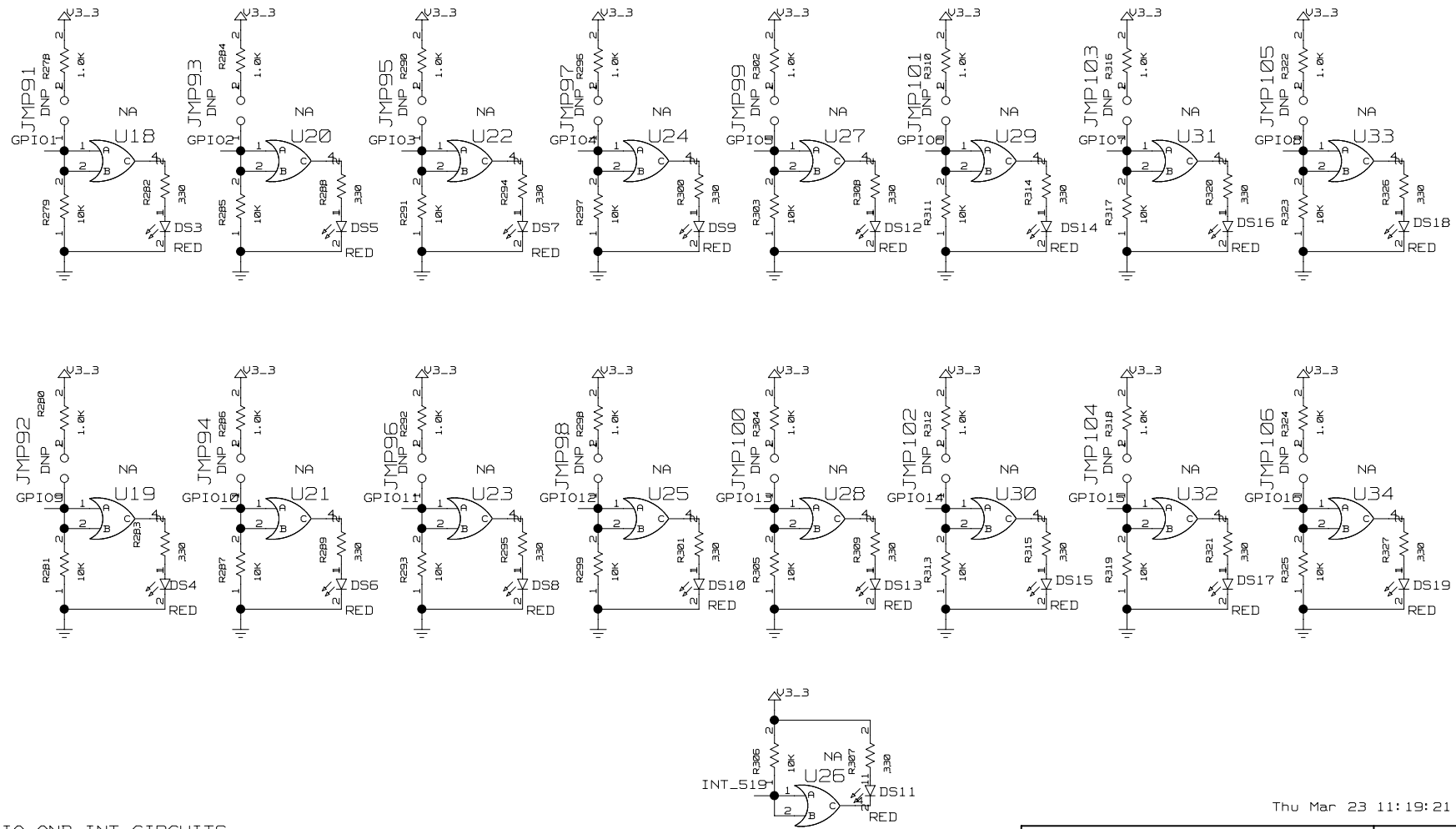

GPIO AND INT CIRCUITS

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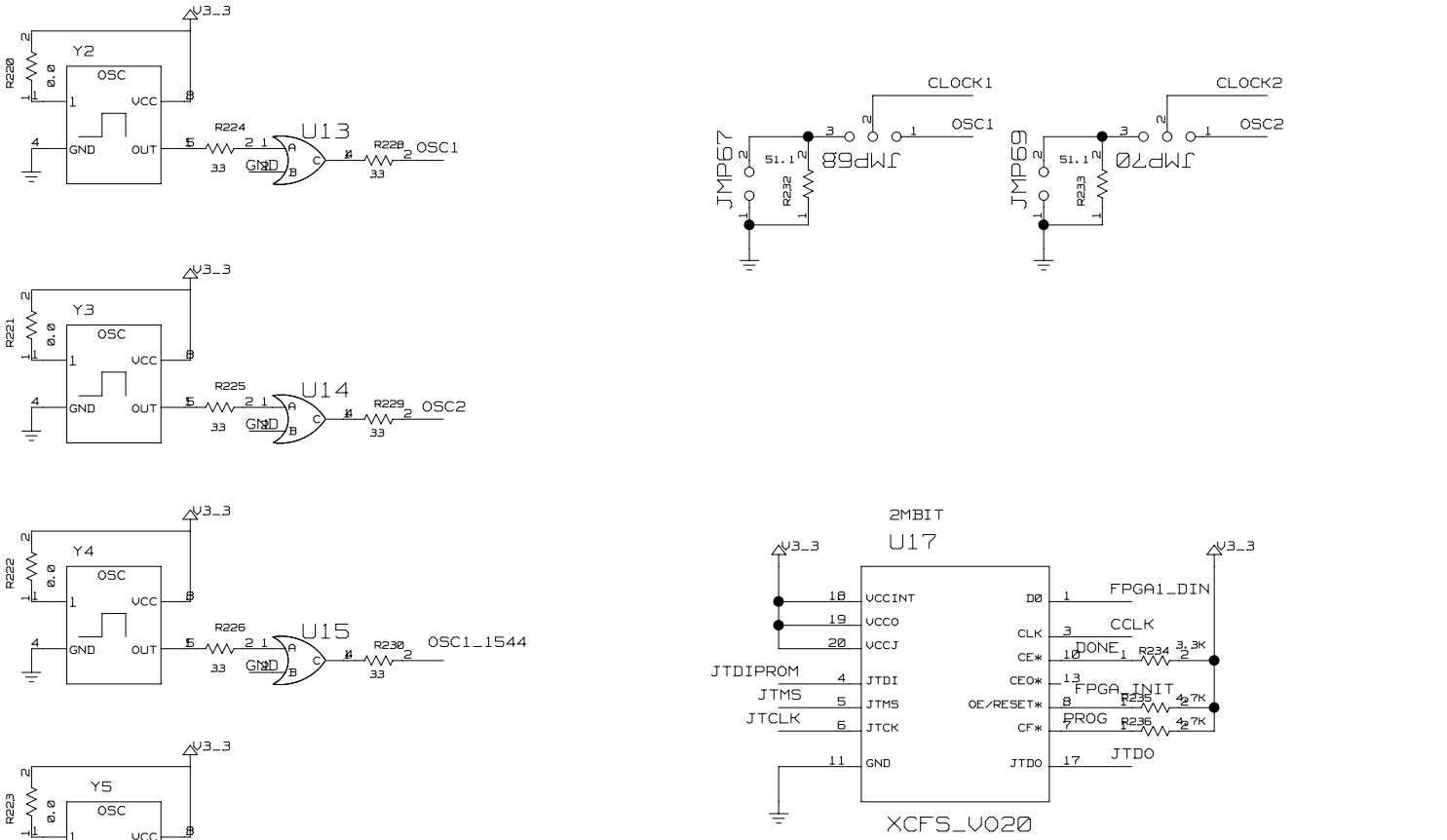

CLOCKS AND PLATFORM FLASH PROM

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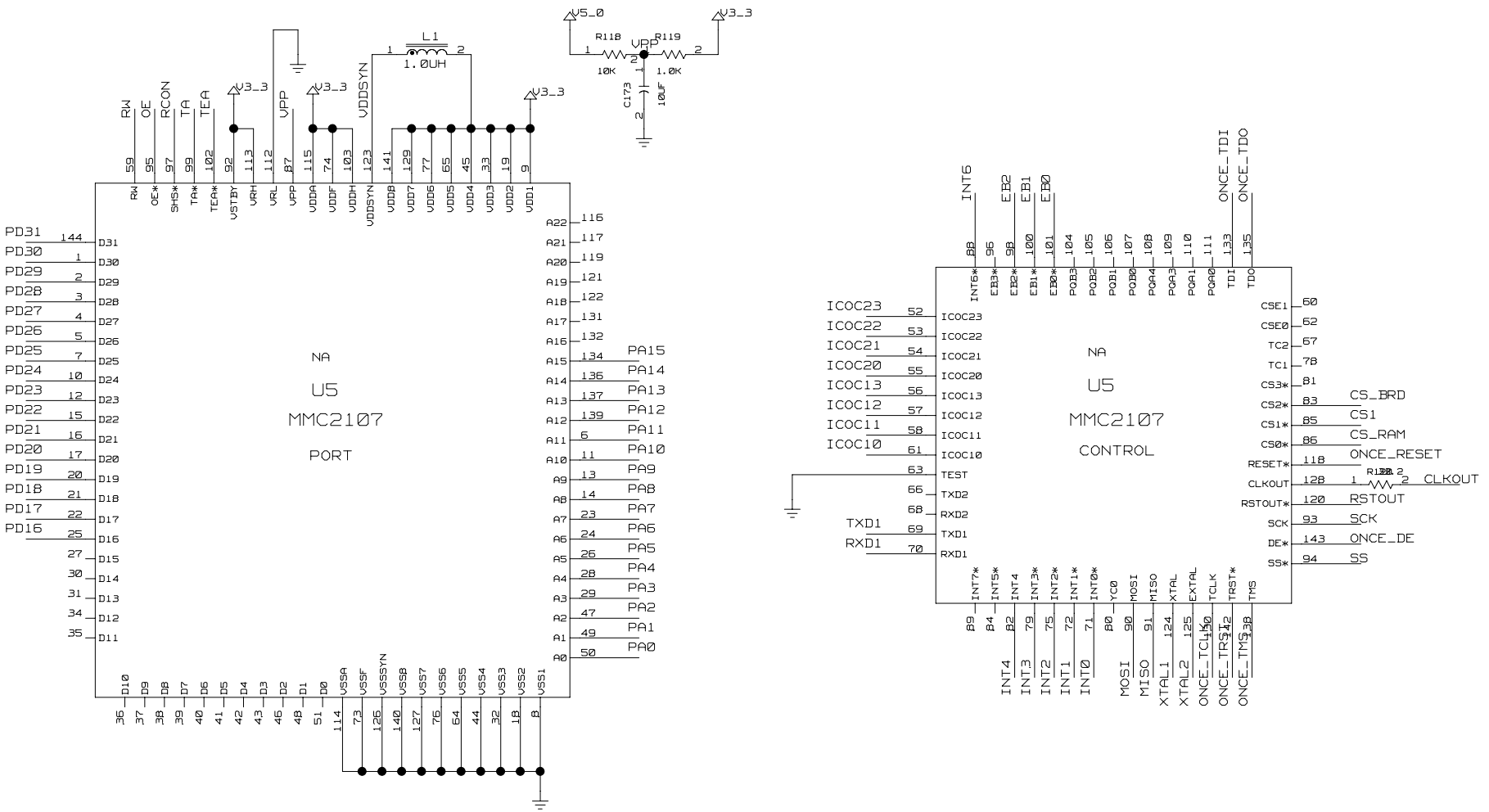

MICROPROCESSOR

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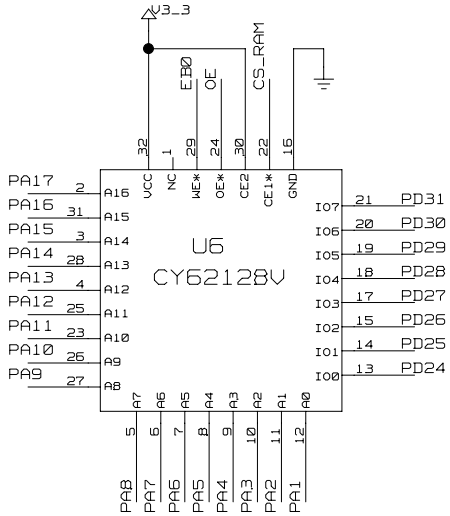

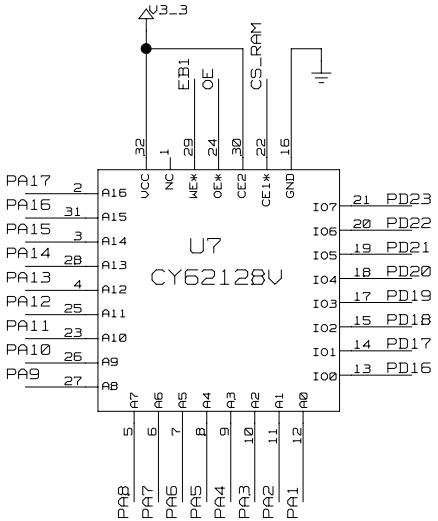

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MICROPROCESSOR MEMORY

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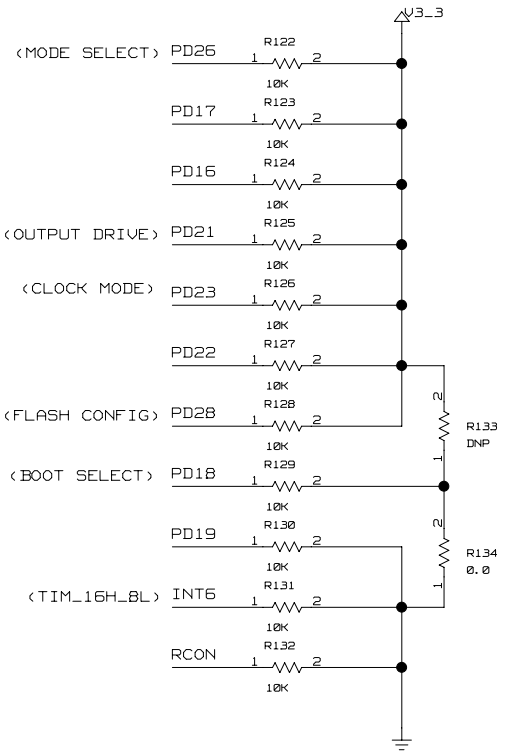

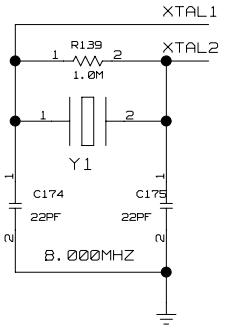

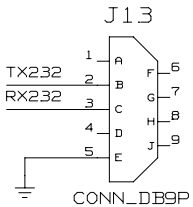

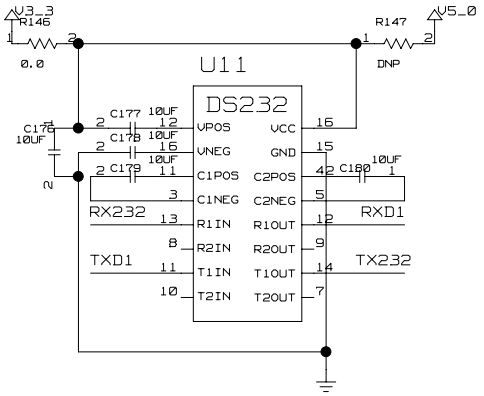

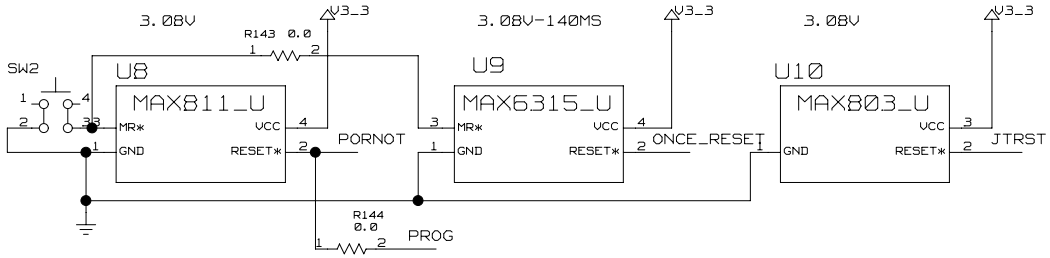

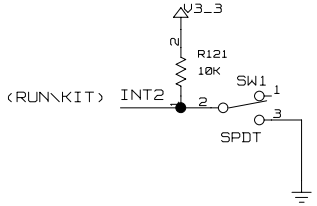

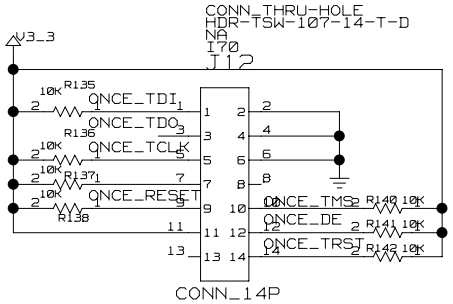

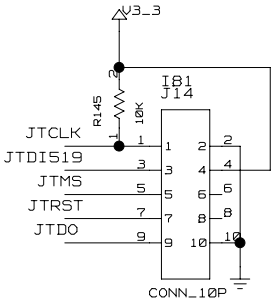

MICROPROCESSOR SUPPORT AND JTAG

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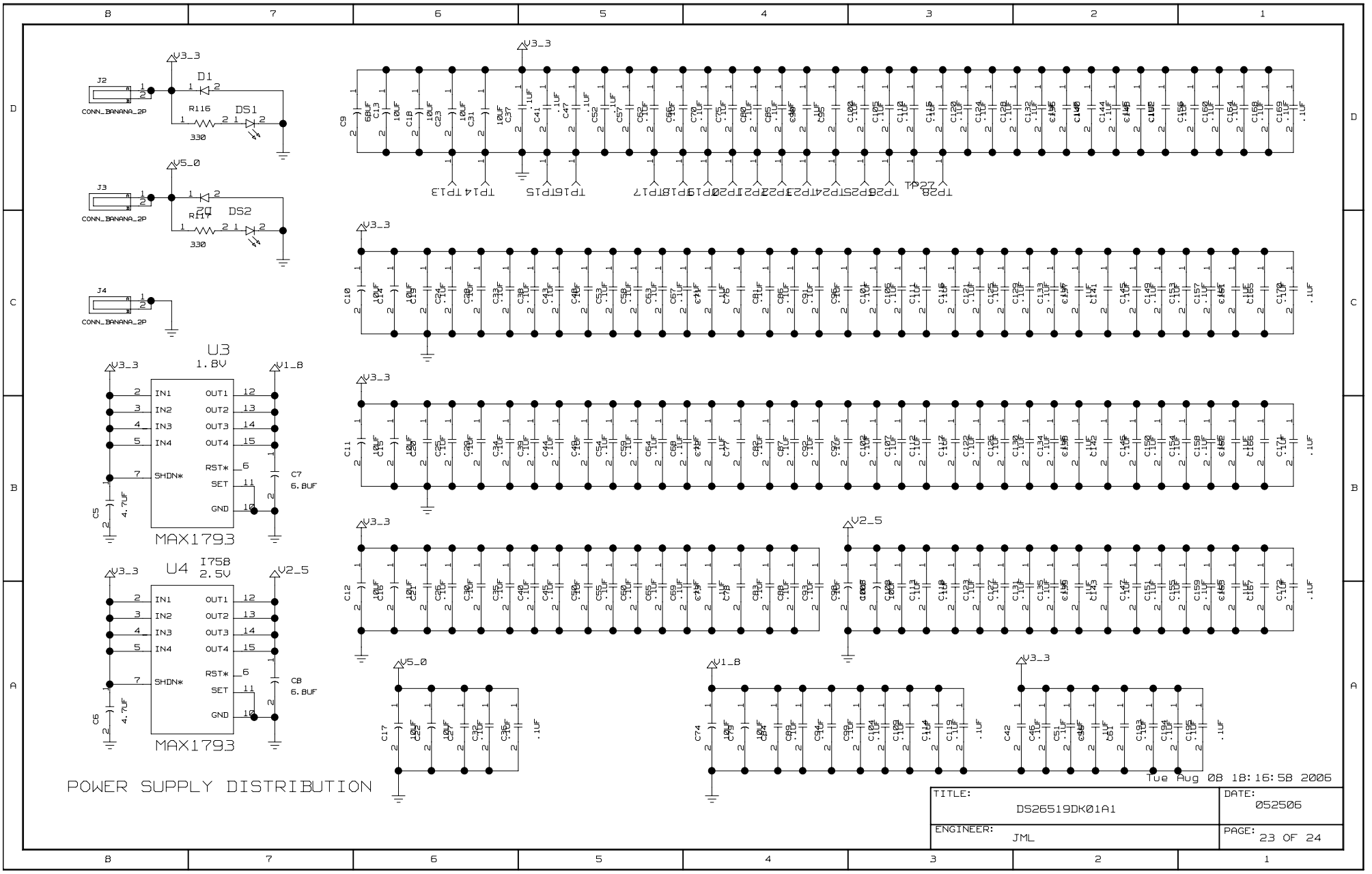
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U3
1.8V
MAX1793
U4
I758
2.5V
MAX1793
POWER SUPPLY DISTRIBUTION
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REVISION HISTORY -

070606 - 01 - INITIAL RELEASE FOR DESIGN REVIEW

080906 - A0 - RELEASE FOR FAB QUOTES

012507 - A1 - MODE PINS AND INT PINS FOR FPGA
PINOUT ON 8-PORT RJ48 CONNECTORS

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