

### GENERAL DESCRIPTION

The DS26519DK is an easy-to-use evaluation board for the DS26519 16-port T1/E1/J1 transceiver. The DS26519DK is a stand-alone system. The board comes complete with a transceiver, transformers, termination resistors, configuration jumpers, network connectors, processor, RS-232 interface, and power adapter. Dallas' ChipView software gives point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs support GPIO pins to indicate status, and FPGAs provide for multiple clock and signal routing configurations.

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### DEMO KIT CONTENTS

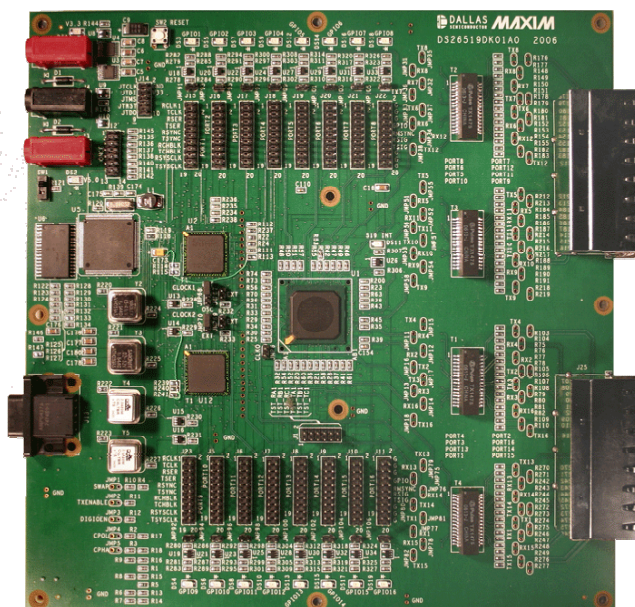
- DS26519DK Board
- CD\_ROM Including:
  - ChipView Software
  - DS26519 Definition Files
  - DS26519DK Definition File
  - DS26519DK Data Sheet
  - DS26519 Data Sheet

### FEATURES

- Demonstrates Key Functions of DS26519 T1/E1/J1 SCT
- Network Connectors, Transformers, and Termination Ease Connectivity
- Careful Layout Provides Signal Integrity
- On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS26519 Register Set
- Software-Controlled (Register Mapped) Configuration Switches Facilitate Clock and Signal Routing
- All System-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs Programmed via GPIO Pins Provide Status
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

### ORDERING INFORMATION

PART	DESCRIPTION
DS26519DK	Demo kit for DS26519



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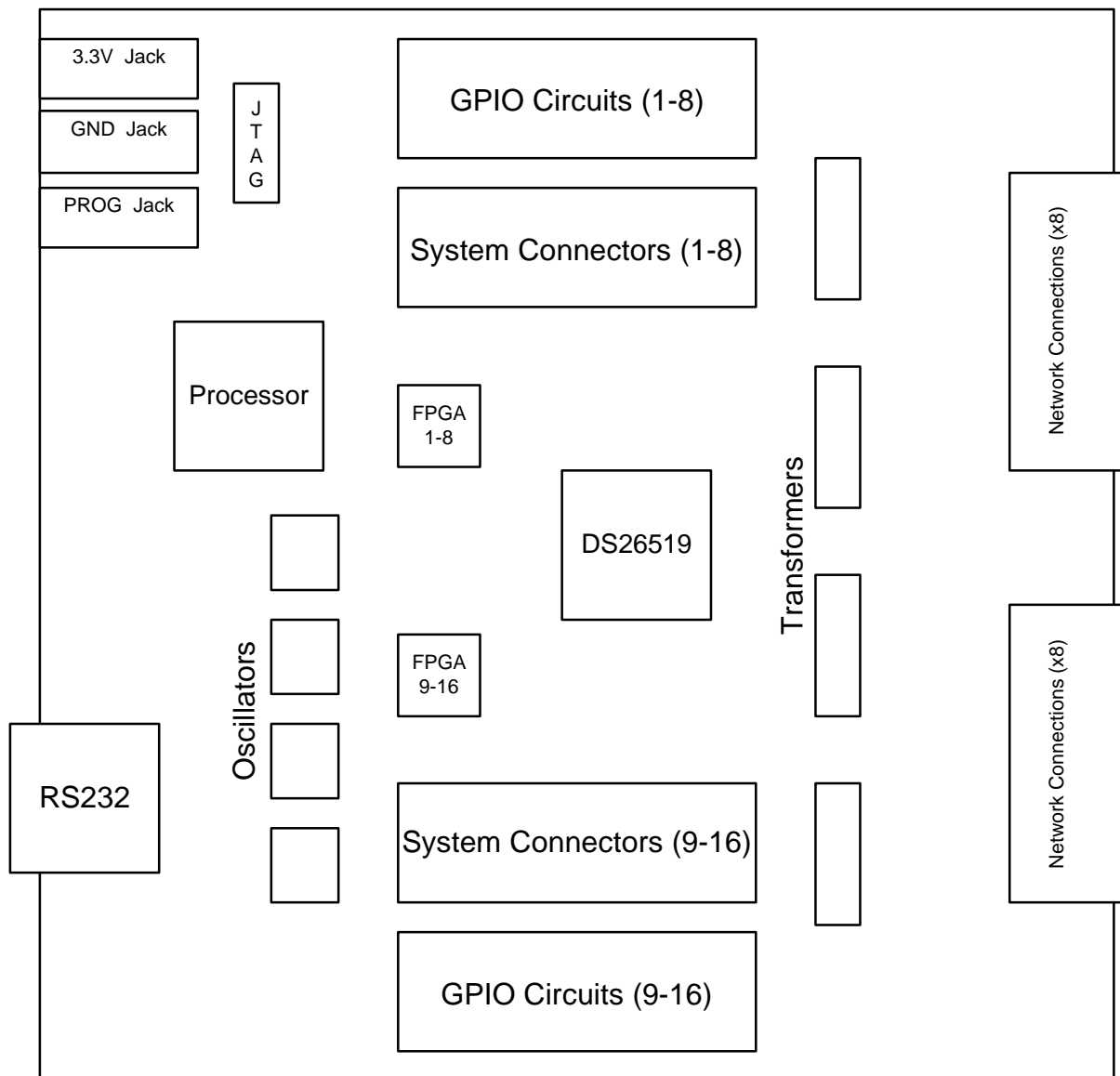
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## 1. BOARD FLOORPLAN

Figure 1 shows the floor plan of the DS26519DK. The DS26519 is near the center of the board. The network connections are provided on the right side of the board, which includes transformers and stacked RJ48 connectors. Toward the center of the board are two FPGAs that provide muxes for control of system-side connections via memory-mapped registers. Above and below the DS26519 are headers that provide access to all system-side signals. The GPIO circuits next to the system connectors provide an interface to the GPIO pins via a header and an LED for each GPIO. The power-supply connections, microprocessor, and JTAG connection are all in the top left quadrant of the board. The power-supply section has three banana jacks for 3.3V, ground, and programming (used at the factory). The bottom left quadrant of the board houses a serial port connector for interface to a computer and clock distribution circuitry.

**Figure 1-1. DS26519DK Board Floorplan**



## 2. CLOCK JUMPERS

Jumpers JMP68 and JMP70 (middle left of board) select the main clock source for ports 1–8 and ports 9–16, respectively. The source can be external via JMP67 (ports 1–8) or JMP69 (ports 9–16) or on-board oscillators Y2 (ports 1–8) and Y3 (ports 9–16). Oscillators Y4 and Y5 are auxiliary oscillators for ports 1–8 and ports 9–16, respectively. The clock sources are muxed to the DS26519DK oscillators via FPGAs (see the [ADDRESS MAP](#) section for details).

## 3. LINE-SIDE CONNECTIONS

The DS26519DK provides four octal transformers, two stacked RJ48 connectors, and test points to support all 16 ports. The test points are clearly labeled on both sides of the transformers with port numbers.

## 4. SYSTEM CONNECTORS

System-side signals can be accessed from 16 headers. The headers are clearly labeled with port and signal information.

## 5. MICROCONTROLLER

The microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS26519 and the FPGAs.

## 6. POWER-SUPPLY CONNECTORS

Connect a 3.3V power supply across the red J2 and black J4 (GND) banana jacks for normal operation. Banana jack J3 is used by the factory for application of programming voltage for the microcontroller. Diodes D1 and D2 provide protection against power connection reversal. The LED DS1 provides indications that a 3.3V supply is connected properly. The 3.3V supply is regulated to supply proper voltages to various circuits on the board.

## 7. CONNECTING TO A COMPUTER

Connect a standard DB-9 serial cable between the serial port on the DS26519DK and an available serial port on the host computer. The host computer must be a Windows-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

## 8. INSTALLING AND RUNNING THE SOFTWARE

ChipView is a general-purpose program that supports a number of Dallas Semiconductor demo kits. To install the ChipView software, run SETUP.EXE from the disk included in the DS26519DK box or from the zip file downloadable on our website at [www.maxim-ic.com/DS26519DK](http://www.maxim-ic.com/DS26519DK).

After installation, run the ChipView program with the DS26519DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select **Programs→ChipView→ChipView**. In the opening screen, click the **Register View** button. Select the correct serial port in the **Port Selection** dialog box, then click **OK**.

Next, the **Definition File Assignment** window appears. This window has subwindows to select definition files for up to four separate boards on other Dallas evaluation platforms. In the active subwindow, select the 26519T1.DEF (or 26519E1.DEF) definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS26519's register map. To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

## 9. ADDRESS MAP

Address space begins at 0x81000000. All offsets given in the following tables are relative to 0x81000000.

Registers in the FPGA can be easily modified using the ChipView host-based user interface software along with the definition file named "DS26519DK.DEF."

**Table 9-1. Address Map**

OFFSET	DEVICE	DESCRIPTION
0X0000	FPGA	Board identification and clock/signal routing
0X4000	DS26519	DS26519 registers

### 9.1 FPGA Register Map

**Table 9-2. FPGA Register Map for FPGA 0 (U2)**

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0100	BID	Read only	Board ID
0X0102	XBIDH	Read only	High Nibble Extended Board ID
0X0103	XBIDM	Read only	Middle Nibble Extended Board ID
0X0104	XBIDL	Read only	Low Nibble Extended Board ID
0X0105	BREV	Read only	Board FAB Revision
0X0106	AREV	Read only	Board Assembly Revision
0X0107	PREV	Read only	FPGA Revision
0X0108	PNUM	Read only	FPGA number
0x010a 0x010b 0x010c 0x010d 0x010e 0x010f 0x0110 0x0111	TCLKnSRC	Control	DS26519 TCLKn Source , Ports 1–8
0X0112	TSERSRC1	Control	DS26519 TSER Source, Ports 1–4
0x0113	TSERSRC2	Control	DS26519 TSER Source, Ports 5–8
0X0114	TSYNCIO	Control	DS26519 TSYNC IO, Ports 1–8
0X0115	RSYNCIO	Control	DS26519 RSYNC IO, Ports 1–8
0x0116	TSYNC SRC1	Control	DS26519 TSYNC Source, Ports 1–4
0x0117	TSYNC SRC2	Control	DS26519 TSYNC Source, Ports 5–8
0x0118	RSYNC SRC1	Control	DS26519 RSYNC source, Ports 1–4
0x0119	RSYNC SRC2	Control	DS26519 RSYNC source, Ports 5–8
0x011a	CLKDIVIDE	Control	Local sync clock divider
0x011b	SYNCSRC	Control	Sync source/Local sync clock source
0x011c	TSYSCLK SRC1	Control	DS26519 TSYSCLK Source, Ports 1–4
0x011d	TSYSCLK SRC2	Control	DS26519 TSYSCLK Source, Ports 5–8
0x011e	RSYSCLK SRC1	Control	DS26519 RSYSCLK Source, Ports 1–4
0X011f	RSYSCLK SRC2	Control	DS26519 RSYSCLK Source, Ports 5–8

**Table 9-3. FPGA Register Map for FPGA 1 (U12)**

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0X0000	BID	Read only	Board ID
0X0002	XBIDH	Read only	High Nibble Extended Board ID
0X0003	XBIDM	Read only	Middle Nibble Extended Board ID
0X0004	XBIDL	Read only	Low Nibble Extended Board ID
0X0005	BREV	Read only	Board FAB Revision
0X0006	AREV	Read only	Board Assembly Revision
0X0007	PREV	Read only	FPGA Revision
0X0008	PNUM	Read only	FPGA number
0x000a 0x000b 0x000c 0x000d 0x000e 0x000f 0x0010 0x0011	TCLKnSRC	Control	DS26519 TCLKn Source , Ports 9–16
0X0012	TSESR1	Control	DS26519 TSESR Source, Ports 9–12
0x0013	TSESR2	Control	DS26519 TSESR Source, Ports 13–16
0X0014	TSYNCIO	Control	DS26519 TSYNC IO, Ports 9–16
0X0015	RSYNCIO	Control	DS26519 RSYNC IO, Ports 9–16
0x0016	TSYNC1	Control	DS26519 TSYNC Source, Ports 9–12
0x0017	TSYNC2	Control	DS26519 TSYNC Source, Ports 13–16
0x0018	RSYNC1	Control	DS26519 RSYNC source, Ports 9–12
0x0019	RSYNC2	Control	DS26519 RSYNC source, Ports 13–16
0x001a	CLKDIVIDE	Control	Local sync
0x001b	SYNCSRC	Control	Sync source/Local sync clock source
0x001c	TSYSCLK1	Control	DS26519 TSYSCLK Source, Ports 9–12
0x001d	TSYSCLK2	Control	DS26519 TSYSCLK Source, Ports 13–16
0x001e	RSYSCLK1	Control	DS26519 RSYSCLK Source, Ports 9–12
0X001f	RSYSCLK2	Control	DS26519 RSYSCLK Source, Ports 13–16

**Note:** The following register descriptions are specific to FPGA0 (U2) but pertain to FPGA1 (U12). The ports that are referenced in the descriptions change from ports 1–8 to ports 9–12. CLOCK1 references change to CLOCK2 (except in the RSYSCLKn and TSYSCLKn register, where CLOCK2 is used as a source in both FPGAs). BPCLK1 reference changes to BPCLK2.

## 9.2 ID Registers

**BID: BOARD ID (Offset = 0X0000)**

BID is read-only with a value of 0xD.

**XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset = 0X0002)**

XBIDH is read-only with a value of 0x0.

**XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset = 0X0003)**

XBIDM is read-only with a value of 0x2.

**XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset = 0X0004)**

XBIDL is read-only with a value of 0xa.

**BREV: BOARD FAB REVISION (Offset = 0X0005)**

BREV is read-only and displays the current fab revision.

**AREV: BOARD ASSEMBLY REVISION (Offset = 0X0006)**

AREV is read-only and displays the current assembly revision.

**PREV: FPGA REVISION (Offset = 0X0007)**

PREV is read-only and displays the current FPGA code revision.

**PNUM: FPGA NUMBER (Offset = 0X0008)**

PNUM is read-only and displays the active FPGA number (0 or 1).



### 9.3 Control Registers

Register Name: **TCLK1SRC**

Register Description: **TCLK1 SOURCE**

Register Offset: **0x010a**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK1 to OSC1\_1544. An 0x0F written to this register connects TCLK1 to CLOCK1. A one written to bit RCLKn connects TCLK1 to RCLKn.

Register Name: **TCLK2SRC**

Register Description: **TCLK2 SOURCE**

Register Offset: **0x010b**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK2 to OSC1\_1544. An 0x0F written to this register connects TCLK2 to CLOCK1. A one written to bit RCLKn connects TCLK2 to RCLKn.

Register Name: **TCLK3SRC**

Register Description: **TCLK3 SOURCE**

Register Offset: **0x010c**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK3 to OSC1\_1544. An 0x0F written to this register connects TCLK3 to CLOCK1. A one written to bit RCLKn connects TCLK3 to RCLKn.

Register Name: **TCLK4SRC**

Register Description: **TCLK4 SOURCE**

Register Offset: **0x010d**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK4 to OSC1\_1544. An 0x0F written to this register connects TCLK4 to CLOCK1. A one written to bit RCLKn connects TCLK4 to RCLKn.

Register Name: **TCLK5SRC**  
 Register Description: **TCLK5 SOURCE**  
 Register Offset: **0x010e**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK5 to OSC1\_1544. An 0x0F written to this register connects TCLK5 to CLOCK1. A one written to bit RCLKn connects TCLK5 to RCLKn.

Register Name: **TCLK6SRC**  
 Register Description: **TCLK6 SOURCE**  
 Register Offset: **0x010f**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK6 to OSC1\_1544. An 0x0F written to this register connects TCLK6 to CLOCK1. A one written to bit RCLKn connects TCLK6 to RCLKn.

Register Name: **TCLK7SRC**  
 Register Description: **TCLK7 SOURCE**  
 Register Offset: **0x0110**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK7 to OSC1\_1544. An 0x0F written to this register connects TCLK7 to CLOCK1. A one written to bit RCLKn connects TCLK7 to RCLKn.

Register Name: **TCLK8SRC**  
 Register Description: **TCLK8 SOURCE**  
 Register Offset: **0x0111**

Bit #	7	6	5	4	3	2	1	0
Name	RCLK8	RCLK7	RCLK6	RCLK5	RCLK4	RCLK3	RCLK2	RCLK1
Default	0	0	0	0	0	0	0	0

**Note:** An 0xF0 written to this register connects TCLK8 to OSC1\_1544. An 0x0F written to this register connects TCLK8 to CLOCK1. A one written to bit RCLKn connects TCLK8 to RCLKn.

Register Name: **TSERSRC1**  
 Register Description: **TSER SOURCE 1**  
 Register Offset: **0x0112**

Bit #	7	6	5	4	3	2	1	0
Name	RSER4	RSER4	RSER3	RSER3	RSER2	RSER2	RSER1	RSER1
Default	0	0	0	0	0	0	0	0

**Note:** A one written to either bit labeled RSER4, RSER3, RSER2, RSER1 connects TSERn with the respective RSERn pin. If both RSERn bits are written a one, TSERn is driven to a one. If both RSERn bits are written a zero, TSERn is pulled low. For example, 0x03 will drive TSER1 to a one.

Register Name: **TSERSRC2**  
 Register Description: **TSER SOURCE 2**  
 Register Offset: **0x0113**

Bit #	7	6	5	4	3	2	1	0
Name	RSER8	RSER8	RSER7	RSER7	RSER6	RSER6	RSER5	RSER5
Default	0	0	0	0	0	0	0	0

**Note:** A one written to either bit labeled RSER8, RSER7, RSER6, RSER5 connects TSERn with the respective RSERn pin. If both RSERn bits are written a one, TSERn is driven to a one. If both RSERn bits are written a zero, TSERn is pulled low. For example, 0x03 will drive TSER1 to a one.

Register Name: **TSYNCIO**  
 Register Description: **TSYNC I/O SELECT**  
 Register Offset: **0x0114**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC8	TSYNC7	TSYNC6	TSYNC5	TSYNC4	TSYNC3	TSYNC2	TSYNC1
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bit TSYNCn makes the TSYNCn pin an output (driven by TSYNCnO). A zero written to bit TSYNCn makes TSYNCn an input.

Register Name: **RSYNCIO**  
 Register Description: **RSYNC I/O SELECT**  
 Register Offset: **0x0115**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC8	RSYNC7	RSYNC6	RSYNC5	RSYNC4	RSYNC3	RSYNC2	RSYNC1
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bit RSYNCn makes the RSYNCn pin an output (driven by RSYNCnO). A zero written to bit RSYNCn makes RSYNCn an input.

Register Name: **TSYNCSRC1**  
 Register Description: **TSYNC SOURCE 1**  
 Register Offset: **0x0116**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC4	SYNC4	RSYNC3	SYNC3	RSYNC2	SYNC2	RSYNC1	SYNC1
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bit SYNCn connects TSYNCnO to a common internal SYNC net. A one written to RSYNCn connects RSYNCn to TSYNCnO. If both RSYNCn and SYNCn are written a one, TSYNCnO is driven to a logic 1. If both RSYNCn and SYNCn are written a zero, TSYNCnO is held at zero.

Register Name: **TSYNCSRC2**  
 Register Description: **TSYNC SOURCE 2**  
 Register Offset: **0x0117**

Bit #	7	6	5	4	3	2	1	0
Name	RSYNC8	SYNC8	RSYNC7	SYNC7	RSYNC6	SYNC6	RSYNC5	SYNC5
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bit SYNCn connects TSYNCnO to a common internal SYNC net. A one written to RSYNCn connects RSYNCn to TSYNCnO. If both RSYNCn and SYNCn are written a one, TSYNCnO is driven to a logic 1. If both RSYNCn and SYNCn are written a zero, TSYNCnO is held at zero.

Register Name: **RSYNCSRC1**  
 Register Description: **RSYNC SOURCE 1**  
 Register Offset: **0x0118**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC4	SYNC4	TSYNC3	SYNC3	TSYNC2	SYNC2	TSYNC1	SYNC1
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bit SYNCn connects RSYNCnO to a common internal SYNC net. A one written to TSYNCn connects TSYNCn to RSYNCnO. If both TSYNCn and SYNCn are written a one, RSYNCnO is driven to a logic 1. If both TSYNCn and SYNCn are written a zero, RSYNCnO is held at zero.

Register Name: **RSYNCSRC2**  
 Register Description: **RSYNC SOURCE 2**  
 Register Offset: **0x0119**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC8	SYNC8	TSYNC7	SYNC7	TSYNC6	SYNC6	TSYNC5	SYNC5
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bit SYNCn connects RSYNCnO to a common internal SYNC net. A one written to TSYNCn connects TSYNCn to RSYNCnO. If both TSYNCn and SYNCn are written a one, RSYNCnO is driven to a logic 1. If both TSYNCn and SYNCn are written a zero, RSYNCnO is held at zero.

Register Name: **CLKDIVIDE**  
 Register Description: **SYNC CLOCK DIVIDER**  
 Register Offset: **0x011a**

Bit #	7	6	5	4	3	2	1	0
Name	B7	B6	B5	B4	B3	B2	B1	B0
Default	0	0	0	0	0	0	0	0

**Note:** The SYNC SOURCE clock is divided by the value in this register to provide a local sync. For instance, for T1 a divisor of 193 is appropriate (C1H)

Register Name: **SYNCSRC**  
 Register Description: **LOCAL SYNC CLOCK SOURCE AND NET SYNC SOURCE**  
 Register Offset: **0x011b**

Bit #	7	6	5	4	3	2	1	0
Name	TSYNC1	RSYNC1	LOCAL	LOCAL	BPCLK1	OSC1	CLOCK1	CLOCK1
Default	0	0	0	0	0	0	0	0

**Note:** A one written to the upper nibble connects internal net (sync) to respective source. A one written lower nibble connects local sync generator to respective clock. Bit named LOCAL is a locally generated sync.

Register Name: **TSYSCLKSRC1**  
 Register Description: **TSYSCLK SOURCE 1**  
 Register Offset: **0x011c**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to TSYSCLK4, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to TSYSCLK3, TSYSCLK2, and TSYSCLK1, respectively. CLOCK2 comes from FPGA1.

Register Name: **TSYSCLKSRC2**  
 Register Description: **TSYSCLK SOURCE 2**  
 Register Offset: **0x011d**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to TSYSCLK8, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to TSYSCLK7, TSYSCLK6, and TSYSCLK5, respectively. CLOCK2 comes from FPGA1.

Register Name: **RSYSCLKSRC1**  
 Register Description: **RSYSCLK SOURCE 1**  
 Register Offset: **0x011e**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to RSYCLK4, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to RSYCLK3, RSYCLK2, and RSYCLK1, respectively. CLOCK2 comes from FPGA1.

Register Name: **RSYSCLKSRC2**  
 Register Description: **RSYSCLK SOURCE 2**  
 Register Offset: **0x011f**

Bit #	7	6	5	4	3	2	1	0
Name	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2	BPCLK1	CLOCK2
Default	0	0	0	0	0	0	0	0

**Note:** A one written to bits 6 or 7 connects BPCLK1 or CLOCK2 to RSYCLK8, respectively. Bits (4, 5), (2, 3), and (0, 1) correspond similarly to RSYCLK7, RSYCLK6, and RSYCLK5, respectively. CLOCK2 comes from FPGA1.

## **10. ADDITIONAL INFORMATION/RESOURCES**

### **10.1 DS26519 Information**

For more information about the DS26519, refer to the DS26519 data sheet at [www.maxim-ic.com/DS26519](http://www.maxim-ic.com/DS26519).

### **10.2 DS26519DK Information**

For more information about the DS26519DK including software downloads, refer to the DS26519DK Quick View page at [www.maxim-ic.com/DS26519DK](http://www.maxim-ic.com/DS26519DK).

### **10.3 Technical Support**

For additional technical support, go to [www.maxim-ic.com/support](http://www.maxim-ic.com/support).

## 11. COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C174, C175	2	L_0603 CERAM 22pF 25V 5% NPO	AVX	06033A220JAT
C19, C20, C21, C24-C30, C32-C73, C75-C78, C80-C97, C99-C102, C104-C172, C193-C195	150	L_0603 CERAM .1uF 16V 20% X7R	AVX	0603YC104MAT
Y2-Y5	4	SOCKET, OSCILLATOR, HALF SIZE, 4-PIN THROUGH-HOLE	ARI	110880
J4	1	SOCKET, BANANA PLUG, HORIZONTAL, BLACK	MSR	164-6218
J2, J3	2	SOCKET, BANANA PLUG, HORIZONTAL, RED	MSR	164-6219
D1, D2	2	DIODE 1A 50V GEN PURPOSE SILICON	GEN	1N4001
J13	1	L_CONN, DB9 RA, LONG CASE	AMP	747459-1
R6-R9, R19, R22, R24, R75-R90, R95-R115, R134, R143, R144, R146, R148-R163, R168-R199, R204-R223, R237-R257, R262-R277	153	L_RES 0603 0 Ohm 1/16W 1%	AVX	CJ10-000F
U6, U7	2	IC, SRAM, 128K X 8, 32 PIN SOIC	CYP	CY62128VL-70SC
U11	1	DUAL RS232 XMITR/RCVR 16 PIN SOIC (300 MIL)	DAL	DS232AS
Y1	1	XTAL, LOW PROFILE, 8.000MHZ	ECL	EC1-8.000M
C1-C4, C181-C192	16	0805 CERAM 560pF 50V 5% NPO	PAN	ECJ-2VC1H561K
C7,C8	2	1206 CERAM 6.8uF 6.3V 10% X5R	PAN	ECJ-3YB0J685K
C10-C18, C22, C23, C31, C74, C79, C98, C103, C176-C180	21	L_1206 CERAM 10uF 10V 20%	PAN	ECJ-3YB1A106M
C5,C6	2	1206 CERAM 4.7uF 25V 10% X5R	PAN	ECJ-3YB1E475K
C9	1	L_D CASE TANT 68uF 16V 20%	PAN	ECS-T1CD686R
C173	1	L_B CASE TANT 10uF 16V 20%	PAN	ECS-T1CX106R
R20	1	RES 0603 10.0K Ohm 1/16W 1%	PAN	ERJ-3EKF1002V
R91-R94, R164-R167, R200-R203, R258-R261	16	RES 0603 121 Ohm 1/16W 1%	PAN	ERJ-3EKF1210V
R120	1	RES 0603 33.2 Ohm 1/16W 1%	PAN	ERJ-3EKF33R2V
R232, R233	2	L_RES 0603 51.1 Ohm 1/16W 1%	PAN	ERJ-3EKF51R1V
R119, R278, R280, R284, R286, R290, R292, R296, R298, R302, R304, R310, R312, R316, R318, R322, R324	17	L_RES 0603 1.0K Ohm 1/16W 5%	PAN	ERJ-3GEYJ102V
R10-R18, R118, R121- R132, R135-R138, R140-R142, R145, R279, R281, R285, R287, R291, R293, R297, R299, R303, R305, R306, R311, R313, R317, R319, R323, R325	47	L_RES 0603 10K Ohm 1/16W 5%	PAN	ERJ-3GEYJ103V

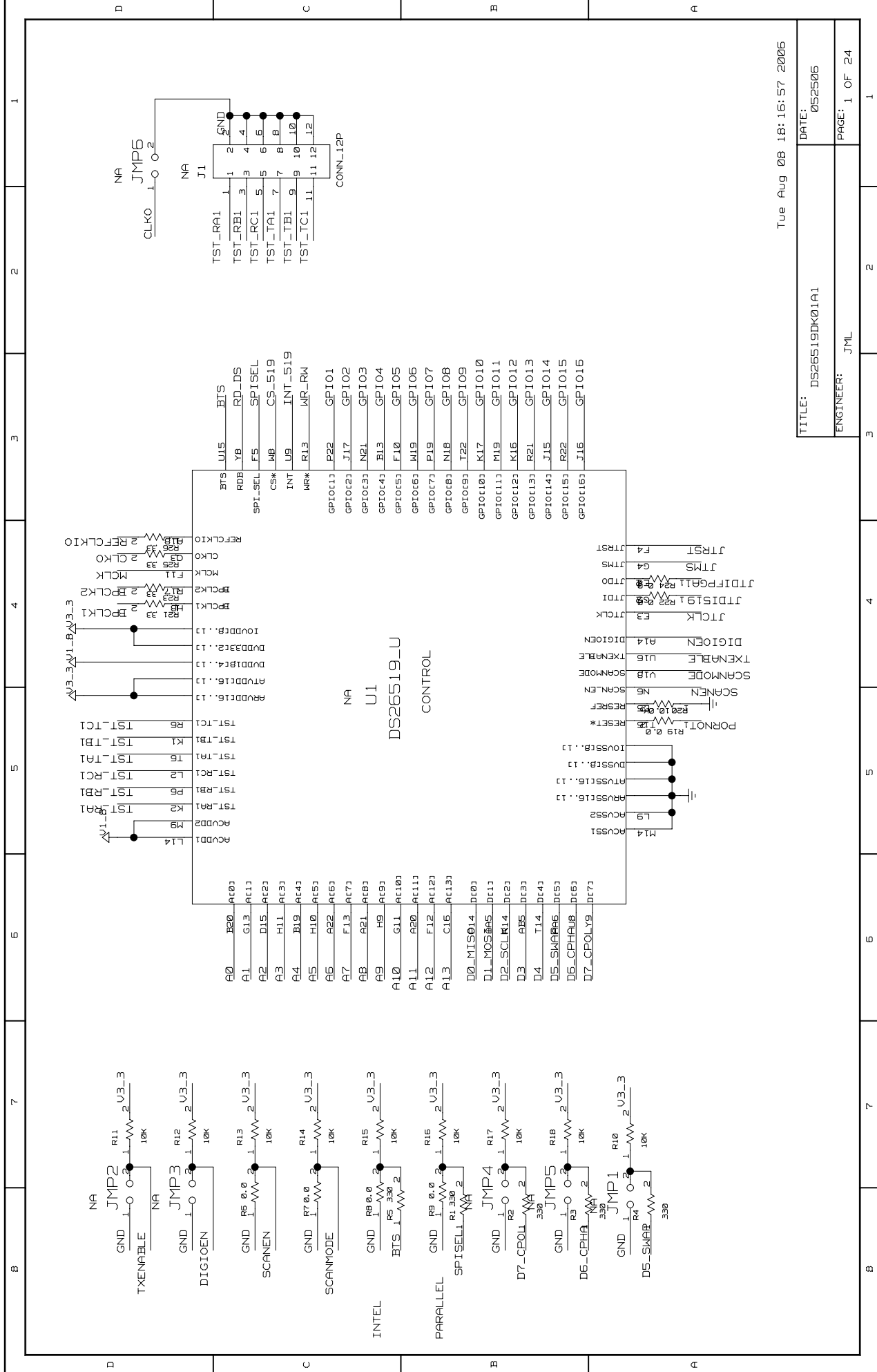


DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
R139	1	RES 0603 1.0M Ohm 1/16W 5%	PAN	ERJ-3GEYJ105V
R21, R23, R25, R26, R28-R74, R224-R231, R328	60	L_RES 0603 33 Ohm 1/16W 5%	PAN	ERJ-3GEYJ330V
R1-R5, R116, R117, R282, R283, R288, R289, R294, R295, R300, R301, R307-R309, R314, R315, R320, R321, R326, R327	24	L_RES 0603 330 Ohm 1/16W 5%	PAN	ERJ-3GEYJ331V
R234	1	RES 0603 3.3K Ohm 1/16W 5%	PAN	ERJ-3GEYJ332V
R235, R236	2	RES 0603 4.7K Ohm 1/16W 5%	PAN	ERJ-3GEYJ472V
SW2	1	L_SWITCH MOM 4PIN SINGLE POLE	PAN	EVQPAE04M
J12	1	HEADER, 14 PIN, DUAL ROW, VERT	STC	HDR-TSW-107-14-T-D
J5-J11, J15-J23	16	HEADER, 20 PIN, DUAL ROW, VERT	STC	HDR-TSW-110-14-T-D
DS1, DS2	2	LED, RED, SMD	PAN	LN1251C
DS3-DS19	17	L_LED, RED, SMD	PAN	LN1251C
U3	1	L_IC, LINEAR REGULATOR, 1.5W, 1.8V OR ADJ, 1A, 16 PIN TSSOP-EP	MAX	MAX1793EUE-18
U4	1	IC, LINEAR REGULATOR, 1.5W, 2.5V OR ADJ, 1A, 16 PIN TSSOP-EP	MAX	MAX1793EUE-25
U9	1	IC, OPEN DRAIN MICROPROCESSOR RESET CKT, 3.08V 140MS, 4PIN SOT143	MAX	MAX6315US31D3-T
U10	1	MICROPROCESSOR RESET CIRCUITS, 3.08V RESET, 3 PIN SC70	MAX	MAX803TEXR-T
U8	1	MICROPROCESSOR VOLTAGE MONITOR, 3.08V RESET, 4PIN SOT143	MAX	MAX811TEUS-T
U5	1	IC, MCORE MICROCONTROLLER, 144 PIN LQFP	MOT	MMC2107PV
JMP7-JMP66, JMP71-JMP106	96	DO NOT PLACE, OPEN 2PIN TH JUMPER	NA	NA
R133, R147	2	RES 0603 DO NOT POPULATE	NA	NA
TP1-TP28, TP37-TP48, TP50	41	TESTPOINT, 1 PLATED HOLE, DO NOT STUFF	NA	NA
U13-U16, U18-U34	21	L_TINYLOGIC HIGH SPEED 2-INPUT OR GATE, 5 PIN SOT23	FAI	NC7SZ32M5
J1	1	L_CONN, 12 PIN, DUAL ROW, VERT	SUL	PTC06DAAN
J24, J25	2	CONNECTOR, STACKED OCTAL JACK, 64- PIN, SHIELDED	MOL	SD-44520-001
U1	1	SOCKET, SURFACE MOUNT, BGA, 484P, 1MM	IRO	SG-BGA-6120
SW1	1	L_SWITCH, SPDT SLIDE, 3PIN TH	TYC	SSA12
JMP1-JMP6, JMP67, JMP69	8	L_2 PIN HEADER, .100 CENTERS, VERTICAL	STC	TSW-102-07-T-S
JMP68, JMP70	2	L_HEADER, 3-PIN, .100 CENTERS, VERTICAL	STC	TSW-103-07-T-S
J14	1	L_TERMINAL STRIP, 10 PIN, DUAL ROW, VERT	STC	TSW-105-07-T-D
T1-T4	4	XFMR, XMIT/RCV, 1 TO 2 AND 1 TO 1, SMT 32 PIN	PUL	TX1475

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
L1	1	INDUCTOR 1.0uH 2PIN SMT 20%	COT	UP1B-1R0
U2, U12	2	XILINX SPARTAN 2.5V FPGA,256 PIN BGA	XIL	XC2S50-5FG256C
U17	1	IC, PLATFORM FLASH IN-SYS PROG CONFIG PROM, 2MBIT, 20 PIN TSSOP	XIL	XCF02SVO20C

## 12. SCHEMATICS

The schematics are featured in the following pages.



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B	7	6	5	4	3	2	1
D	NA U1	NA U1	NA U1	NA U1	NA U1	NA U1	NA U1
C	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT
C	RRING7 F21 RRING RTIP7 G21 RTIP RTIPE7 F22 RTIPE RCHBLK7 E1B RCHBLK RCLK7 R4733 V20 RCLK RSER7 B1B RSR RSIG7 H17 RSIG RSYNCR7 W419 RSYNC RSYSCLK7 C19 RSYSCLK RMSYNCR7 D16 RMSYNC	RRING9 AB12 RRING RTIP9 AB13 RTIP RTIPE9 AB13 RTIPE RCHBLK9 G7 RCHBLK RCLK9 R5233 V32 RCLK RSER9 L17 RSR RSIG9 F6 RSIG RSYNCR9 W419 RSYNC RSYSCLK9 G6 RSYSCLK RMSYNCR9 T21 RMSYNC	RRING10 AB15 RRING RTIP10 AB15 RTIP RTIPE10 AB16 RTIPE RCHBLK10 L15 RCHBLK RCLK10 R5423 V22 RCLK RSER10 L16 RSR RSIG10 P20 RSIG RSYNCR10 W419 RSYNC RSYSCLK10 P18 RSYSCLK RMSYNCR10 V22 RMSYNC	RRING11 AB17 RRING RTIP11 AB17 RTIP RTIPE11 AB18 RTIPE RCHBLK11 B2 RCHBLK RCLK11 R5033 V33 RCLK RSER11 B1 RSR RSIG11 D2 RSIG RSYNCR11 W419 RSYNC RSYSCLK11 F2 RSYSCLK RMSYNCR11 V6 RMSYNC	RRING12 N22 RRING RTIP12 M22 RTIP RTIPE12 L22 RTIPE RCHBLK12 M4 RCHBLK RCLK12 R5033 V32 RCLK RSER12 K7 RSR RSIG12 Y4 RSIG RSYNCR12 W419 RSYNC RSYSCLK12 AB2 RSYSCLK RMSYNCR12 H4 RMSYNC	RRING13 AB18 RRING RTIP13 AB18 RTIP RTIPE13 AB19 RTIPE RCHBLK13 B2 RCHBLK RCLK13 R5033 V33 RCLK RSER13 B1 RSR RSIG13 D2 RSIG RSYNCR13 W419 RSYNC RSYSCLK13 F2 RSYSCLK RMSYNCR13 V6 RMSYNC	RRING14 AB19 RRING RTIP14 AB19 RTIP RTIPE14 AB20 RTIPE RCHBLK14 B2 RCHBLK RCLK14 R5033 V33 RCLK RSER14 B1 RSR RSIG14 D2 RSIG RSYNCR14 W419 RSYNC RSYSCLK14 F2 RSYSCLK RMSYNCR14 V6 RMSYNC
B	NA U1	NA U1	NA U1	NA U1	NA U1	NA U1	NA U1
A	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT	DS26519_U PORT
A	RRINGB D22 RRING RTIPB C21 RTIP RTIPEB C22 RTIPE RCHBLKB U20 RCHBLK RCLKB R4633 V20 RCLK RSERB T20 RSR RSIGB U19 RSIG RSYNCRB W419 RSYNC RSYSCLKB AB22 RSYSCLK RMSYNCRB M21 RMSYNC	RRING10 AB15 RRING RTIP10 AB15 RTIP RTIPE10 AB16 RTIPE RCHBLK10 L15 RCHBLK RCLK10 R5423 V22 RCLK RSER10 L16 RSR RSIG10 P20 RSIG RSYNCR10 W419 RSYNC RSYSCLK10 P18 RSYSCLK RMSYNCR10 V22 RMSYNC	RRING11 AB17 RRING RTIP11 AB17 RTIP RTIPE11 AB18 RTIPE RCHBLK11 B2 RCHBLK RCLK11 R5033 V33 RCLK RSER11 B1 RSR RSIG11 D2 RSIG RSYNCR11 W419 RSYNC RSYSCLK11 F2 RSYSCLK RMSYNCR11 V6 RMSYNC	RRING12 N22 RRING RTIP12 M22 RTIP RTIPE12 L22 RTIPE RCHBLK12 M4 RCHBLK RCLK12 R5033 V32 RCLK RSER12 K7 RSR RSIG12 Y4 RSIG RSYNCR12 W419 RSYNC RSYSCLK12 AB2 RSYSCLK RMSYNCR12 H4 RMSYNC	RRING13 AB18 RRING RTIP13 AB18 RTIP RTIPE13 AB19 RTIPE RCHBLK13 B2 RCHBLK RCLK13 R5033 V33 RCLK RSER13 B1 RSR RSIG13 D2 RSIG RSYNCR13 W419 RSYNC RSYSCLK13 F2 RSYSCLK RMSYNCR13 V6 RMSYNC	RRING14 AB19 RRING RTIP14 AB19 RTIP RTIPE14 AB20 RTIPE RCHBLK14 B2 RCHBLK RCLK14 R5033 V33 RCLK RSER14 B1 RSR RSIG14 D2 RSIG RSYNCR14 W419 RSYNC RSYSCLK14 F2 RSYSCLK RMSYNCR14 V6 RMSYNC	RRING15 AB20 RRING RTIP15 AB20 RTIP RTIPE15 AB21 RTIPE RCHBLK15 B2 RCHBLK RCLK15 R5033 V33 RCLK RSER15 B1 RSR RSIG15 D2 RSIG RSYNCR15 W419 RSYNC RSYSCLK15 F2 RSYSCLK RMSYNCR15 V6 RMSYNC
A	TRINGA E20 TRINGB TRINGB E19 TTIPA F18 TTIPB TTIPB F18 TCHBLK H12 TCHBLKB TCLK D18 TCLKB TSCR E17 TSERB TSIG F14 TSIGB TSYNCR H18 W419 TSYNCB TSYSCLK Y21 TSYSCLB	TRINGA M1 TRING10 TRINGB U14 TTIPA U1 TTIP10 TTIPB M13 TCHBLK M22 TCHBLK10 TCLK P16 TCLK10 TSCR R20 TSERB TSIG U21 TSIG10 TSYNCR M18 W419 TSYNC10 TSYSCLK R19 TSYSCLB	TRINGA Y11 TRING9 TRINGB Y12 TTIPA U1 TTIP9 TTIPB M12 TCHBLK M20 TCHBLK9 TCLK K14 TCLK9 TSCR U21 TSERB TSIG U22 TSIG9 TSYNCR K15 W419 TSYNC9 TSYSCLK L4 TSYSCLB	TRINGA L20 TRING12 TRINGB M20 TTIPA L1 TTIP12 TTIPB L13 TCHBLK M6 TCHBLK12 TCLK M18 TCLK12 TSCR C1 TSERB TSIG A1 TSIG12 TSYNCR M18 W419 TSYNC12 TSYSCLK AB3 TSYSCLB	TRINGA L20 TRING12 TRINGB M20 TTIPA L1 TTIP12 TTIPB L13 TCHBLK M6 TCHBLK12 TCLK M18 TCLK12 TSCR C1 TSERB TSIG A1 TSIG12 TSYNCR M18 W419 TSYNC12 TSYSCLK AB3 TSYSCLB	TRINGA L20 TRING12 TRINGB M20 TTIPA L1 TTIP12 TTIPB L13 TCHBLK M6 TCHBLK12 TCLK M18 TCLK12 TSCR C1 TSERB TSIG A1 TSIG12 TSYNCR M18 W419 TSYNC12 TSYSCLK AB3 TSYSCLB	TRINGA L20 TRING12 TRINGB M20 TTIPA L1 TTIP12 TTIPB L13 TCHBLK M6 TCHBLK12 TCLK M18 TCLK12 TSCR C1 TSERB TSIG A1 TSIG12 TSYNCR M18 W419 TSYNC12 TSYSCLK AB3 TSYSCLB
A	TITLE: DS26519DK01A1	TITLE: DS26519DK01A1	TITLE: DS26519DK01A1	TITLE: DS26519DK01A1	TITLE: DS26519DK01A1	TITLE: DS26519DK01A1	TITLE: DS26519DK01A1
A	ENGINEER: JML	ENGINEER: JML	ENGINEER: JML	ENGINEER: JML	ENGINEER: JML	ENGINEER: JML	ENGINEER: JML
A	DATE: 052506	DATE: 052506	DATE: 052506	DATE: 052506	DATE: 052506	DATE: 052506	DATE: 052506
A	PAGE: 3 OF 24	PAGE: 3 OF 24	PAGE: 3 OF 24	PAGE: 3 OF 24	PAGE: 3 OF 24	PAGE: 3 OF 24	PAGE: 3 OF 24
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B	7	6	5	4	3	2	1
D	7	6	5	4	3	2	1
C	7	6	5	4	3	2	1
B	7	6	5	4	3	2	1
A	7	6	5	4	3	2	1
D	7	6	5	4	3	2	1
C	7	6	5	4	3	2	1
B	7	6	5	4	3	2	1
A	7	6	5	4	3	2	1
D	7	6	5	4	3	2	1
C	7	6	5	4	3	2	1
B	7	6	5	4	3	2	1
A	7	6	5	4	3	2	1

NA  
U1

RRING13	AL2	RRING	DS26519_U	PORT	RRING15	A6	RRING	DS26519_U	PORT	RRING15	A6	RRING	DS26519_U	PORT	TRINGA	DB	IRING15
RTIP13	AL1	RTIP			RTIP15	B6	RTIP			RTIP15	B7	RTIP			TRINGB	EB	ITIP15
RTIPE13	AL3	RTIPE			RTIPE15	A7	RTIPE			RTIPE15	A7	RTIPE			TTIPB	E7	ITIP15
RCHBLK13	HE	RCHBLK			RCHBLK15	H14	RCHBLK			RCHBLK15	H14	RCHBLK			TCHBK	Y22	ICHBLK15
RCLK13	W1	RCLK			RCLK15	W1	RCLK			RCLK15	W1	RCLK			TCLK	P21	ICLK15
RSER13	J4	RSER			RSER15	H13	RSER			RSER15	H13	RSER			TSER	H15	ISER15
RSIG13	J3	RSIG			RSIG15	J14	RSIG			RSIG15	J14	RSIG			TSIG	G14	ISIG15
RSYNCL13	W1	RSYNC			RSYNCL15	W1	RSYNC			RSYNCL15	W1	RSYNC			TSYNC	G14	ISYNCL15
RSYSCLK13	FB	RSYSCLK			RSYSCLK15	G15	RSYSCLK			RSYSCLK15	G15	RSYSCLK			TSYSCLK	E16	ISYSCLK15
RMSYNCL13	G1	RMSYNC			RMSYNCL15	F15	RMSYNC			RMSYNCL15	F15	RMSYNC			TSYSCLK	E16	ISYSCLK15

NA  
U1

RRING14	BB	RRING	DS26519_U	PORT	RRING16	N2	RRING	DS26519_U	PORT	RRING16	N2	RRING	DS26519_U	PORT	TRINGA	M3	IRING16
RTIP14	AB	RTIP			RTIP16	N1	RTIP			RTIP16	N1	RTIP			TRINGB	L3	ITIP16
RTIPE14	BB	RTIPE			RTIPE16	M1	RTIPE			RTIPE16	M1	RTIPE			TTIPB	M4	ITIP16
RCHBLK14	U17	RCHBLK			RCHBLK16	R16	RCHBLK			RCHBLK16	R16	RCHBLK			TCHBK	F16	ICHBLK16
RCLK14	W1	RCLK			RCLK16	W1	RCLK			RCLK16	W1	RCLK			TCLK	D17	ICLK16
RSER14	P7	RSER			RSER16	M16	RSER			RSER16	M16	RSER			TSER	F17	ISER16
RSIG14	K3	RSIG			RSIG16	P15	RSIG			RSIG16	P15	RSIG			TSIG	G17	ISIG16
RSYNCL14	W1	RSYNC			RSYNCL16	W1	RSYNC			RSYNCL16	W1	RSYNC			TSYNC	G17	ISYNCL16
RSYSCLK14	R7	RSYSCLK			RSYSCLK16	T19	RSYSCLK			RSYSCLK16	T19	RSYSCLK			TSYSCLK	M17	ISYSCLK16
RMSYNCL14	K4	RMSYNC			RMSYNCL16	N17	RMSYNC			RMSYNCL16	N17	RMSYNC			TSYSCLK	M17	ISYSCLK16

NA  
U1

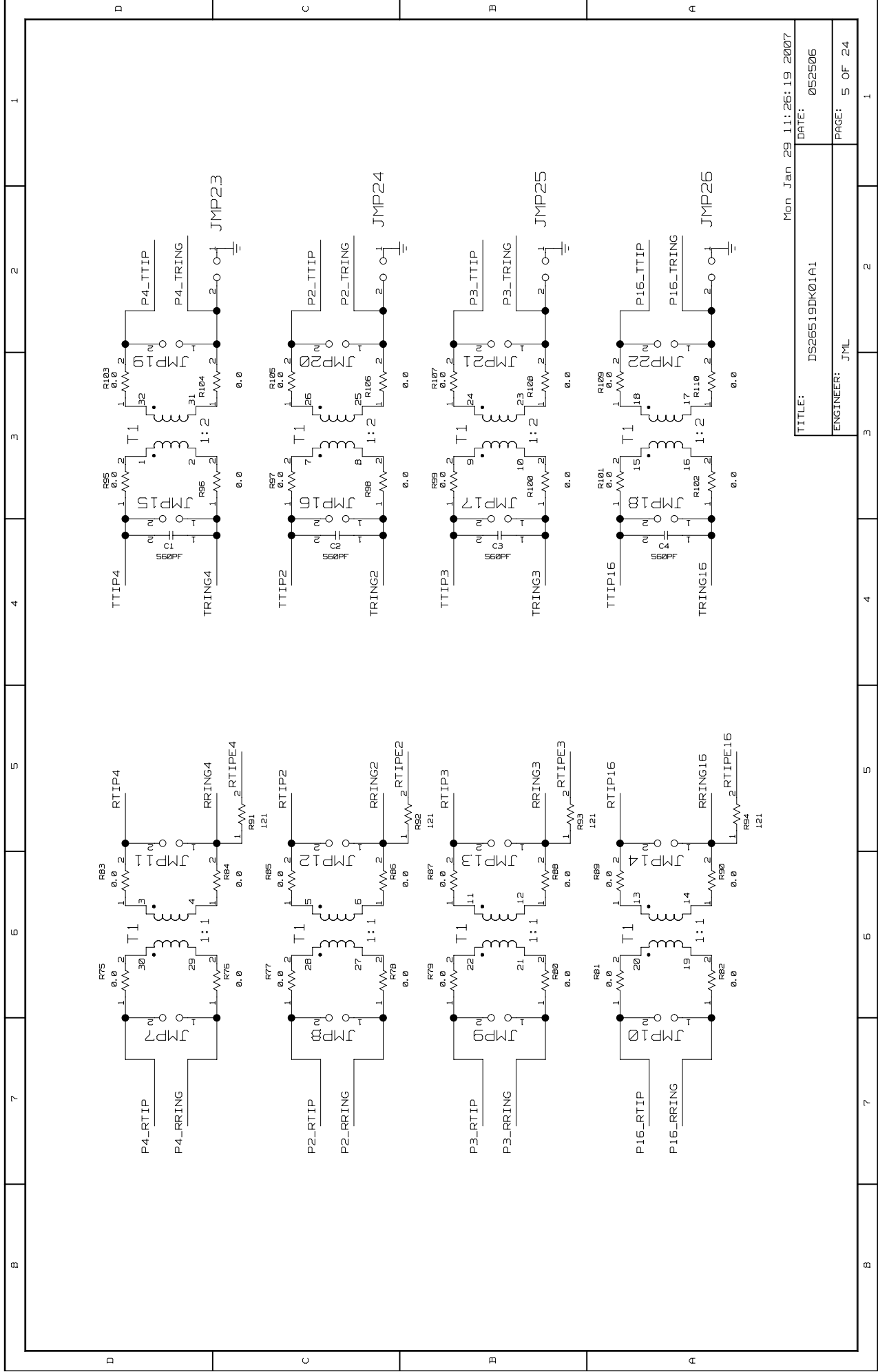
RRING14	BB	RRING	DS26519_U	PORT	RRING16	N2	RRING	DS26519_U	PORT	RRING16	N2	RRING	DS26519_U	PORT	TRINGA	M3	IRING16
RTIP14	AB	RTIP			RTIP16	N1	RTIP			RTIP16	N1	RTIP			TRINGB	L3	ITIP16
RTIPE14	BB	RTIPE			RTIPE16	M1	RTIPE			RTIPE16	M1	RTIPE			TTIPB	M4	ITIP16
RCHBLK14	U17	RCHBLK			RCHBLK16	R16	RCHBLK			RCHBLK16	R16	RCHBLK			TCHBK	F16	ICHBLK16
RCLK14	W1	RCLK			RCLK16	W1	RCLK			RCLK16	W1	RCLK			TCLK	D17	ICLK16
RSER14	P7	RSER			RSER16	M16	RSER			RSER16	M16	RSER			TSER	F17	ISER16
RSIG14	K3	RSIG			RSIG16	P15	RSIG			RSIG16	P15	RSIG			TSIG	G17	ISIG16
RSYNCL14	W1	RSYNC			RSYNCL16	W1	RSYNC			RSYNCL16	W1	RSYNC			TSYNC	G17	ISYNCL16
RSYSCLK14	R7	RSYSCLK			RSYSCLK16	T19	RSYSCLK			RSYSCLK16	T19	RSYSCLK			TSYSCLK	M17	ISYSCLK16
RMSYNCL14	K4	RMSYNC			RMSYNCL16	N17	RMSYNC			RMSYNCL16	N17	RMSYNC			TSYSCLK	M17	ISYSCLK16

NA  
U1

RRING14	BB	RRING	DS26519_U	PORT	RRING16	N2	RRING	DS26519_U	PORT	RRING16	N2	RRING	DS26519_U	PORT	TRINGA	M3	IRING16
RTIP14	AB	RTIP			RTIP16	N1	RTIP			RTIP16	N1	RTIP			TRINGB	L3	ITIP16
RTIPE14	BB	RTIPE			RTIPE16	M1	RTIPE			RTIPE16	M1	RTIPE			TTIPB	M4	ITIP16
RCHBLK14	U17	RCHBLK			RCHBLK16	R16	RCHBLK			RCHBLK16	R16	RCHBLK			TCHBK	F16	ICHBLK16
RCLK14	W1	RCLK			RCLK16	W1	RCLK			RCLK16	W1	RCLK			TCLK	D17	ICLK16
RSER14	P7	RSER			RSER16	M16	RSER			RSER16	M16	RSER			TSER	F17	ISER16
RSIG14	K3	RSIG			RSIG16	P15	RSIG			RSIG16	P15	RSIG			TSIG	G17	ISIG16
RSYNCL14	W1	RSYNC			RSYNCL16	W1	RSYNC			RSYNCL16	W1	RSYNC			TSYNC	G17	ISYNCL16
RSYSCLK14	R7	RSYSCLK			RSYSCLK16	T19	RSYSCLK			RSYSCLK16	T19	RSYSCLK			TSYSCLK	M17	ISYSCLK16
RMSYNCL14	K4	RMSYNC			RMSYNCL16	N17	RMSYNC			RMSYNCL16	N17	RMSYNC			TSYSCLK	M17	ISYSCLK16

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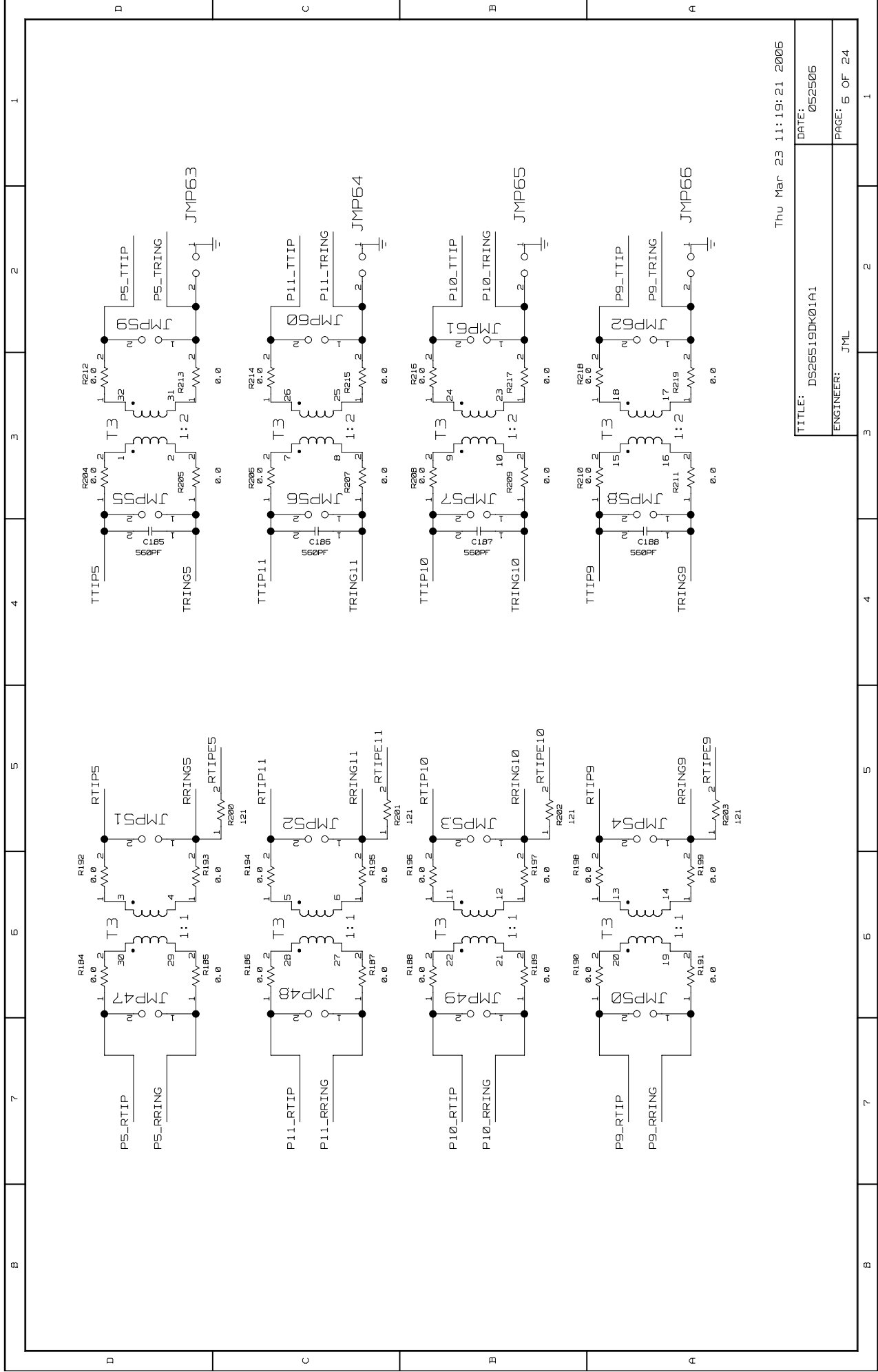
4

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1

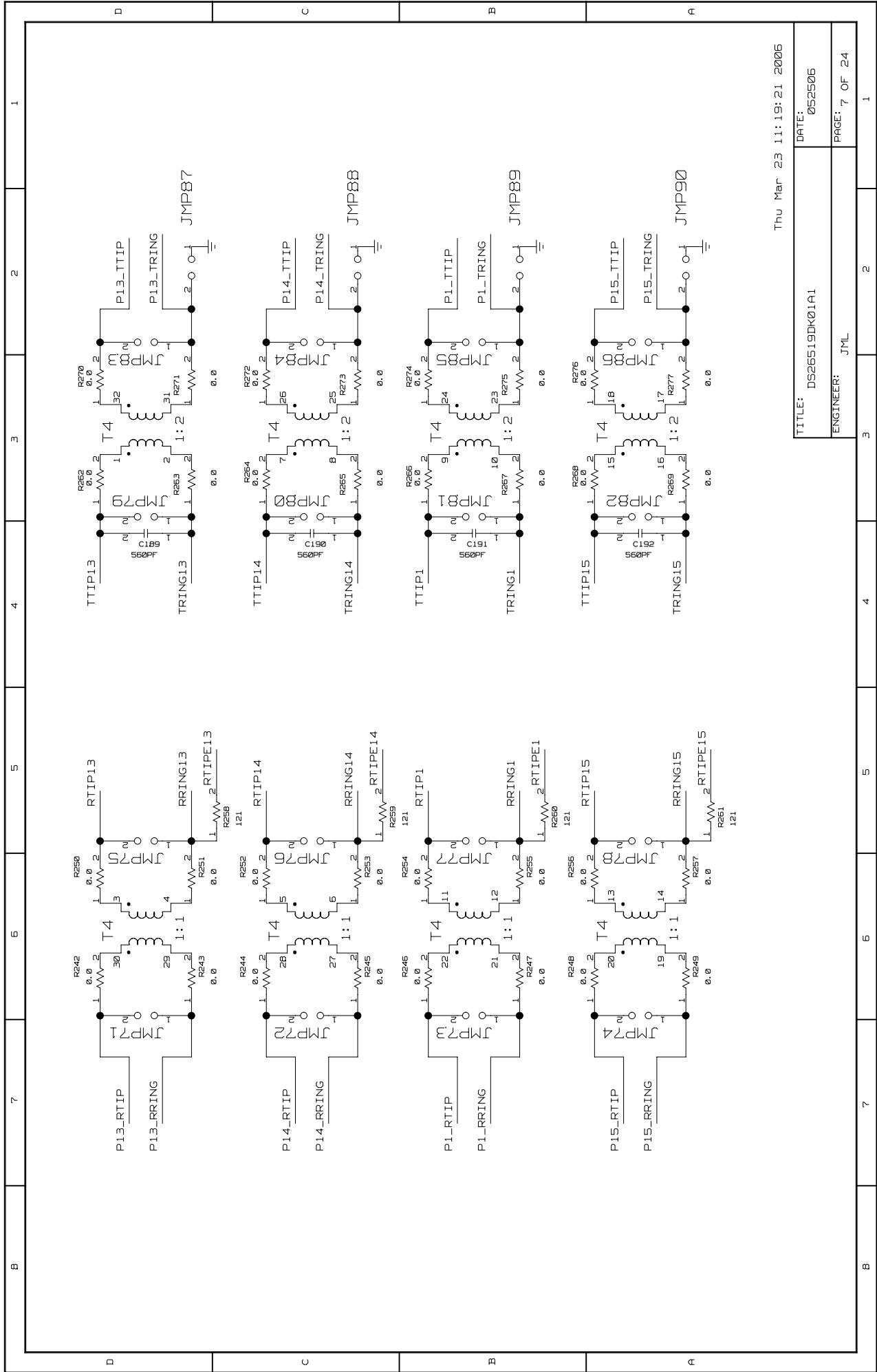


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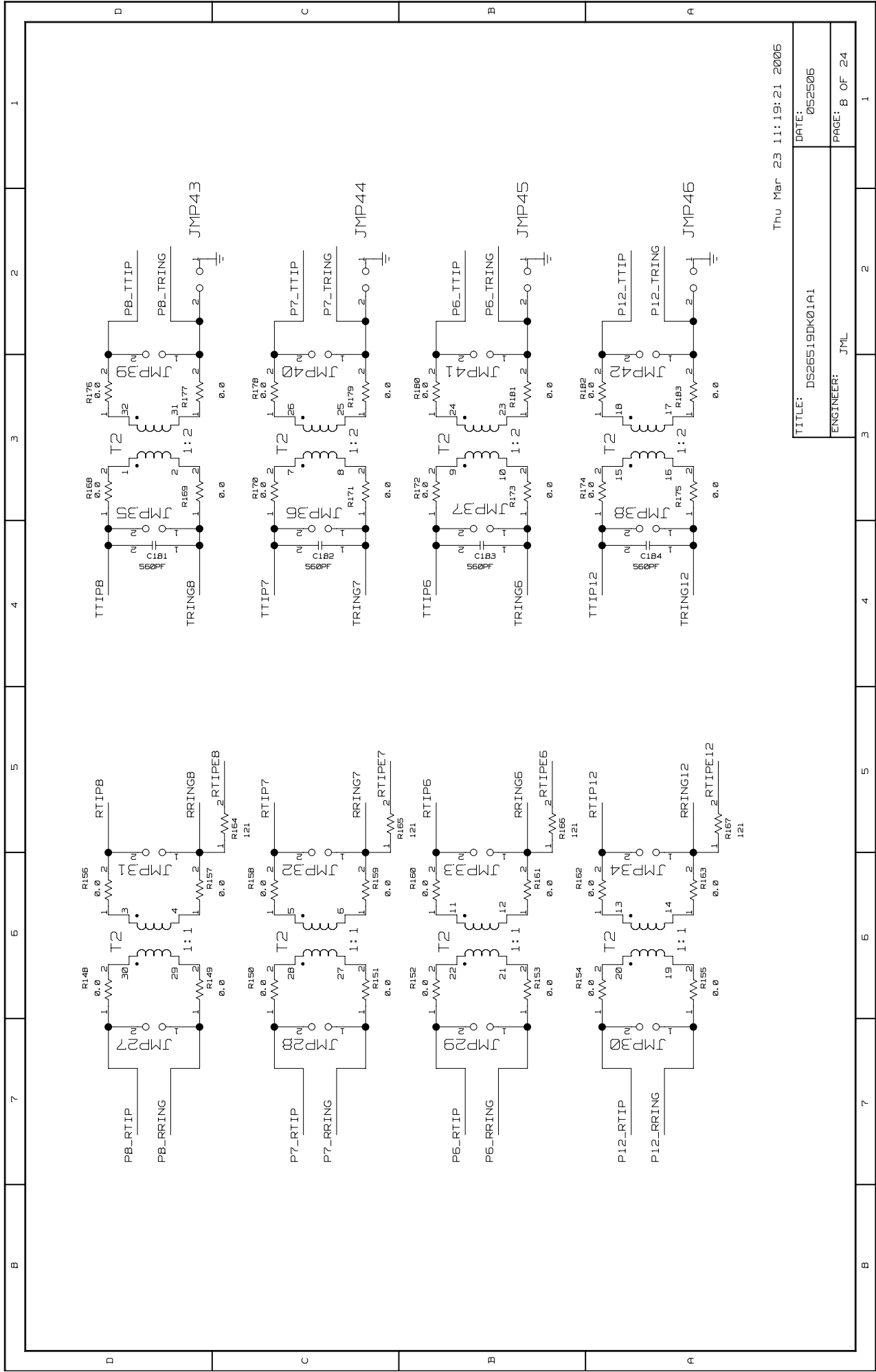
Thu Mar 23 11:19:21 2006

TITLE: DS26519DK01A1

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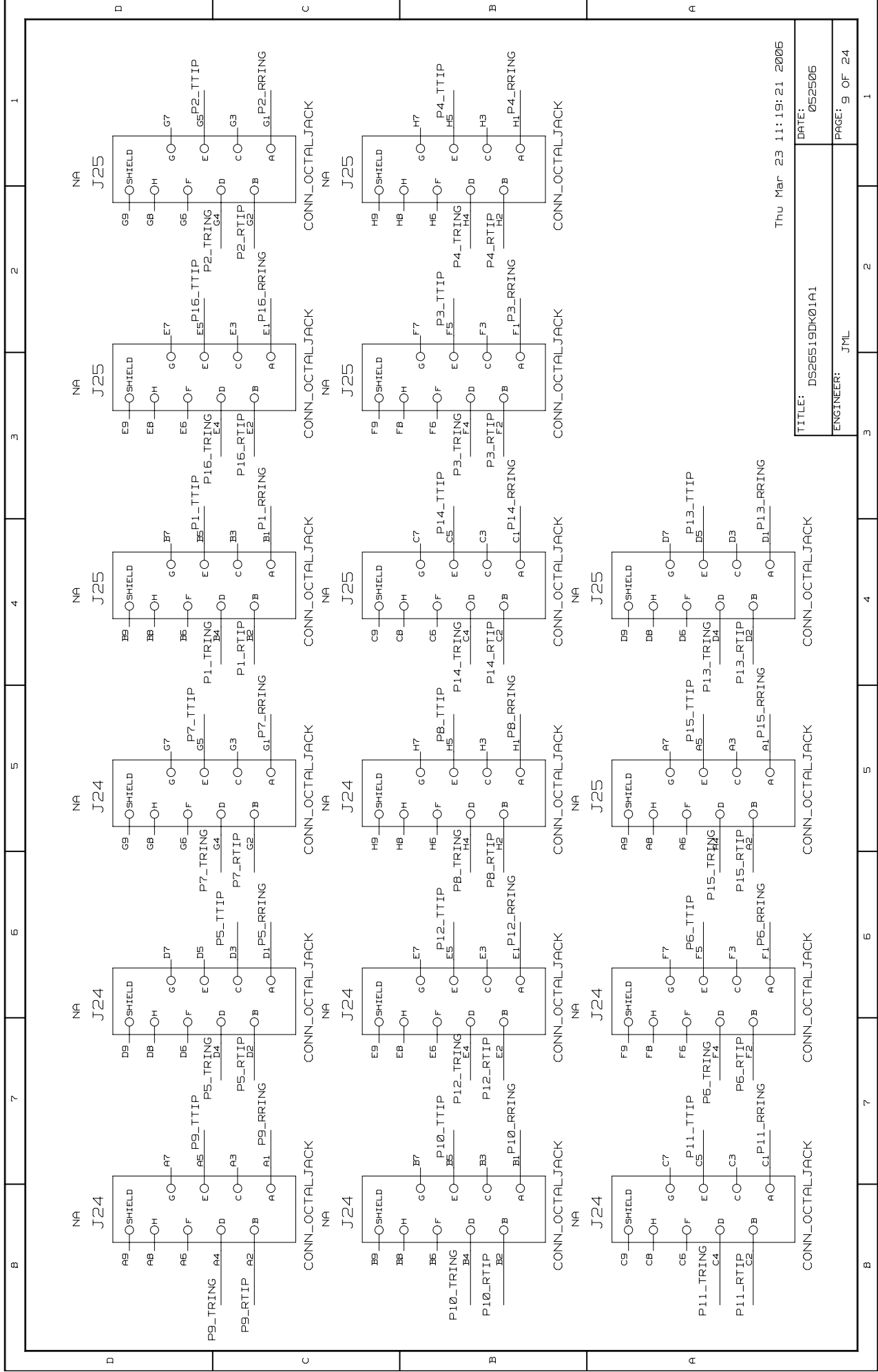


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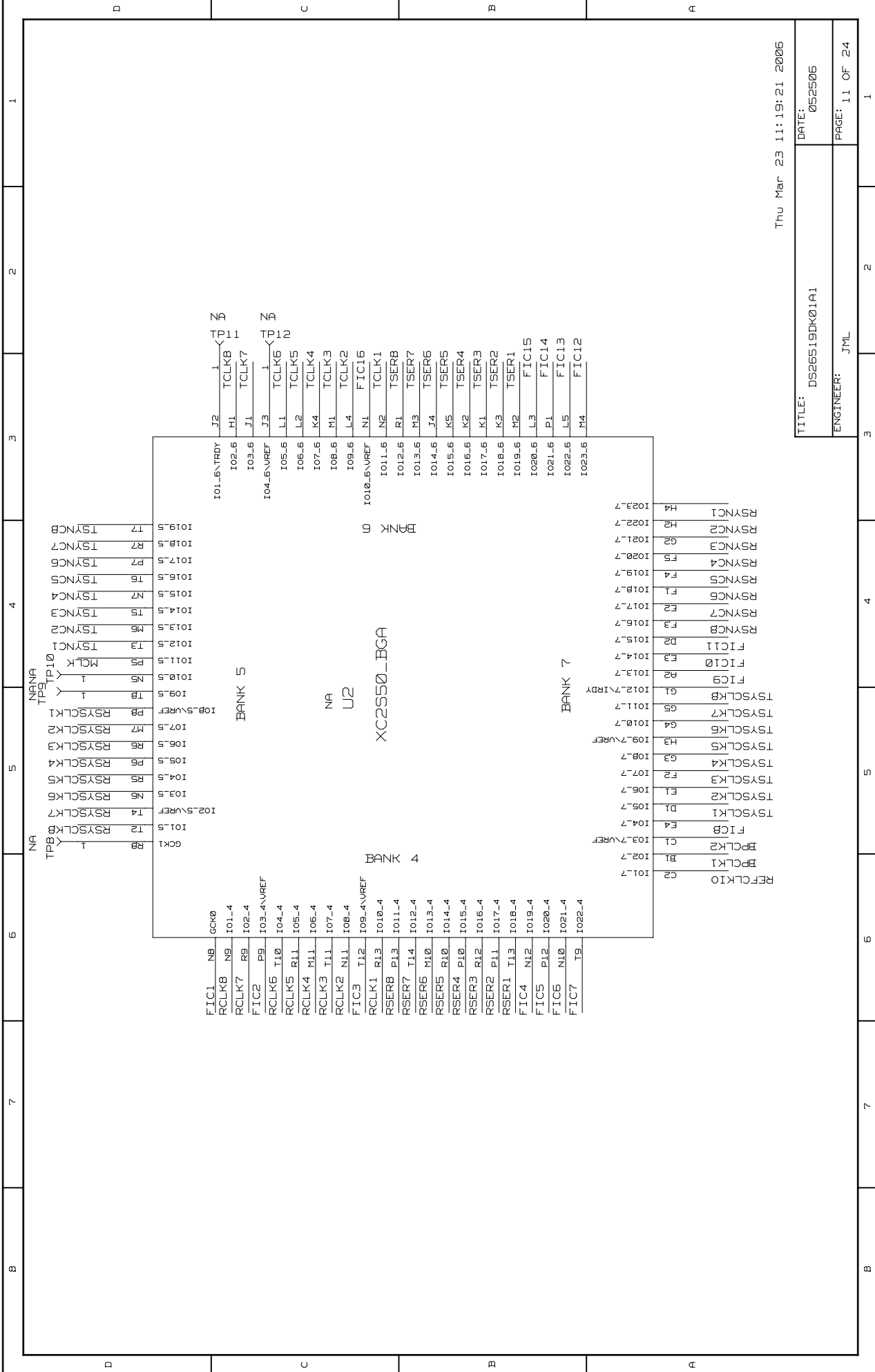
D C B A

TITLE: DS26519DK01A1  
 ENGINEER: JML

DATE: Thu Mar 23 11:19:21 2006  
 DATE: 052506

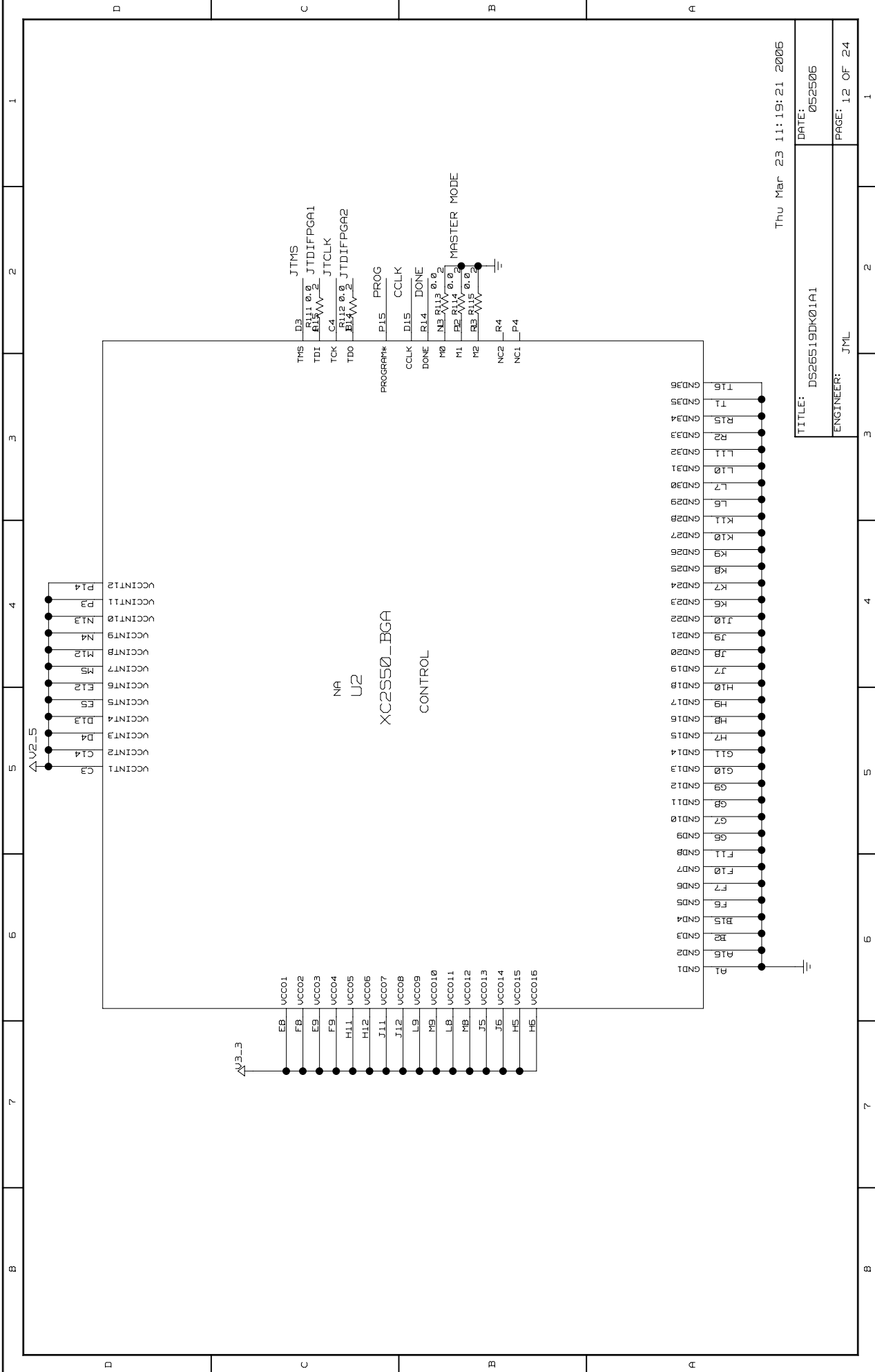
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U3\_3

U2\_5

TMS B3 JTMS  
 TDI B11 0.2 JTDIFPGAL  
 TCK C4 JTDIFPGAL  
 TDO B12 0.2 JTDIFPGAL  
 B14  
 PROGRAM P15 PROG  
 CCLK D15 CCLK  
 DONE R14 DONE  
 M0 B3 R13 0.2  
 M1 B2 R14 0.2 MASTER MODE  
 M2 B3 R15 0.2  
 NC2 R4  
 NC1 P4

NA  
 U2  
 XC2S50\_BGA  
 CONTROL

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B	7	6	5	4	3	2	1	
D	C	B	A					
CLOCK2 PD31 PD30 PD29 PD28 PD27 PD26 PD25 PD24 PA14 PA13 PA12 PA11 PA10 PA9 PA8 PA7 PA6 PA5 PA4 PA3	BB GCK3 A7 I01.0 B7 I02.0\NREF C7 I03.0 B6 I04.0 A5 I05.0 C5 I06.0 B4 I07.0\NREF A3 I08.0 B3 I09.0 D8 I010.0 A6 I011.0 C8 I012.0 D7 I013.0 E7 I014.0 B5 I015.0 D6 I016.0 A4 I017.0 E6 I018.0 D5 I019.0 C5 I020.0	OSC2_1544 GCK2 I01.1\CS* B13 ICOC10 I02.1\WRITE* C13 ICOC11 I03.1 A14 OF I04.1\NREF C11 RM E11 ICOC12 I05.1 B11 ICOC13 CS_BRD I06.1 A11 ICOC20 I07.1 B1 ICOC21 I08.1 C10 ICOC22 I09.1\NREF B9 I10.1 D9 PD16 I11.1 B8 PD17 I12.1 C12 PD18 I13.1 D12 PD19 I14.1 B12 PD20 I15.1 A13 PD21 I16.1 D11 PD22 I17.1 A12 PD23 I18.1 B10 ICOC23 I19.1 D10 PD24 I20.1 A10 ICOC25 I21.1 B9 RSTOUT I22.1 A9	NA U12 XC2S50_BGA BANK 0 BANK 1 BANK 2 BANK 3	I02.1\NIRDY I02.2\NREF I03.2\N3 I04.2 I05.2 I06.2\N2 I07.2\N1 I08.2 I09.2 I10.2\NREF I11.2 I12.2\N(DIN, D0) I13.2\N(DOUT, BUSY) I14.2 I15.2 I16.2 I17.2 I18.2 I19.2 I20.2 I21.2 I22.2 I23.2 I24.2	H16 D7_CPOL H15 D6_CPHA G16 D5_SWAP D4 D3 F15 D2_SCLK E16 D1_MOSI F14 D0_MISO D16 F13 A11 E13 A10 D14 FPGA2_DIN C15 H14 AB J13 A7 G14 A6 G15 A5 G12 A4 F16 A3 F12 A2 E15 A1 E14 A0 C16 A1.3 B16 A1.4	1023.3 J14 1022.3 K12 1021.3 INT2 1020.3 INT3 1019.3 INT4 1018.3 INT4 1017.3 PORN0T 1016.3 ONCE_RESET 1015.3 SS 1014.3 SCK 1013.3 MIS0 1012.3 MOSI 1011.3 CLROUT 1010.3 TP47 1009.3 TP46 1008.3 TP45 1007.3 TP44 1006.3 TP43 1005.3 PA15 1004.3 INT_S19 1003.3 PA0 1002.3 PA1 1001.3 PA2 1000.3 FPGA_INIT	DS26S19DKK01A1 JML DATE: 052506 PAGE: 13 OF 24	Mon Jan 29 12:59:52 2007

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101.5VTRDY J2      1      TP40  
 102.6 H1      TCLK16  
 103.6 J1      TCLK15      TP41 ~~10~~  
 104.6VUREF J3      1      TP42  
 105.6 L1      TCLK14  
 106.6 L2      TCLK13  
 107.6 K4      TCLK12  
 108.6 M1      TCLK11  
 109.6 L4      TCLK10  
 1010.6VUREF N1      FIC16  
 1011.6 N2      TCLK9  
 1012.6 R1      TSER16  
 1013.6 M3      TSER15  
 1014.6 J4      TSER14  
 1015.6 K5      TSER13  
 1016.6 K2      TSER12  
 1017.6 K1      TSER11  
 1018.6 K3      TSER10  
 1019.6 M2      TSER9  
 1020.6 L3      FIC15  
 1021.6 P1      FIC14  
 1022.6 L5      FIC13  
 1023.6 M4      FIC12

1019.5 T7      TSYNC16  
 1018.5 R7      TSYNC15  
 1017.5 P7      TSYNC14  
 1016.5 T6      TSYNC13  
 1015.5 N7      TSYNC12  
 1014.5 T5      TSYNC11  
 1013.5 M6      TSYNC10  
 1012.5 T3      TSYNC9  
 1011.5 P5      MCLK  
 1010.5 N5      1      TP39  
 109.5 T8      1      TP38  
 108.5VUREF P8      RSYCLK9  
 107.5 M7      RSYCLK10  
 106.5 R6      RSYCLK11  
 105.5 P6      RSYCLK12  
 104.5 R5      RSYCLK13  
 103.5 N6      RSYCLK14  
 102.5VUREF T4      RSYCLK15  
 101.5 T2      RSYCLK16  
 101.5 GCK1      1      TP37

101.7 G2      REFCLK10  
 102.7 B1      BCLK1  
 103.7 C1      FIB  
 104.7 E4      TSYCLK16  
 105.7 D1      TSYCLK15  
 106.7 E1      TSYCLK14  
 107.7 F2      TSYCLK13  
 108.7 G3      TSYCLK12  
 109.7VUREF H3      TSYCLK11  
 1010.7 G4      TSYCLK10  
 1011.7 G5      TSYCLK9  
 1012.7VTRDY G1      1      IRDY  
 1013.7 R2      FIC9  
 1014.7 E3      FIC10  
 1015.7 D2      FIC11  
 1016.7 F3      RSYNC16  
 1017.7 E2      RSYNC15  
 1018.7 F1      RSYNC14  
 1019.7 F4      RSYNC13  
 1020.7 F5      RSYNC12  
 1021.7 G2      RSYNC11  
 1022.7 H2      RSYNC10  
 1023.7 H4      RSYNC9

101.7 G2      REFCLK10  
 102.7 B1      BCLK1  
 103.7 C1      FIB  
 104.7 E4      TSYCLK16  
 105.7 D1      TSYCLK15  
 106.7 E1      TSYCLK14  
 107.7 F2      TSYCLK13  
 108.7 G3      TSYCLK12  
 109.7VUREF H3      TSYCLK11  
 1010.7 G4      TSYCLK10  
 1011.7 G5      TSYCLK9  
 1012.7VTRDY G1      1      IRDY  
 1013.7 R2      FIC9  
 1014.7 E3      FIC10  
 1015.7 D2      FIC11  
 1016.7 F3      RSYNC16  
 1017.7 E2      RSYNC15  
 1018.7 F1      RSYNC14  
 1019.7 F4      RSYNC13  
 1020.7 F5      RSYNC12  
 1021.7 G2      RSYNC11  
 1022.7 H2      RSYNC10  
 1023.7 H4      RSYNC9

101.7 G2      REFCLK10  
 102.7 B1      BCLK1  
 103.7 C1      FIB  
 104.7 E4      TSYCLK16  
 105.7 D1      TSYCLK15  
 106.7 E1      TSYCLK14  
 107.7 F2      TSYCLK13  
 108.7 G3      TSYCLK12  
 109.7VUREF H3      TSYCLK11  
 1010.7 G4      TSYCLK10  
 1011.7 G5      TSYCLK9  
 1012.7VTRDY G1      1      IRDY  
 1013.7 R2      FIC9  
 1014.7 E3      FIC10  
 1015.7 D2      FIC11  
 1016.7 F3      RSYNC16  
 1017.7 E2      RSYNC15  
 1018.7 F1      RSYNC14  
 1019.7 F4      RSYNC13  
 1020.7 F5      RSYNC12  
 1021.7 G2      RSYNC11  
 1022.7 H2      RSYNC10  
 1023.7 H4      RSYNC9

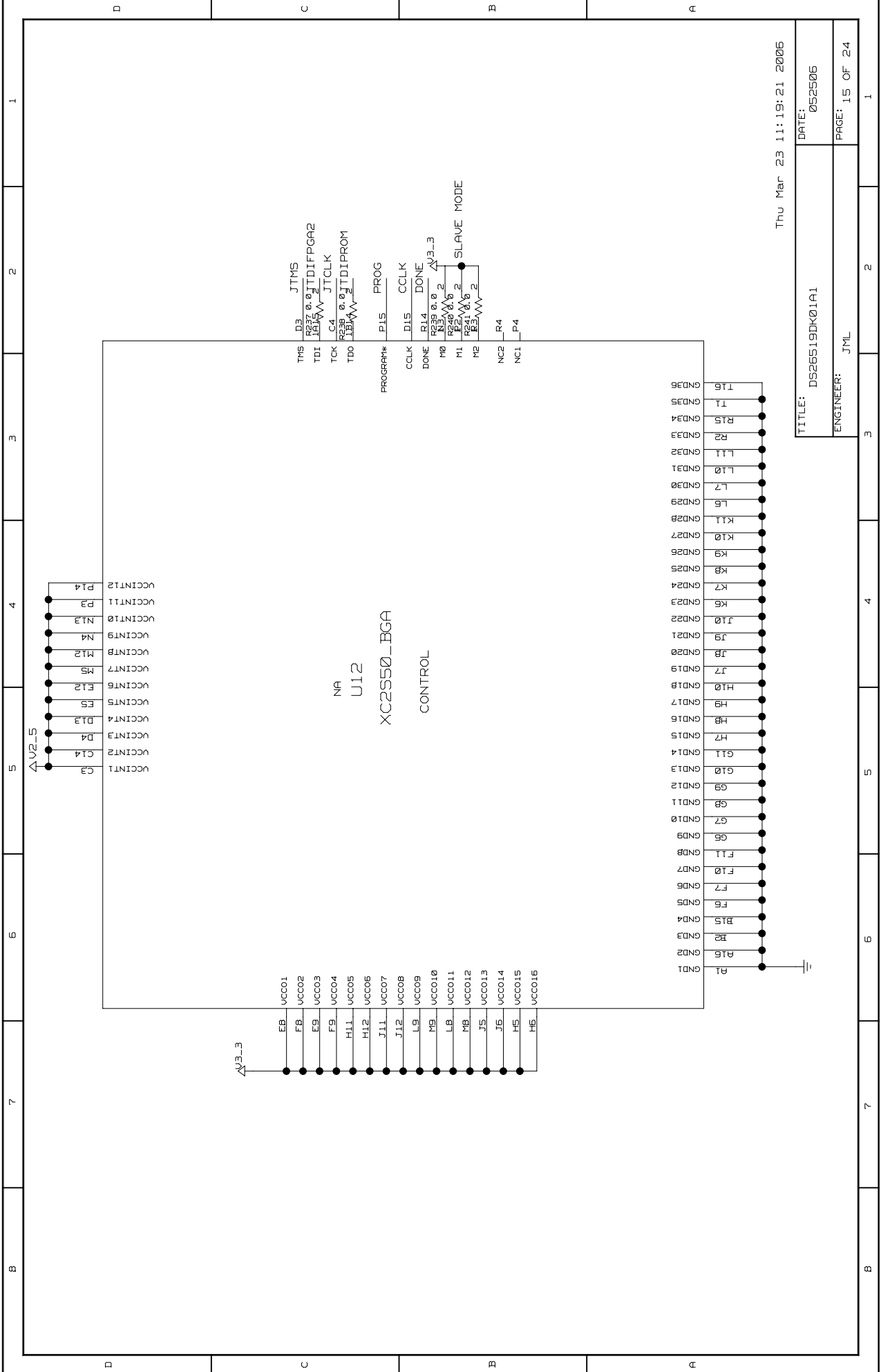
101.7 G2      REFCLK10  
 102.7 B1      BCLK1  
 103.7 C1      FIB  
 104.7 E4      TSYCLK16  
 105.7 D1      TSYCLK15  
 106.7 E1      TSYCLK14  
 107.7 F2      TSYCLK13  
 108.7 G3      TSYCLK12  
 109.7VUREF H3      TSYCLK11  
 1010.7 G4      TSYCLK10  
 1011.7 G5      TSYCLK9  
 1012.7VTRDY G1      1      IRDY  
 1013.7 R2      FIC9  
 1014.7 E3      FIC10  
 1015.7 D2      FIC11  
 1016.7 F3      RSYNC16  
 1017.7 E2      RSYNC15  
 1018.7 F1      RSYNC14  
 1019.7 F4      RSYNC13  
 1020.7 F5      RSYNC12  
 1021.7 G2      RSYNC11  
 1022.7 H2      RSYNC10  
 1023.7 H4      RSYNC9

101.7 G2      REFCLK10  
 102.7 B1      BCLK1  
 103.7 C1      FIB  
 104.7 E4      TSYCLK16  
 105.7 D1      TSYCLK15  
 106.7 E1      TSYCLK14  
 107.7 F2      TSYCLK13  
 108.7 G3      TSYCLK12  
 109.7VUREF H3      TSYCLK11  
 1010.7 G4      TSYCLK10  
 1011.7 G5      TSYCLK9  
 1012.7VTRDY G1      1      IRDY  
 1013.7 R2      FIC9  
 1014.7 E3      FIC10  
 1015.7 D2      FIC11  
 1016.7 F3      RSYNC16  
 1017.7 E2      RSYNC15  
 1018.7 F1      RSYNC14  
 1019.7 F4      RSYNC13  
 1020.7 F5      RSYNC12  
 1021.7 G2      RSYNC11  
 1022.7 H2      RSYNC10  
 1023.7 H4      RSYNC9

101.7 G2      REFCLK10  
 102.7 B1      BCLK1  
 103.7 C1      FIB  
 104.7 E4      TSYCLK16  
 105.7 D1      TSYCLK15  
 106.7 E1      TSYCLK14  
 107.7 F2      TSYCLK13  
 108.7 G3      TSYCLK12  
 109.7VUREF H3      TSYCLK11  
 1010.7 G4      TSYCLK10  
 1011.7 G5      TSYCLK9  
 1012.7VTRDY G1      1      IRDY  
 1013.7 R2      FIC9  
 1014.7 E3      FIC10  
 1015.7 D2      FIC11  
 1016.7 F3      RSYNC16  
 1017.7 E2      RSYNC15  
 1018.7 F1      RSYNC14  
 1019.7 F4      RSYNC13  
 1020.7 F5      RSYNC12  
 1021.7 G2      RSYNC11  
 1022.7 H2      RSYNC10  
 1023.7 H4      RSYNC9

101.7 G2      REFCLK10  
 102.7 B1      BCLK1  
 103.7 C1      FIB  
 104.7 E4      TSYCLK16  
 105.7 D1      TSYCLK15  
 106.7 E1      TSYCLK14  
 107.7 F2      TSYCLK13  
 108.7 G3      TSYCLK12  
 109.7VUREF H3      TSYCLK11  
 1010.7 G4      TSYCLK10  
 1011.7 G5      TSYCLK9  
 1012.7VTRDY G1      1      IRDY  
 1013.7 R2      FIC9  
 1014.7 E3      FIC10  
 1015.7 D2      FIC11  
 1016.7 F3      RSYNC16  
 1017.7 E2      RSYNC15  
 1018.7 F1      RSYNC14  
 1019.7 F4      RSYNC13  
 1020.7 F5      RSYNC12  
 1021.7 G2      RSYNC11  
 1022.7 H2      RSYNC10  
 1023.7 H4      RSYNC9





U3\_3

EB VCC01  
 FB VCC02  
 E9 VCC03  
 F9 VCC04  
 H11 VCC05  
 H12 VCC06  
 J11 VCC07  
 J12 VCC08  
 L9 VCC09  
 M9 VCC010  
 LB VCC011  
 MB VCC012  
 JS VCC013  
 JB VCC014  
 HS VCC015  
 HE VCC016

XC2S50\_BGA  
 CONTROL

TMS JTMS  
 TDI TDIIFPGA2  
 TCK JTCLK  
 TDO TDIIPROM

PROGRAM P15 PROG  
 CCLK DL15 CCLK  
 DONE RL4 DONE  
 M0 M2  
 M1 M2 SLAVE MODE  
 NC2 R4  
 NC1 P4

U2\_5  
 VCCINT1 C3  
 VCCINT2 C4  
 VCCINT3 D4  
 VCCINT4 D3  
 VCCINT5 E5  
 VCCINT6 E2  
 VCCINT7 M5  
 VCCINT8 M2  
 VCCINT9 N4  
 VCCINT10 N3  
 VCCINT11 P3  
 VCCINT12 P4

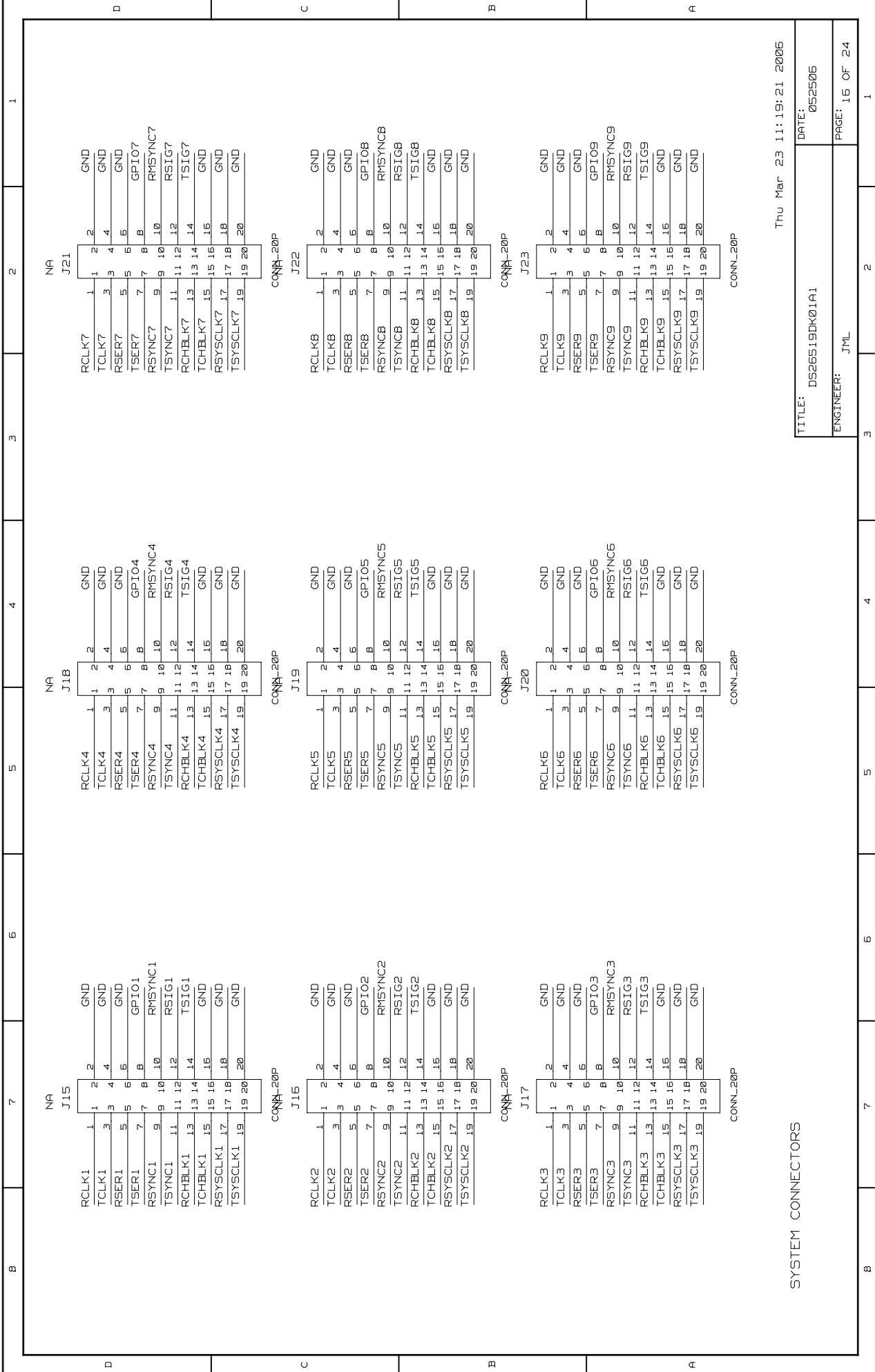
R1  
 R16  
 R2  
 R3  
 R4  
 R5  
 R6  
 R7  
 R8  
 R9  
 F11  
 F10  
 F7  
 F6  
 B15  
 B2  
 B16  
 GND1  
 GND2  
 GND3  
 GND4  
 GND5  
 GND6  
 GND7  
 GND8  
 GND9  
 GND10  
 GND11  
 GND12  
 GND13  
 GND14  
 GND15  
 H7  
 H8  
 H9  
 H10  
 J7  
 J8  
 J9  
 J10  
 K6  
 K7  
 K8  
 K9  
 K10  
 K11  
 L6  
 L7  
 L10  
 L11  
 R2  
 R15  
 T1  
 T16  
 GND16

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B 1 2 3 4 5 6 7

D C B A 1 2 3 4 5 6 7



1 2 3 4 5 6 7

CONN\_20P J21  
 RCLK7 1 2 GND  
 TCLK7 3 4 GND  
 RSER7 5 6 GND  
 TSER7 7 8 GPIO7  
 RSYNC7 9 10 RMSG7  
 TSYNC7 11 12 RMSG7  
 TCHBLK7 13 14 15 16 GND  
 RSYSCLK7 17 18 GND  
 TSYSCLK7 19 20 GND

CONN\_20P J18  
 RCLK4 1 2 GND  
 TCLK4 3 4 GND  
 RSER4 5 6 GND  
 TSER4 7 8 GPIO4  
 RSYNC4 9 10 RMSG4  
 TSYNC4 11 12 RMSG4  
 TCHBLK4 13 14 15 16 GND  
 RSYSCLK4 17 18 GND  
 TSYSCLK4 19 20 GND

CONN\_20P J15  
 RCLK1 1 2 GND  
 TCLK1 3 4 GND  
 RSER1 5 6 GND  
 TSER1 7 8 GPIO1  
 RSYNC1 9 10 RMSG1  
 TSYNC1 11 12 RMSG1  
 TCHBLK1 13 14 15 16 GND  
 RSYSCLK1 17 18 GND  
 TSYSCLK1 19 20 GND

CONN\_20P J12  
 RCLK2 1 2 GND  
 TCLK2 3 4 GND  
 RSER2 5 6 GND  
 TSER2 7 8 GPIO2  
 RSYNC2 9 10 RMSG2  
 TSYNC2 11 12 RMSG2  
 TCHBLK2 13 14 15 16 GND  
 RSYSCLK2 17 18 GND  
 TSYSCLK2 19 20 GND

CONN\_20P J20  
 RCLK6 1 2 GND  
 TCLK6 3 4 GND  
 RSER6 5 6 GND  
 TSER6 7 8 GPIO6  
 RSYNC6 9 10 RMSG6  
 TSYNC6 11 12 RMSG6  
 TCHBLK6 13 14 15 16 GND  
 RSYSCLK6 17 18 GND  
 TSYSCLK6 19 20 GND

CONN\_20P J19  
 RCLK5 1 2 GND  
 TCLK5 3 4 GND  
 RSER5 5 6 GND  
 TSER5 7 8 GPIO5  
 RSYNC5 9 10 RMSG5  
 TSYNC5 11 12 RMSG5  
 TCHBLK5 13 14 15 16 GND  
 RSYSCLK5 17 18 GND  
 TSYSCLK5 19 20 GND

CONN\_20P J17  
 RCLK3 1 2 GND  
 TCLK3 3 4 GND  
 RSER3 5 6 GND  
 TSER3 7 8 GPIO3  
 RSYNC3 9 10 RMSG3  
 TSYNC3 11 12 RMSG3  
 TCHBLK3 13 14 15 16 GND  
 RSYSCLK3 17 18 GND  
 TSYSCLK3 19 20 GND

CONN\_20P J23  
 RCLK9 1 2 GND  
 TCLK9 3 4 GND  
 RSER9 5 6 GND  
 TSER9 7 8 GPIO9  
 RSYNC9 9 10 RMSG9  
 TSYNC9 11 12 RMSG9  
 TCHBLK9 13 14 15 16 GND  
 RSYSCLK9 17 18 GND  
 TSYSCLK9 19 20 GND

CONN\_20P J22  
 RCLK8 1 2 GND  
 TCLK8 3 4 GND  
 RSER8 5 6 GND  
 TSER8 7 8 GPIO8  
 RSYNC8 9 10 RMSG8  
 TSYNC8 11 12 RMSG8  
 TCHBLK8 13 14 15 16 GND  
 RSYSCLK8 17 18 GND  
 TSYSCLK8 19 20 GND

CONN\_20P J20  
 RCLK6 1 2 GND  
 TCLK6 3 4 GND  
 RSER6 5 6 GND  
 TSER6 7 8 GPIO6  
 RSYNC6 9 10 RMSG6  
 TSYNC6 11 12 RMSG6  
 TCHBLK6 13 14 15 16 GND  
 RSYSCLK6 17 18 GND  
 TSYSCLK6 19 20 GND

CONN\_20P J19  
 RCLK5 1 2 GND  
 TCLK5 3 4 GND  
 RSER5 5 6 GND  
 TSER5 7 8 GPIO5  
 RSYNC5 9 10 RMSG5  
 TSYNC5 11 12 RMSG5  
 TCHBLK5 13 14 15 16 GND  
 RSYSCLK5 17 18 GND  
 TSYSCLK5 19 20 GND

CONN\_20P J17  
 RCLK3 1 2 GND  
 TCLK3 3 4 GND  
 RSER3 5 6 GND  
 TSER3 7 8 GPIO3  
 RSYNC3 9 10 RMSG3  
 TSYNC3 11 12 RMSG3  
 TCHBLK3 13 14 15 16 GND  
 RSYSCLK3 17 18 GND  
 TSYSCLK3 19 20 GND

CONN\_20P J23  
 RCLK9 1 2 GND  
 TCLK9 3 4 GND  
 RSER9 5 6 GND  
 TSER9 7 8 GPIO9  
 RSYNC9 9 10 RMSG9  
 TSYNC9 11 12 RMSG9  
 TCHBLK9 13 14 15 16 GND  
 RSYSCLK9 17 18 GND  
 TSYSCLK9 19 20 GND

CONN\_20P J22  
 RCLK8 1 2 GND  
 TCLK8 3 4 GND  
 RSER8 5 6 GND  
 TSER8 7 8 GPIO8  
 RSYNC8 9 10 RMSG8  
 TSYNC8 11 12 RMSG8  
 TCHBLK8 13 14 15 16 GND  
 RSYSCLK8 17 18 GND  
 TSYSCLK8 19 20 GND

CONN\_20P J20  
 RCLK6 1 2 GND  
 TCLK6 3 4 GND  
 RSER6 5 6 GND  
 TSER6 7 8 GPIO6  
 RSYNC6 9 10 RMSG6  
 TSYNC6 11 12 RMSG6  
 TCHBLK6 13 14 15 16 GND  
 RSYSCLK6 17 18 GND  
 TSYSCLK6 19 20 GND

CONN\_20P J19  
 RCLK5 1 2 GND  
 TCLK5 3 4 GND  
 RSER5 5 6 GND  
 TSER5 7 8 GPIO5  
 RSYNC5 9 10 RMSG5  
 TSYNC5 11 12 RMSG5  
 TCHBLK5 13 14 15 16 GND  
 RSYSCLK5 17 18 GND  
 TSYSCLK5 19 20 GND

CONN\_20P J17  
 RCLK3 1 2 GND  
 TCLK3 3 4 GND  
 RSER3 5 6 GND  
 TSER3 7 8 GPIO3  
 RSYNC3 9 10 RMSG3  
 TSYNC3 11 12 RMSG3  
 TCHBLK3 13 14 15 16 GND  
 RSYSCLK3 17 18 GND  
 TSYSCLK3 19 20 GND

CONN\_20P J23  
 RCLK9 1 2 GND  
 TCLK9 3 4 GND  
 RSER9 5 6 GND  
 TSER9 7 8 GPIO9  
 RSYNC9 9 10 RMSG9  
 TSYNC9 11 12 RMSG9  
 TCHBLK9 13 14 15 16 GND  
 RSYSCLK9 17 18 GND  
 TSYSCLK9 19 20 GND

CONN\_20P J22  
 RCLK8 1 2 GND  
 TCLK8 3 4 GND  
 RSER8 5 6 GND  
 TSER8 7 8 GPIO8  
 RSYNC8 9 10 RMSG8  
 TSYNC8 11 12 RMSG8  
 TCHBLK8 13 14 15 16 GND  
 RSYSCLK8 17 18 GND  
 TSYSCLK8 19 20 GND

CONN\_20P J20  
 RCLK6 1 2 GND  
 TCLK6 3 4 GND  
 RSER6 5 6 GND  
 TSER6 7 8 GPIO6  
 RSYNC6 9 10 RMSG6  
 TSYNC6 11 12 RMSG6  
 TCHBLK6 13 14 15 16 GND  
 RSYSCLK6 17 18 GND  
 TSYSCLK6 19 20 GND

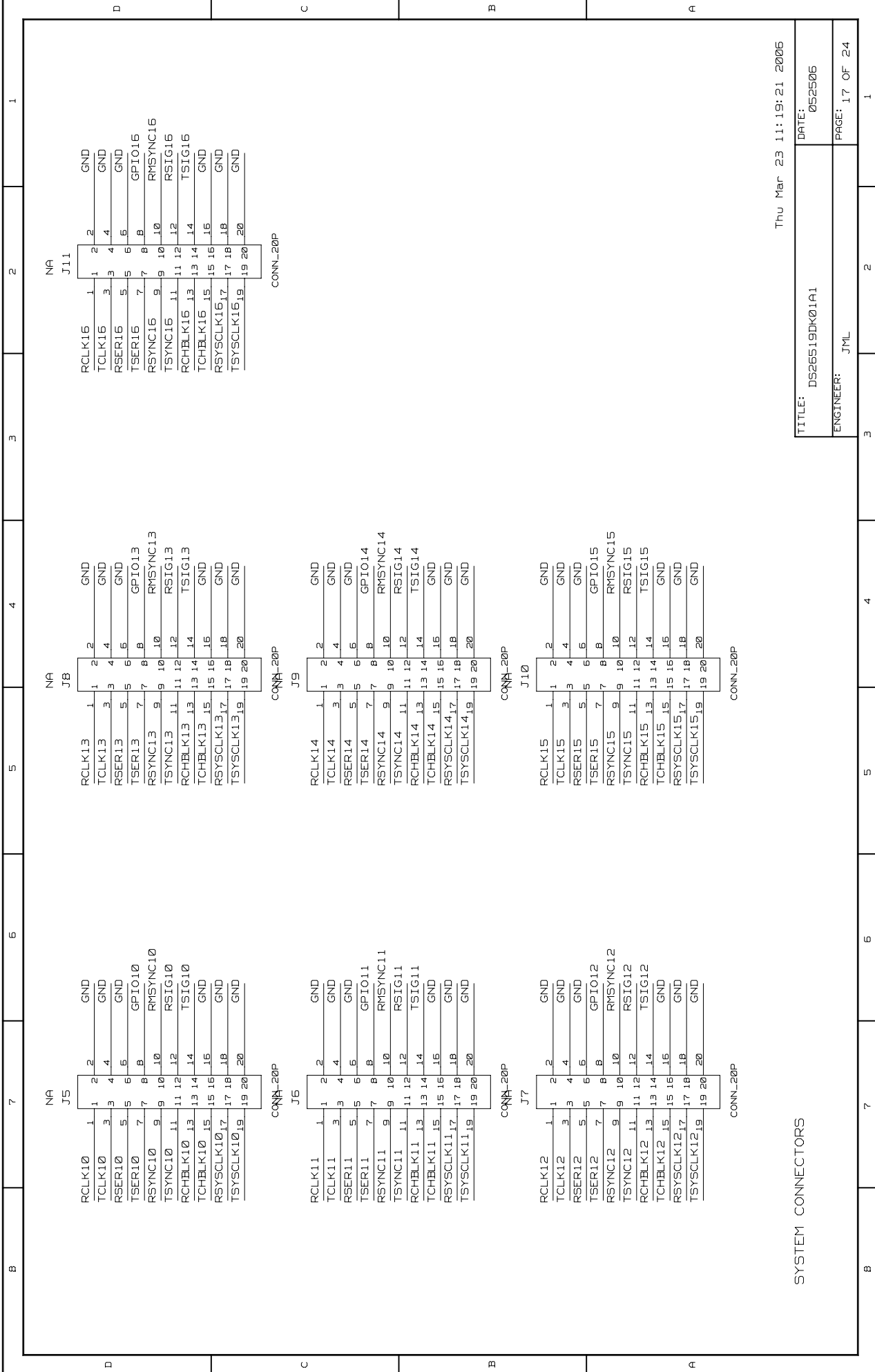
CONN\_20P J19  
 RCLK5 1 2 GND  
 TCLK5 3 4 GND  
 RSER5 5 6 GND  
 TSER5 7 8 GPIO5  
 RSYNC5 9 10 RMSG5  
 TSYNC5 11 12 RMSG5  
 TCHBLK5 13 14 15 16 GND  
 RSYSCLK5 17 18 GND  
 TSYSCLK5 19 20 GND

CONN\_20P J17  
 RCLK3 1 2 GND  
 TCLK3 3 4 GND  
 RSER3 5 6 GND  
 TSER3 7 8 GPIO3  
 RSYNC3 9 10 RMSG3  
 TSYNC3 11 12 RMSG3  
 TCHBLK3 13 14 15 16 GND  
 RSYSCLK3 17 18 GND  
 TSYSCLK3 19 20 GND

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SYSTEM CONNECTORS



CONN\_20P

NA  
J11

1	RCLK16	1	2	GND
2	TCLK16	3	4	GND
3	RSER16	5	6	GND
4	TSER16	7	8	GPIO16
5	RSYNC16	9	10	RMSG16
6	RCHBLK16	11	12	RSIG16
7	TCHBLK16	13	14	TSIG16
8	RSYCLK16	15	16	GND
9	TSYSCLK16	17	18	GND
10		19	20	GND

CONN\_20P

NA  
J10

1	RCLK15	1	2	GND
2	TCLK15	3	4	GND
3	RSER15	5	6	GND
4	TSER15	7	8	GPIO15
5	RSYNC15	9	10	RMSG15
6	RCHBLK15	11	12	RSIG15
7	TCHBLK15	13	14	TSIG15
8	RSYCLK15	15	16	GND
9	TSYSCLK15	17	18	GND
10		19	20	GND

CONN\_20P

NA  
J9

1	RCLK14	1	2	GND
2	TCLK14	3	4	GND
3	RSER14	5	6	GND
4	TSER14	7	8	GPIO14
5	RSYNC14	9	10	RMSG14
6	RCHBLK14	11	12	RSIG14
7	TCHBLK14	13	14	TSIG14
8	RSYCLK14	15	16	GND
9	TSYSCLK14	17	18	GND
10		19	20	GND

CONN\_20P

NA  
J8

1	RCLK13	1	2	GND
2	TCLK13	3	4	GND
3	RSER13	5	6	GND
4	TSER13	7	8	GPIO13
5	RSYNC13	9	10	RMSG13
6	RCHBLK13	11	12	RSIG13
7	TCHBLK13	13	14	TSIG13
8	RSYCLK13	15	16	GND
9	TSYSCLK13	17	18	GND
10		19	20	GND

CONN\_20P

NA  
J7

1	RCLK12	1	2	GND
2	TCLK12	3	4	GND
3	RSER12	5	6	GND
4	TSER12	7	8	GPIO12
5	RSYNC12	9	10	RMSG12
6	RCHBLK12	11	12	RSIG12
7	TCHBLK12	13	14	TSIG12
8	RSYCLK12	15	16	GND
9	TSYSCLK12	17	18	GND
10		19	20	GND

CONN\_20P

NA  
J6

1	RCLK11	1	2	GND
2	TCLK11	3	4	GND
3	RSER11	5	6	GND
4	TSER11	7	8	GPIO11
5	RSYNC11	9	10	RMSG11
6	RCHBLK11	11	12	RSIG11
7	TCHBLK11	13	14	TSIG11
8	RSYCLK11	15	16	GND
9	TSYSCLK11	17	18	GND
10		19	20	GND

CONN\_20P

NA  
J5

1	RCLK10	1	2	GND
2	TCLK10	3	4	GND
3	RSER10	5	6	GND
4	TSER10	7	8	GPIO10
5	RSYNC10	9	10	RMSG10
6	RCHBLK10	11	12	RSIG10
7	TCHBLK10	13	14	TSIG10
8	RSYCLK10	15	16	GND
9	TSYSCLK10	17	18	GND
10		19	20	GND

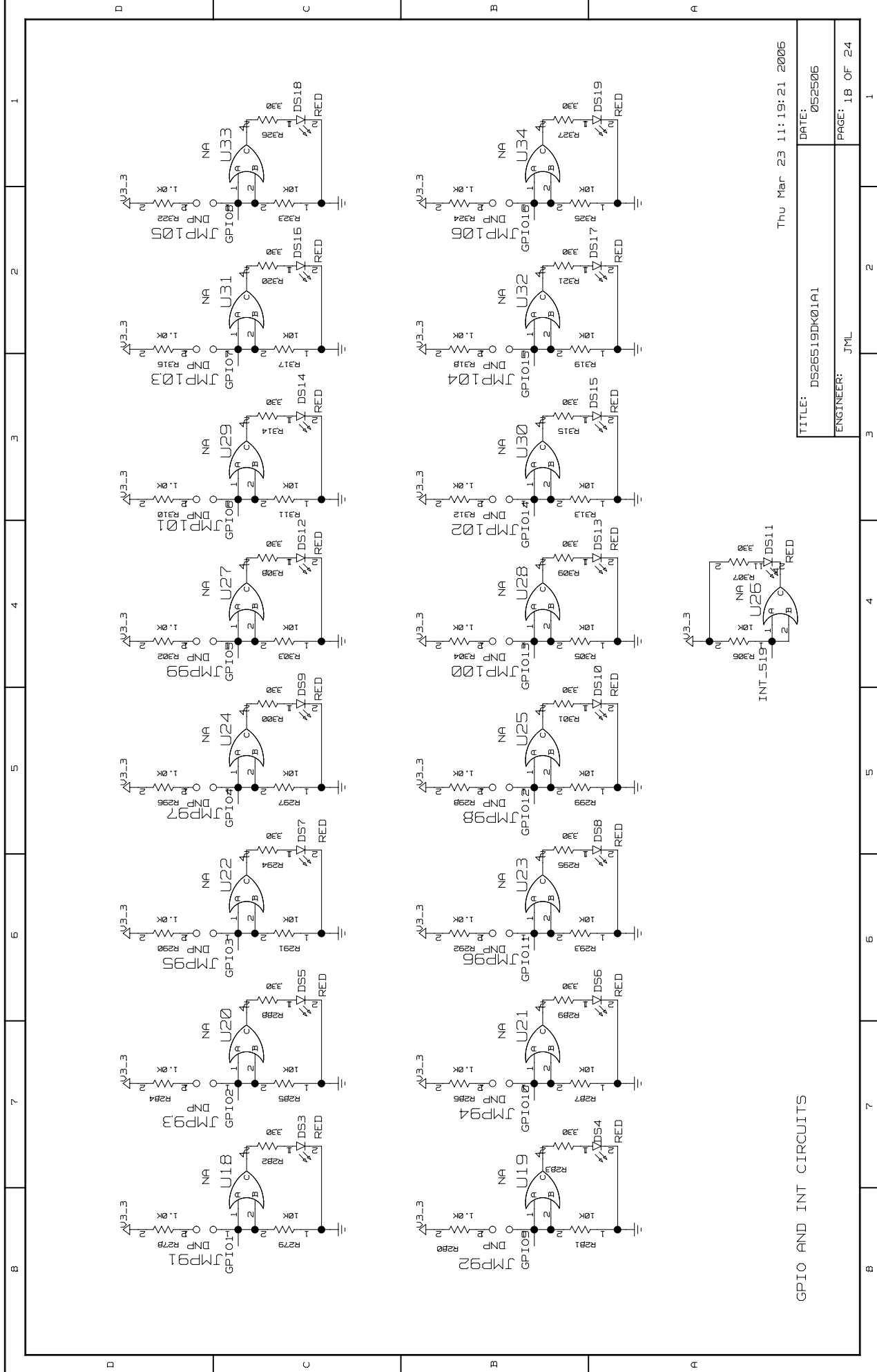
TITLE: DS26519DK01A1

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SYSTEM CONNECTORS



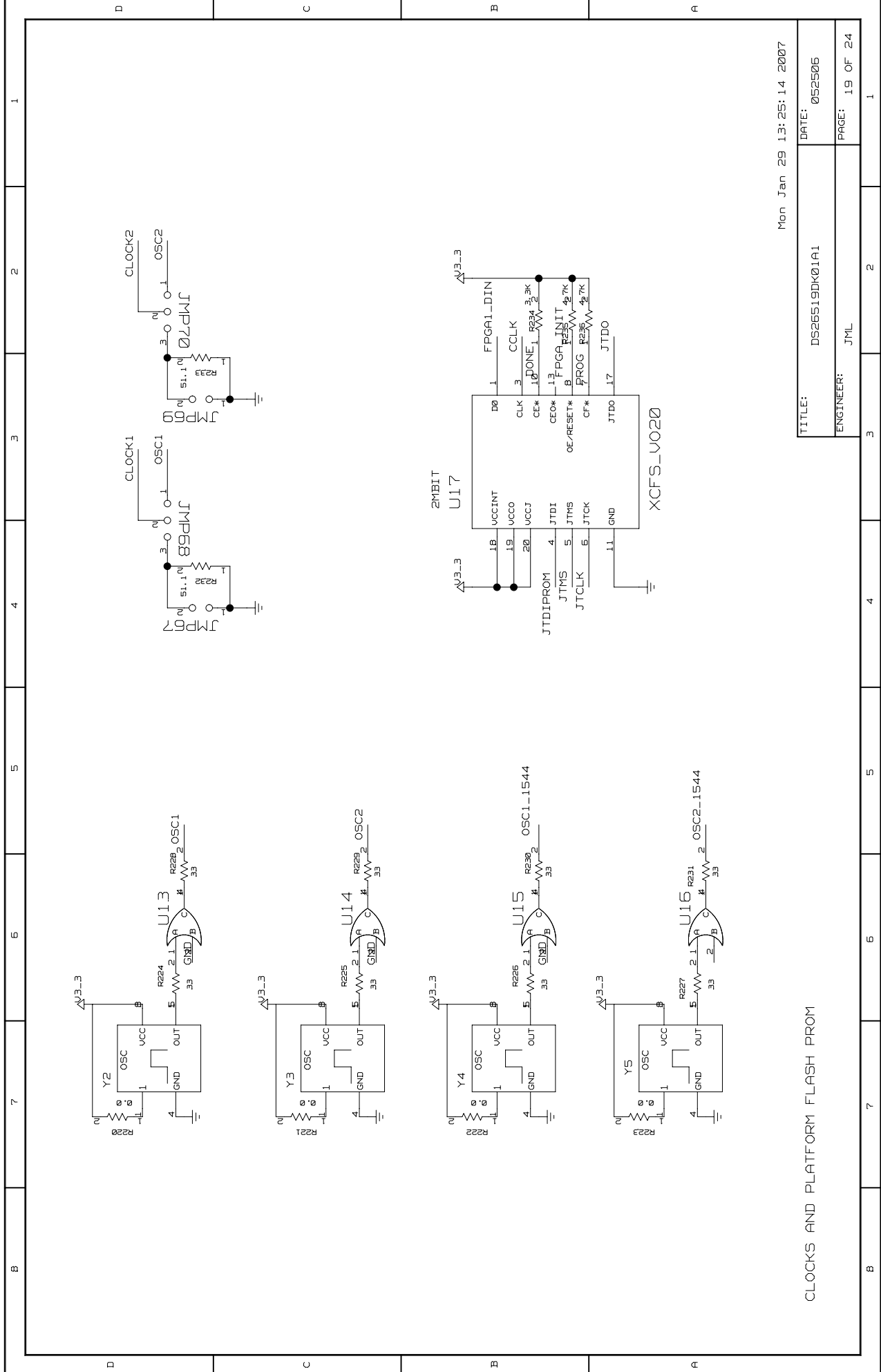
TITLE: DS26519DK01A1  
 ENGINEER: JML

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Thu Mar 23 11:19:21 2006  
 GPIO AND INT CIRCUITS

1 2 3 4 5 6 7 B

1 2 3 4 5 6 7 B

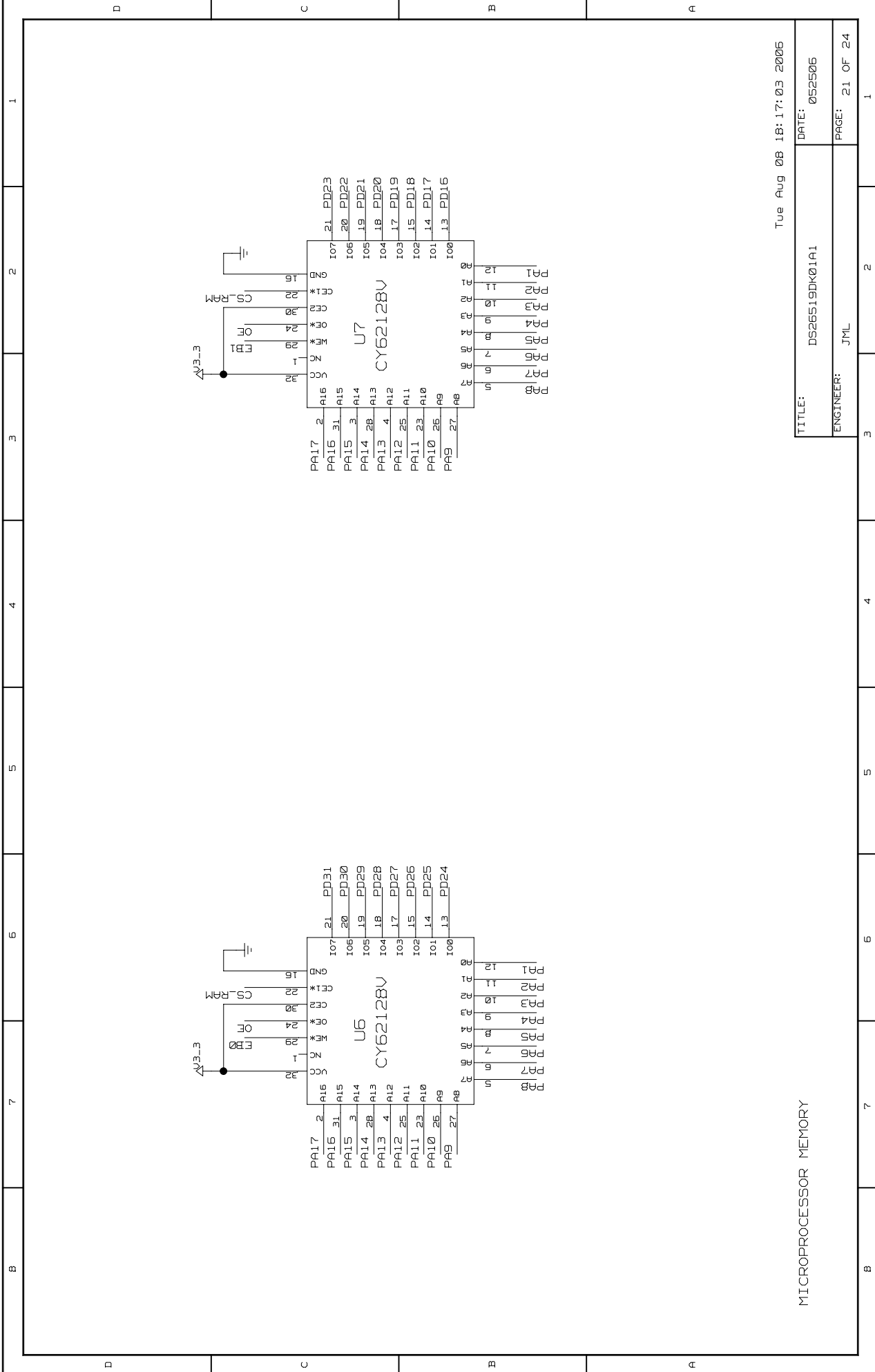


CLOCKS AND PLATFORM FLASH PROM

Mon Jan 29 13:25:14 2007

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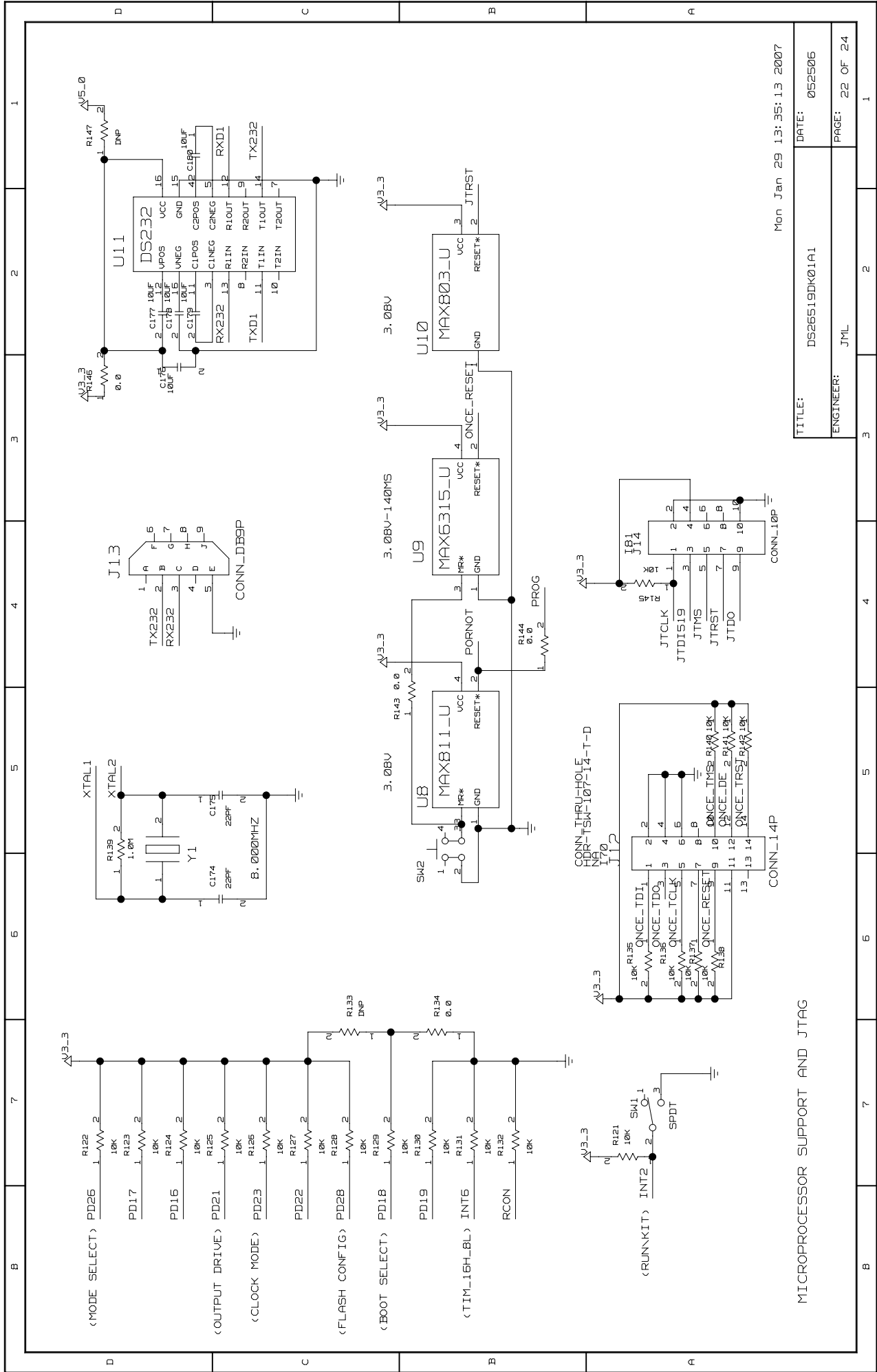




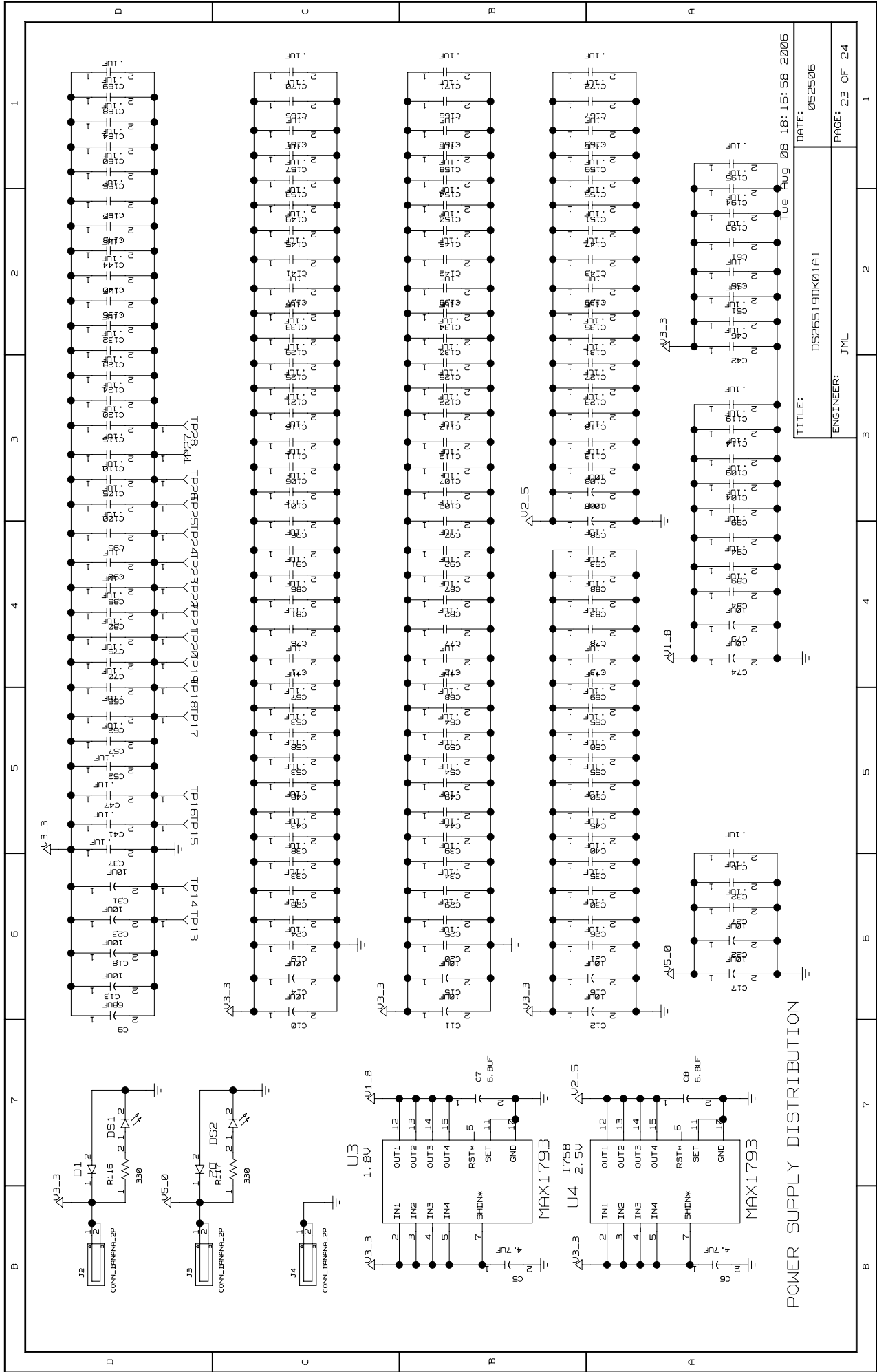
Tue Aug 08 18:17:03 2006

MICROPROCESSOR MEMORY

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POWER SUPPLY DISTRIBUTION

Tue Aug 08 18:16:58 2005

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B	7	6	5	4	3	2	1
D	<p style="text-align: center;">REVISION HISTORY -</p> <p>070506 - 01 - INITIAL RELEASE FOR DESIGN REVIEW</p> <p>080906 - A0 - RELEASE FOR FAB QUOTES</p> <p>012507 - A1 - MODE PINS AND INT PINS FOR FPGA PINOUT ON 8-PORT RJ48 CONNECTORS</p>						A
C							B
B							A
A							D

Mon Jan 29 13:36:19 2007

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