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## FCI7N60

### N-Channel SuperFET® MOSFET 600 V, 7 A, 600 mΩ

#### Features

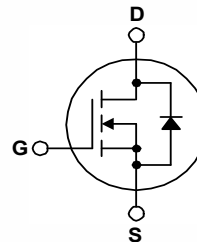
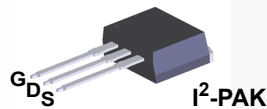
- 650V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 530\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 23\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 60\text{ pF}$ )
- 100% Avalanche Tested
- RoHS compliant

#### Application

- Lighting
- Solar Inverter
- AC-DC Power Supply

#### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



#### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCI7N60	Unit
$V_{DSS}$	Drain to Source Voltage	600	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	7
		- Continuous ( $T_C = 100^\circ\text{C}$ )	4.4
$I_{DM}$	Drain Current	- Pulsed (Note 1)	21
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	230
$I_{AR}$	Avalanche Current	(Note 1)	7
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	8.3
$dv/dt$	Peak Diode Recovery $dv/dt$	(Note 3)	4.5
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	83
		- Derate Above $25^\circ\text{C}$	0.67
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

#### Thermal Characteristics

Symbol	Parameter	FCI7N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FC17N60	FC17N60	I <sup>2</sup> -PAK	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 25^\circ\text{C}$	600	-	-	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_C = 150^\circ\text{C}$	-	650	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.6	-	V/ $^\circ\text{C}$
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 7\text{ A}$	-	700	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	-	-	10	
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	$\pm 100$	nA

### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$	-	0.53	0.6	$\Omega$
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 3.5\text{ A}$	-	6	-	S

### Dynamic Characteristics

C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	710	920	pF
C <sub>oss</sub>	Output Capacitance		-	380	500	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	34	-	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	22	29	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	-	60	-	pF

### Switching Characteristics

t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 7\text{ A}, V_{GS} = 10\text{ V}, R_G = 25\ \Omega$	-	35	80	ns
t <sub>r</sub>	Turn-On Rise Time		-	55	120	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	75	160	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	-	32	75
Q <sub>g(tot)</sub>	Total Gate Charge at 10V	$V_{DS} = 480\text{ V}, I_D = 7\text{ A}, V_{GS} = 10\text{ V}$	-	23	30	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	4.2	5.5	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		(Note 4)	-	11.5	-

### Drain-Source Diode Characteristics

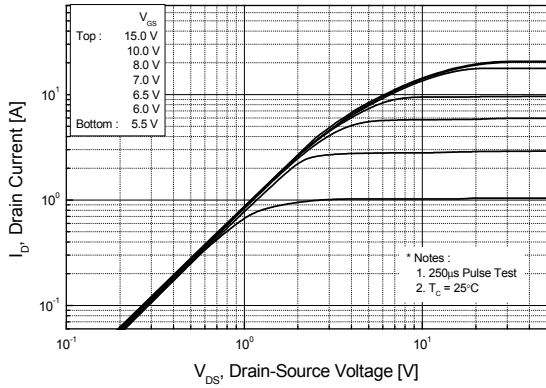
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current	-	-	7	A	
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current	-	-	21	A	
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_{SD} = 7\text{ A}$	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_{SD} = 7\text{ A}, di_F/dt = 100\text{ A}/\mu\text{s}$	-	360	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	4.5	-	$\mu\text{C}$

#### Notes:

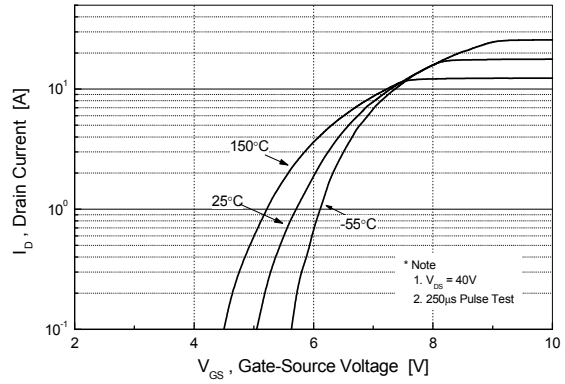
1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 3.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 7\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

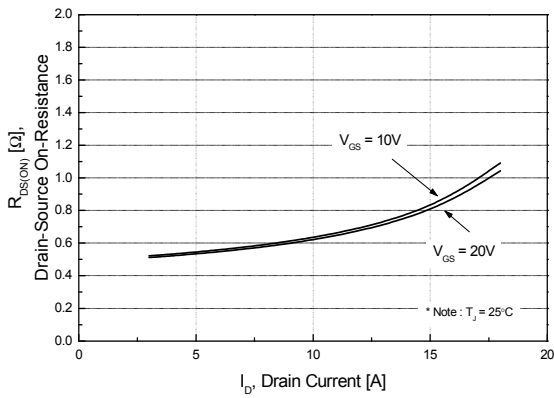
**Figure 1. On-Region Characteristics**



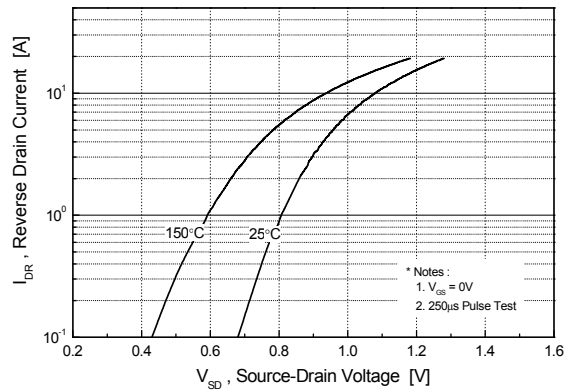
**Figure 2. Transfer Characteristics**



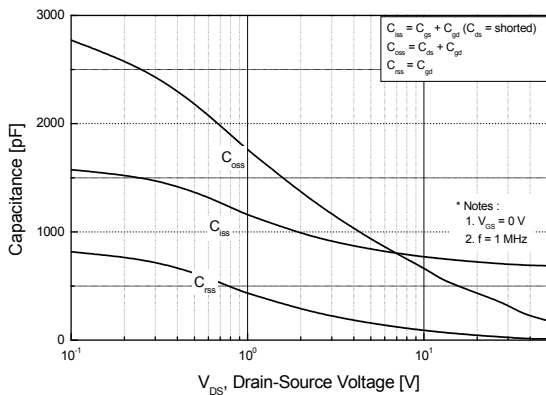
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



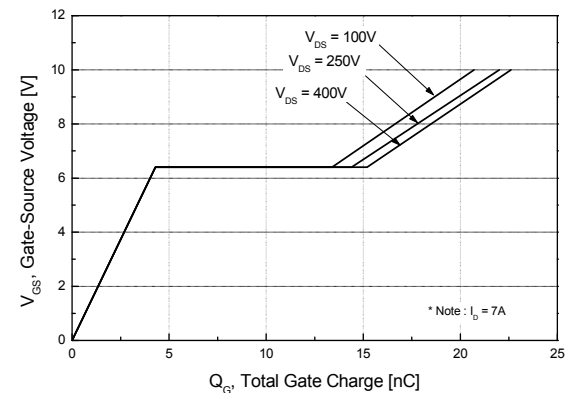
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

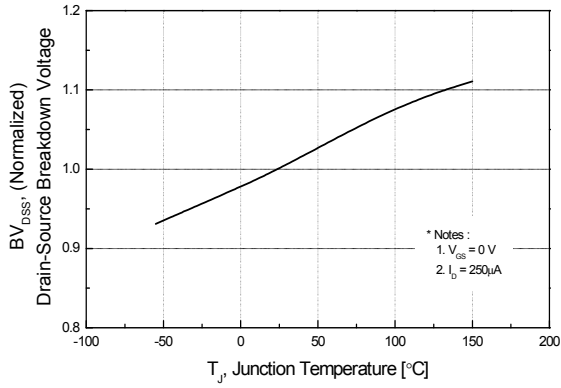


**Figure 6. Gate Charge Characteristics**

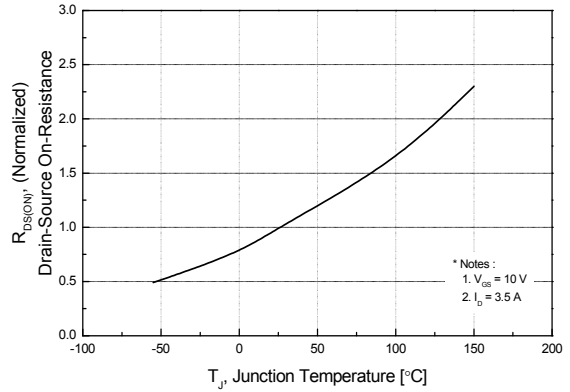


**Typical Performance Characteristics** (Continued)

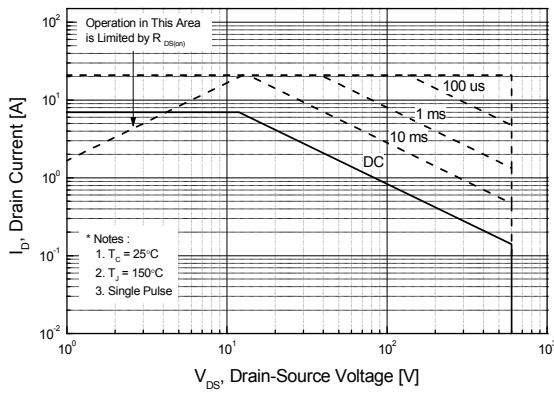
**Figure 7. Breakdown Voltage Variation vs. Temperature**



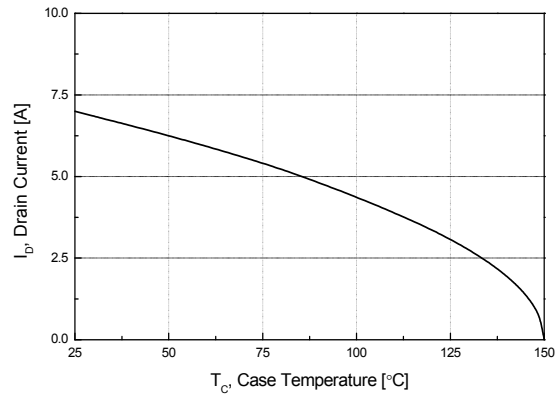
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

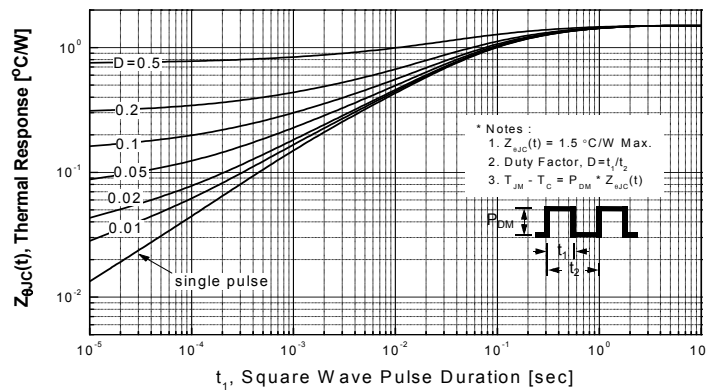




Figure 12. Gate Charge Test Circuit & Waveform

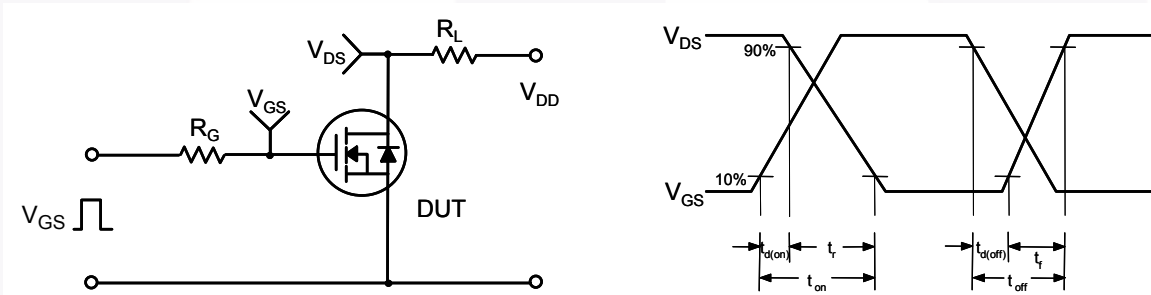


Figure 13. Resistive Switching Test Circuit & Waveforms

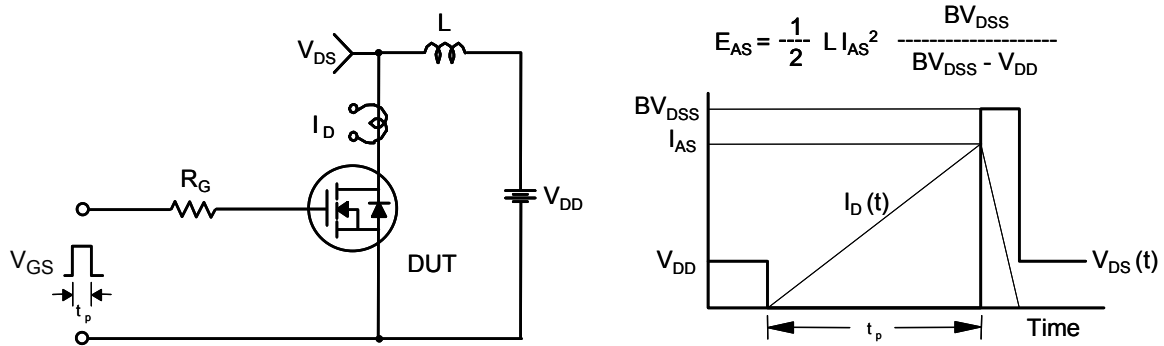
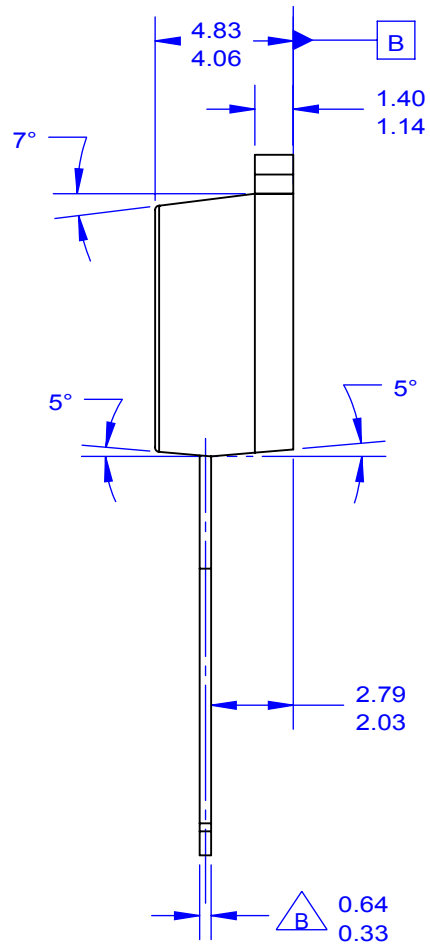
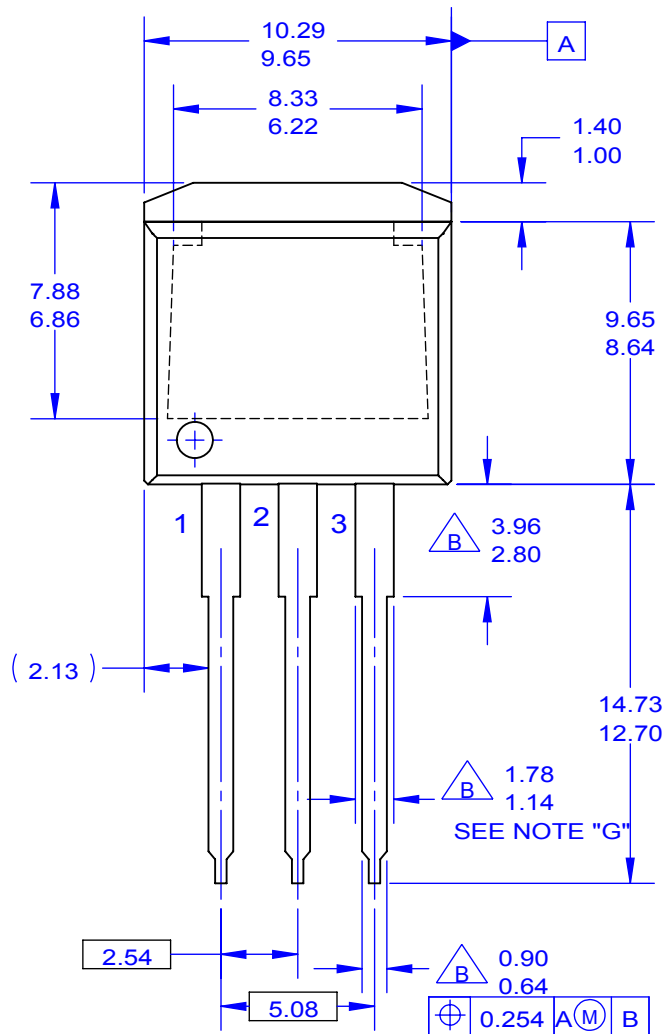


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
- H. DRAWING FILE NAME: TO262A03REV6





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