

Middle Power Class-D Speaker Amplifiers

Class-D Speaker Amplifier for Digital Input



BD5446EFV

No.11075ECT14

●Description

BD5446EFV is a Class D Speaker Amplifier designed for Flat-panel TVs in particular for space-saving and low-power consumption, delivers an output power of 20W+20W. This IC employs state-of-the-art Bipolar, CMOS, and DMOS (BCD) process technology that eliminates turn-on resistance in the output power stage and internal loss due to line resistances up to an ultimate level. With this technology, the IC can achieve high efficiency of 87% (10W+10W output with 8Ω load). In addition, the IC is packaged in a compact reverse heat radiation type power package to achieve low power consumption and low heat generation and eliminates necessity of external heat-sink up to a total output power of 40W. This product satisfies both needs for drastic downsizing, low-profile structures and many function, high quality playback of sound system.

●Features

- 1) BD5446EFV has two system of digital audio interface.
(I²S/LJ format, SDATA: 16 / 20 / 24bit, LRCLK: 32kHz / 44.1kHz / 48kHz, BCLK: 64fs (fixed), SYS_CLK: 256fs (fixed))
- 2) Within the wide range of the power supply voltage, it is possible to operate in a single power supply. (10~26V)
- 3) It contributes to miniaturizing, making to the thin type, and the power saving of the system by high efficiency and low heat.
- 4) S/N of the system can be optimized by adjusting the gain setting among 8 steps. (20~34dB / 2dB step)
- 5) It has the output power limitation function that can be adjusted to an arbitrary output power.
- 6) The decrease in sound quality because of the change of the power supply voltage is prevented with the feedback circuitry of the output. In addition, a low noise and low distortion are achieved.
- 7) It provides with the best stereo DAC output for the headphone usage. As a result, the output of the selection of the digital input in two systems is possible.
- 8) Eliminates pop noise generated when the power supply goes on/off, or when the power supply is suddenly shut off. High quality muting performance is realized by using the soft-muting technology.
- 9) BD5446EFV is a highly reliable design to which it has various protection functions.
(High temperature protection, Under voltage protection, Output short protection, Output DC voltage protection and Clock stop protection)

●Applications

Flat Panel TVs (LCD, Plasma), Home Audio, Desktop PC, Amusement equipments, Electronic Music equipments, etc.,

● Absolute maximum ratings (Ta=25°C)

| Parameter | Symbol | Ratings | Unit | Conditions |
|------------------------------|-------------------|------------|------|------------------------------|
| Supply voltage | V _{CC} | 30 | V | Pin 25, 28, 29, 53, 54 *1 *2 |
| Power dissipation | P _d | 2.0 | W | *3 |
| | | 4.5 | W | *4 |
| | | 6.2 | W | *5 |
| Input voltage | V _{IN} | -0.3 ~ 4.5 | V | Pin 7 ~ 18, 21 *1 |
| Open-drain terminal voltage | V _{ERR} | -0.3 ~ 30 | V | Pin24 *1 |
| Operating temperature range | T _{opr} | -25 ~ +85 | °C | |
| Storage temperature range | T _{stg} | -55 ~ +150 | °C | |
| Maximum junction temperature | T _{jmax} | +150 | °C | |

*1 The voltage that can be applied reference to GND (Pin 6, 36, 37, 45, 46).

*2 Do not, however exceed P_d and T_{jmax}=150°C.

*3 70mm×70mm×1.6mm, FR4, 1-layer glass epoxy board (Copper on bottom layer 0%)

Derating in done at 16mW/°C for operating above Ta=25°C.

*4 70mm×70mm×1.6mm, FR4, 2-layer glass epoxy board (Copper on bottom layer 100%)

Derating in done at 36mW/°C for operating above Ta=25°C. There are thermal via on the board.

*5 70mm×70mm×1.6mm, FR4, 4-layer glass epoxy board (Copper on bottom layer 100%)

Derating in done at 49.6mW/°C for operating above Ta=25°C. There are thermal via on the board.

● Operating conditions (Ta=25°C)

| Parameter | Symbol | Ratings | Unit | Conditions |
|--|-------------------|---------|------|------------------------------|
| Supply voltage | V _{CC} | 10 ~ 26 | V | Pin 25, 28, 29, 53, 54 *1 *2 |
| Minimum load impedance (Speaker Output) | R _{L_SP} | 5.4 | Ω | *6 |
| Minimum load impedance (DAC Output) | R _{L_DA} | 20 | kΩ | Pin 22, 23 |

*6 Do not, however exceed P_d.

* No radiation-proof design.

●Electrical characteristics

(Unless otherwise specified Ta=25°C, Vcc=13V, f=1kHz, RL_SP=8Ω, RL_DA=20kΩ, RESETX=3.3V, MUTEX=3.3V, PDX=3.3V, Gain=20dB, fs=48kHz)

| Item | Symbol | Limits | | | Unit | Conditions |
|---|---------------------|--------|-------|-----|-------|--|
| | | Min | Typ | Max | | |
| Total circuit | | | | | | |
| Circuit current | I _{CC1} | - | 45 | 90 | mA | Pin 25, 28, 29, 53, 54 No load |
| Circuit current (Power down mode) | I _{CC2} | - | 1.5 | 3 | mA | Pin 25, 28, 29, 53, 54, No load RESETX=0V, MUTEX=0V, PDX=0V |
| Open-drain terminal Low level voltage | V _{ERR} | - | - | 0.8 | V | Pin 24, I _o =0.5mA |
| Regulator output voltage 1 | V _{REG_G} | 5.0 | 5.5 | 6.0 | V | Pin 1, 27 |
| Regulator output voltage 2 | V _{REG_3} | 3.0 | 3.3 | 3.6 | V | Pin 5 |
| High level input voltage | V _{IH} | 2.5 | - | 3.3 | V | Pin 7 ~ 18, 21 |
| Low level input voltage | V _{IL} | 0 | - | 0.8 | V | Pin 7 ~ 18, 21 |
| Input current (Input pull-down terminal) | I _{IH} | 33 | 66 | 132 | μA | Pin 7 ~ 18, 21, VIN = 3.3V |
| Speaker Output | | | | | | |
| Maximum momentary output power 1 | P _{O1} | - | 10 | - | W | THD+n=10% GAIN=26dB *7 |
| Maximum momentary output power 2 | P _{O2} | - | 20 | - | W | VCC=18V, THD+n=10% GAIN =26dB *7 |
| Total harmonic distortion | THD _{SP} | - | 0.07 | - | % | P _O =1W, BW=20~20kHz *7 |
| Crosstalk | CT _{SP} | 65 | 80 | - | dB | P _O =1W, BW=IHF-A *7 |
| Output noise voltage (Sampling mode) | V _{NO_SP} | - | 140 | 280 | μVrms | -∞dBFS, BW=IHF-A *7 |
| Residual noise voltage (Mute mode) | V _{NOR_SP} | - | 5 | 10 | μVrms | MUTEX=0V, -∞dBFS, BW=IHF-A *7 |
| PWM sampling frequency | f _{PWM1} | - | 512 | - | KHz | fs=32kHz *7 |
| | f _{PWM2} | - | 705.6 | - | KHz | fs=44.1kHz *7 |
| | f _{PWM3} | - | 768 | - | KHz | fs=48kHz *7 |
| DAC Output | | | | | | |
| Maximum output voltage | V _{OMAX} | 0.85 | 1.0 | - | Vrms | 0dBFS, THD+n=1% |
| Channel Balance | CB | -1 | 0 | 1 | dB | 0dBFS |
| Total harmonic distortion | THD _{DA} | - | 0.05 | 0.5 | % | -20dBFS, BW=20~20kHz |
| Crosstalk | CT _{DA} | 65 | 80 | - | dB | 0dBFS, BW=IHF-A |
| Output noise voltage | V _{NO_DA} | - | 10 | 20 | μVrms | -∞dBFS, BW=IHF-A |
| Residual noise voltage | V _{NOR_DA} | - | 3 | 10 | μVrms | MUTEX=0V, PDX=0V, -∞dBFS, BW=IHF-A |

*7 These items show the typical performance of device and depend on board layout, parts, and power supply.
The standard value is in mounting device and parts on surface of ROHM's board directly.

● **Electrical characteristic curves** ($V_{CC}=13V, T_a=25^\circ C, R_{L_SP}=8\Omega, R_{L_DA}=20k\Omega, Gain=20dB, f_{in}=1kHz, f_s=48kHz$)
 Measured by ROHM designed 4 layer board.

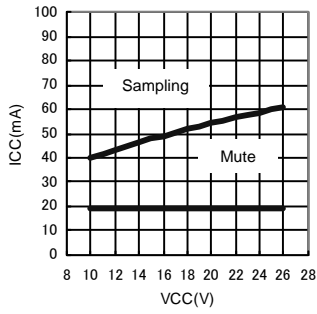


Fig.1

Current consumption
 - Power supply voltage

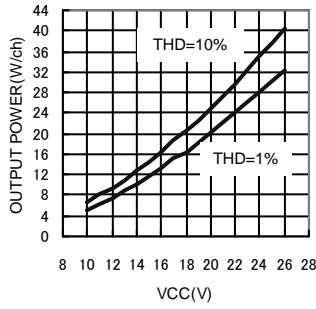


Fig.2

Output power
 - Power supply voltage

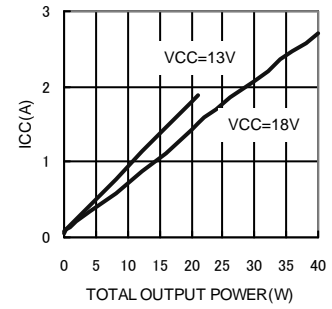


Fig.3

Current consumption
 - Output power

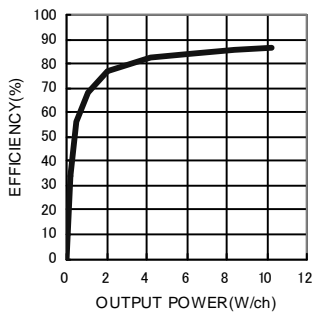


Fig.4

Efficiency - Output power

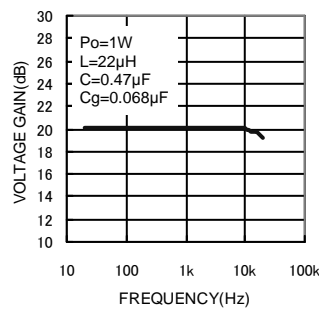


Fig.5

Voltage gain - Frequency

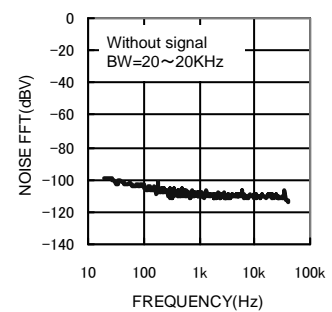


Fig.6

FFT of Output noise voltage

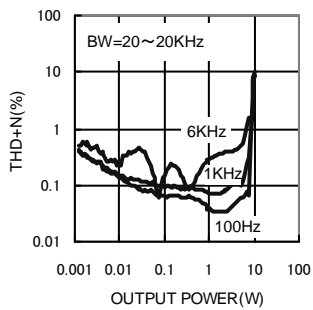


Fig.7

THD+N - Output power

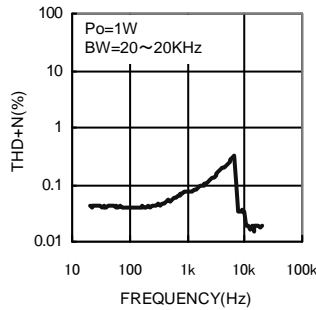


Fig.8

THD+N - Frequency

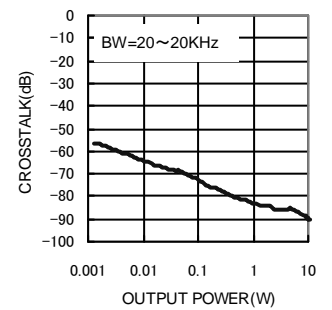


Fig.9

Crosstalk - Output power

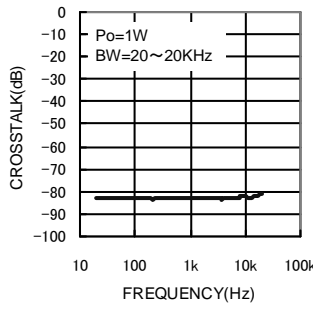


Fig.10

Crosstalk - Frequency

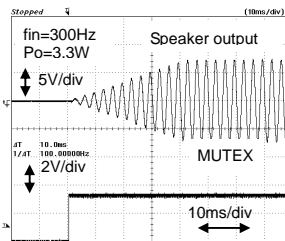


Fig.11

Wave form when
 Releasing Soft-mute

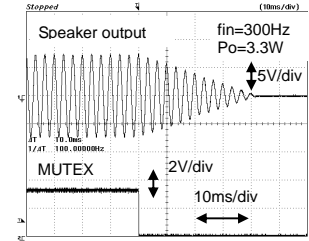


Fig.12

Wave form when
 Activating Soft-mute

●Electrical characteristic curves($V_{CC}=18V, T_a=25^{\circ}C, R_{L_SP}=8\Omega, R_{L_DA}=20k\Omega, Gain=20dB, f_{in}=1kHz, f_s=48kHz$)

Measured by ROHM designed 4layer board.

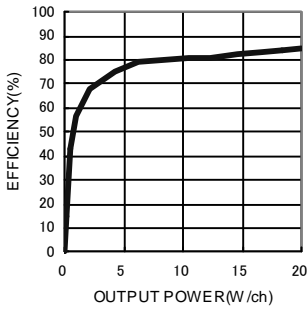


Fig.13

Efficiency – Output power

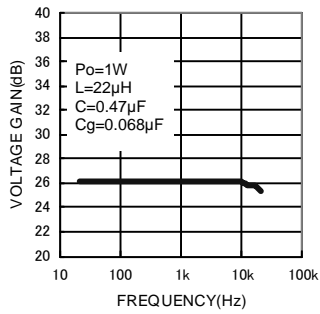


Fig.14

Voltage gain - Frequency

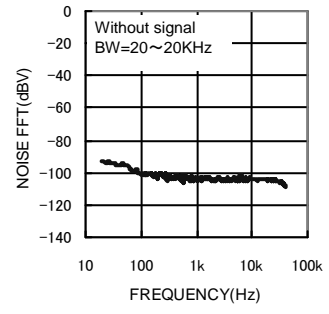


Fig.15

FFT of output noise voltage

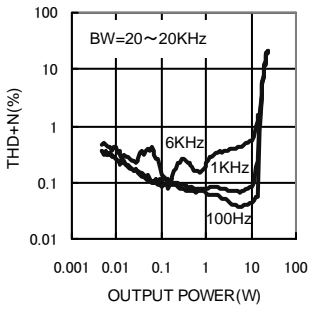


Fig.16

THD+N - Output power

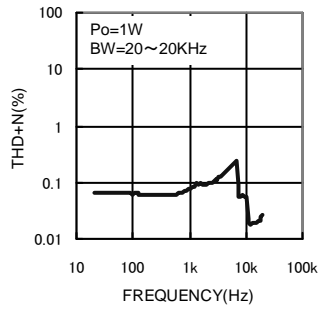


Fig.17

THD+N - Frequency

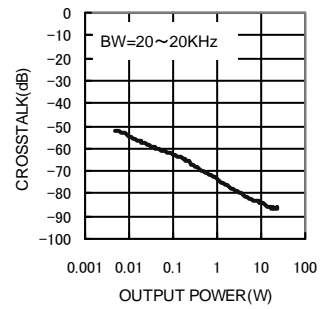


Fig.18

Crosstalk - Output power

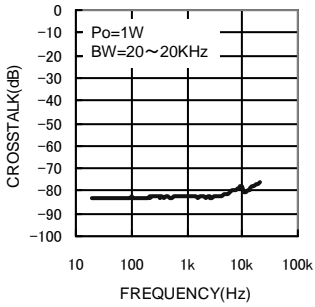
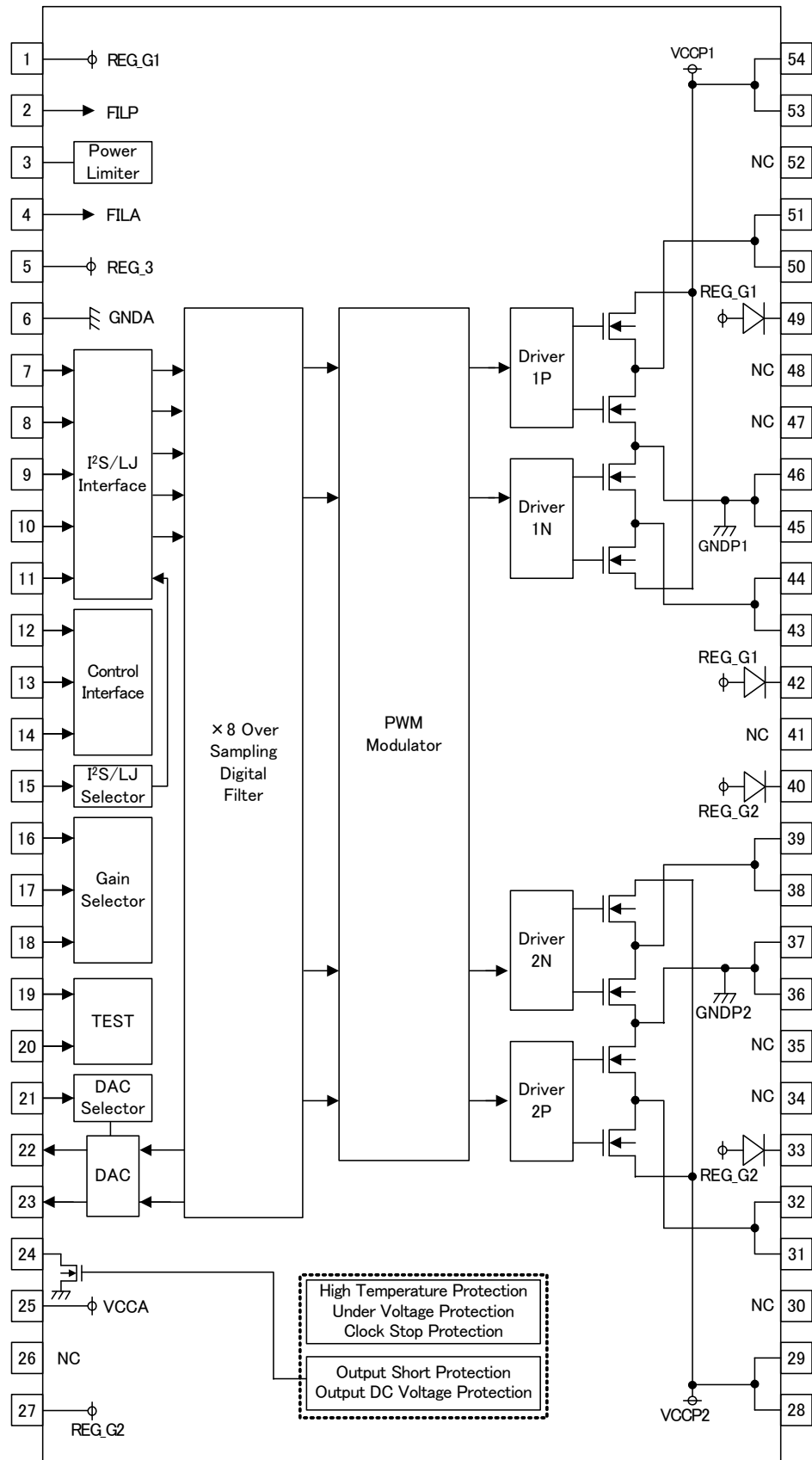


Fig.19

Crosstalk - Frequency

● Pin configuration and Block diagram



●Pin function explanation (Provided pin voltages are typ. Values)

| No. | Pin name | Pin voltage | Pin explanation | Internal equivalence circuit |
|---------|------------------|-------------|---|------------------------------|
| 1 27 | REG_G1 REG_G2 | 5.5V | Internal power supply pin for ch1 Gate driver Internal power supply pin for ch2 Gate driver Please connect the capacitor. | |
| 2 | FILP | 1.75V~2.55V | Bias pin for PWM signal Please connect the capacitor. | |
| 3 | PLMT | 0V | Power limiter setting terminal | |
| 4 | FILA | 2.5V | Bias pin for Analog signal Please connect the capacitor. | |
| 5 | REG3 | 3.3V | Internal power supply pin for Digital circuit Please connect the capacitor. | |
| 6 | GNDA | 0V | GND pin for Analog signal | — |

| No. | Pin name | Pin voltage | Pin explanation | Internal equivalence circuit |
|-------------------------|--|-------------|---|------------------------------|
| 7 8 9 10 11 | SYS_CLK BCLK LRCLK SDATA1 SDATA2 | 0V | Digital audio signal input pin | |
| 12 | RESETX | 0V | Reset pin for Digital circuit H: Reset OFF L: Reset ON | |
| 13 | MUTEX | | Speaker output mute control pin H: Mute OFF L: Mute ON | |
| 14 | PDX | | Power down control pin H: Power down OFF L: Power down ON | |
| 15 | IIS_LJ | 0V | Digital audio signal data format setting terminal H: Left Justified format L: I ² S format | |
| 16 17 18 | GAIN1 GAIN2 GAIN3 | 0V | Gain setting terminal Gain=20dB~34dB, 2dB step | |
| 19 20 | TEST1 TEST2 | 0V | Test pin Please connect to GND. | |
| 21 | SEL_DAC | 0V | DAC output selection terminal H: SDATA2 is output from the DAC L: SDATA1 is output from the DAC | |

| No. | Pin name | Pin voltage | Pin explanation | Internal equivalence circuit |
|----------------------------------|----------------------|-------------|---|------------------------------|
| 22 23 | OUT_DAC2 OUT_DAC1 | 2.5V | ch2 DAC output pin ch1 DAC output pin Please connect it with the latter part circuit through the capacitor. | |
| 24 | ERROR | 3.3V | Error flag pin Please connect pull-up resistor. H: While Normal L: While Error | |
| 25 | VCCA | VCC | Power supply pin for Analog signal | — |
| 26,30 34,35 41,47 48,52 | N.C. | — | Non connection pin | — |

| No. | Pin name | Pin voltage | Pin explanation | Internal equivalence circuit |
|-------|----------|-------------|---|------------------------------|
| 28,29 | VCCP2 | Vcc | Power supply pin for ch2 PWM signal | |
| 31,32 | OUT2P | Vcc~0V | Output pin of ch2 positive PWM Please connect to Output LPF. | |
| 33 | BSP2P | — | Boot-strap pin of ch2 positive Please connect the capacitor. | |
| 36,37 | GNDP2 | 0V | GND pin for ch2 PWM signal | |
| 38,39 | OUT2N | Vcc~0V | Output pin of ch2 negative PWM Please connect to Output LPF. | |
| 40 | BSP2N | — | Boot-strap pin of ch2 negative Please connect the capacitor. | |
| 42 | BSP1N | — | Boot-strap pin of ch1 negative Please connect the capacitor. | |
| 43,44 | OUT1N | Vcc~0V | Output pin of ch1 negative PWM Please connect to Output LPF. | |
| 45,46 | GNDP1 | 0V | GND pin for ch1 PWM signal | |
| 49 | BSP1P | — | Boot-strap pin of ch1 positive Please connect the capacitor. | |
| 50,51 | OUT1P | Vcc~0V | Output pin of ch1 positive PWM Please connect to Output LPF. | |
| 53,54 | VCCP1 | — | Power supply pin for ch1 PWM signal | |

●GAIN1 pin, GAIN2 pin, GAIN3 pin function

| GAIN3 (18pin) | GAIN2 (17pin) | GAIN1 (16pin) | Speaker output gain |
|------------------|------------------|------------------|---------------------|
| L | L | L | 20dB |
| L | L | H | 22dB |
| L | H | L | 24dB |
| L | H | H | 26dB |
| H | L | L | 28dB |
| H | L | H | 30dB |
| H | H | L | 32dB |
| H | H | H | 34dB |

●SEL_DAC pin function

| SEL_DAC (21pin) | OUT_DAC1 (23pin) | OUT_DAC2 (24pin) |
|--------------------|------------------------------------|------------------------------------|
| L | The Lch signal of SDATA1 is output | The Rch signal of SDATA1 is output |
| H | The Lch signal of SDATA2 is output | The Rch signal of SDATA2 is output |

●RESETX pin function

| RESETX (10pin) | State of Digital block |
|-------------------|------------------------|
| L | Reset ON |
| H | Reset OFF |

●RESETX pin

| RESETX (12pin) | State of Digital block |
|-------------------|------------------------|
| L | Reset ON |
| H | Reset OFF |

●PDX pin,MUTEX pin function

| PDX (12pin) | MUTEX (11pin) | Power Down | DAC output (24,25pin) | PWM output (33,34,38,39,43,44,48pin) |
|----------------|------------------|------------|--------------------------|---|
| L | L or H | ON | HiZ_Low | HiZ_Low |
| H | L | OFF | Normal operation | |
| H | H | | | Normal operation |

●IIS_LJ pin function

| IIS_LJ (15pin) | Digital data format |
|-------------------|---------------------|
| L | I2S |
| H | Left Justified |

● **Input digital audio signal sampling frequency (fs) explanation**

PWM sampling frequency, Soft-start, Soft-mute time, and the detection time of the DC voltage protection in the speaker depends on sampling frequency (fs) of the digital audio input.

| Sampling frequency of the digital audio input (fs) | PWM sampling frequency (fpwm) | Soft-start / Soft-mute time | DC voltage protection in the speaker detection time |
|--|-------------------------------|-----------------------------|---|
| 32kHz | 512kHz | 64msec. | 64msec. |
| 44.1kHz | 705.6kHz | 46msec. | 46msec. |
| 48kHz | 768kHz | 43msec. | 43msec. |

● **For voltage gain (Gain setting)**

BD5446EFV prescribe voltage gain at speaker output (BTL output) under the definition 0dBV (1Vrms) as full scale input of the digital audio input signal. For example, digital audio input signal = Full scale input, Gain setting = 20dB, Load resistance $R_{L_SP} = 8\Omega$ will give speaker output (BTL output) amplitude as $V_o=10V_{rms}$. (Output power $P_o = V_o^2/R_{L_SP} = 12.5W$)

● **Speaker output and DAC output**

Digital audio input signal SDATA1 will be output to the speaker. (SDATA2 will not be output to the speaker. DAC output can be selected either from digital audio input signal SDATA1 or SDATA2.)

● **Format of digital audio input**

- **SYS_CLK:** It is System Clock input signal.
It will input LRCLK, BCLK, SDATA1 (SDATA2) that synchronizes with this clock that are 256 times of sampling frequency (256fs).
- **LRCLK:** It is L/R clock input signal.
It corresponds to 32kHz/44.1kHz/48kHz with those clock (fs) that are same to the sampling frequency (fs) .
The data of a left channel and a right channel for one sample is input to this section.
- **BCLK:** It is Bit Clock input signal.
It is used for the latch of data in every one bit by sampling frequency's 64 times sampling frequency (64fs).
- **SDATA1 & SDATA2:** It is Data input signal.
It is amplitude data. The data length is different according to the resolution of the input digital audio data.
It corresponds to 16/ 20/ 24 bit.

● I²S data format

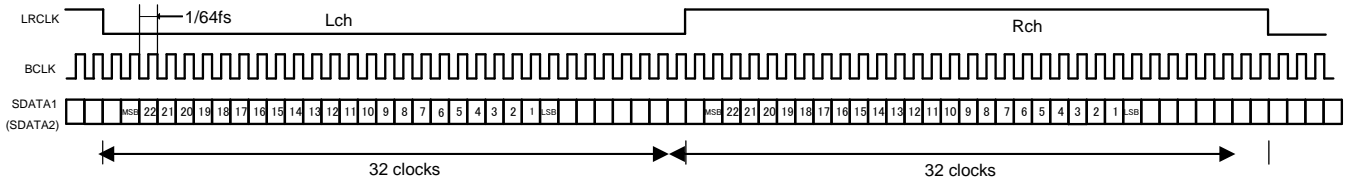


Fig.20 I²S Data Format 64fs, 24 bit Data

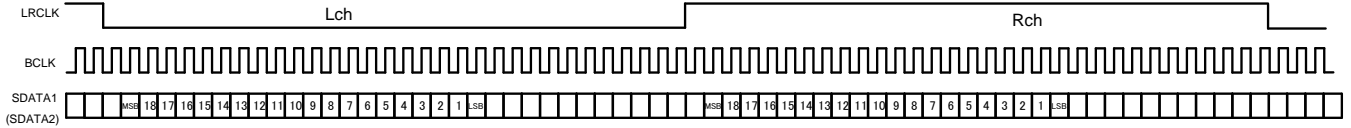


Fig.21 I²S Data Format 64fs, 20 bit Data

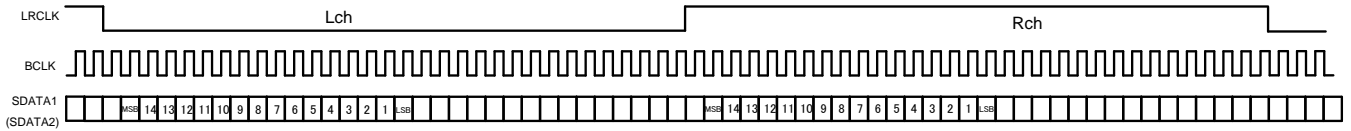


Fig.22 I²S Data Format 64fs, 16 bit Data

The Low section of LRCLK becomes Lch, the High section of LRCLK becomes Rch.
After changing LRCLK, second bit becomes MSB.

● Left-justified format

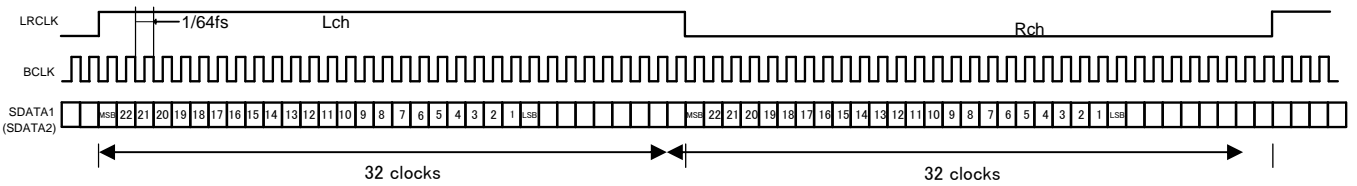


Fig.23 Left-Justified Data Format 64fs, 24 bit Data

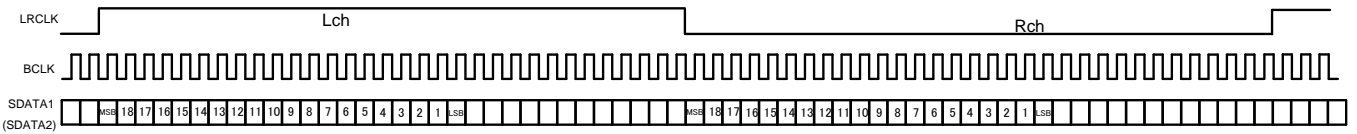


Fig.24 Left-Justified Data Format 64fs, 20 bit Data

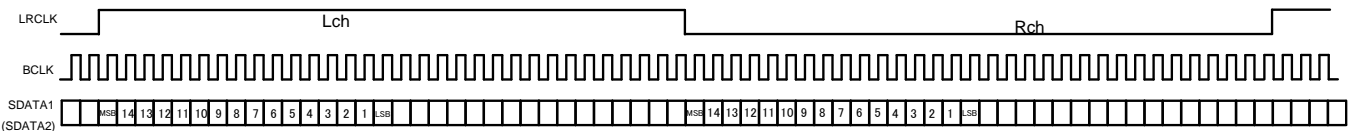


Fig.25 Left-Justified Data Format 64fs, 16 bit Data

The High section of LRCLK becomes Lch, the Low section of LRCLK becomes Rch.
After changing LRCLK, first bit becomes MSB.

●Audio Interface format and timing

Recommended timing and operating conditions (MCLK, BCLK, LRCLK, SDATA)

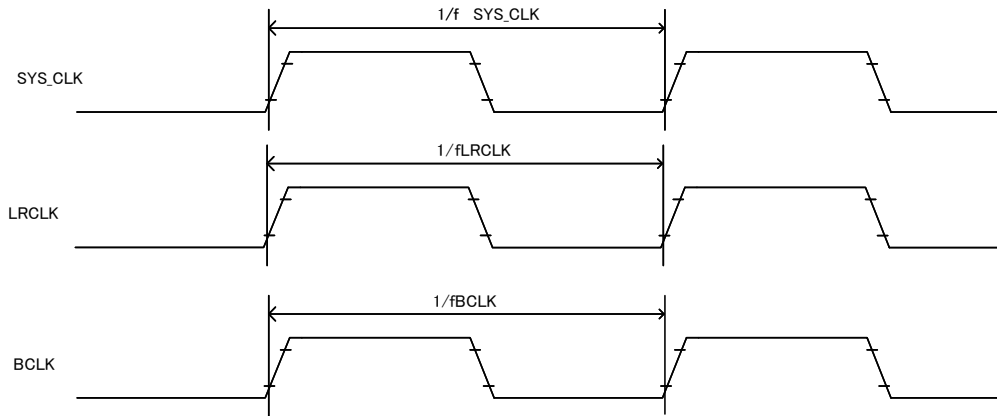


Fig-26 Clock timing

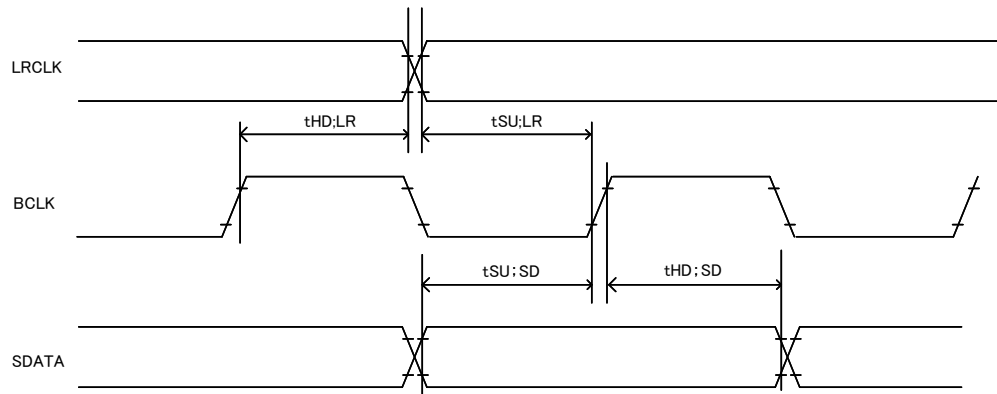


Fig-27 Audio Interface timing (1)

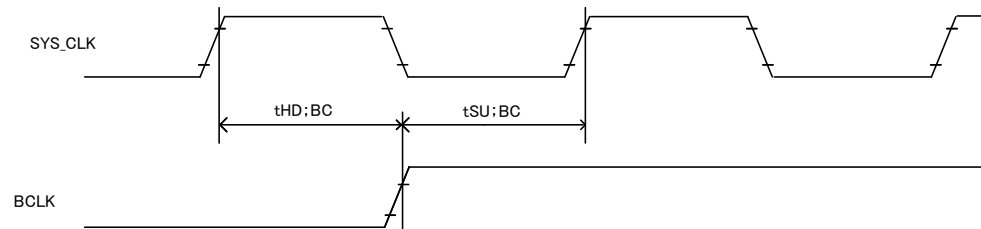


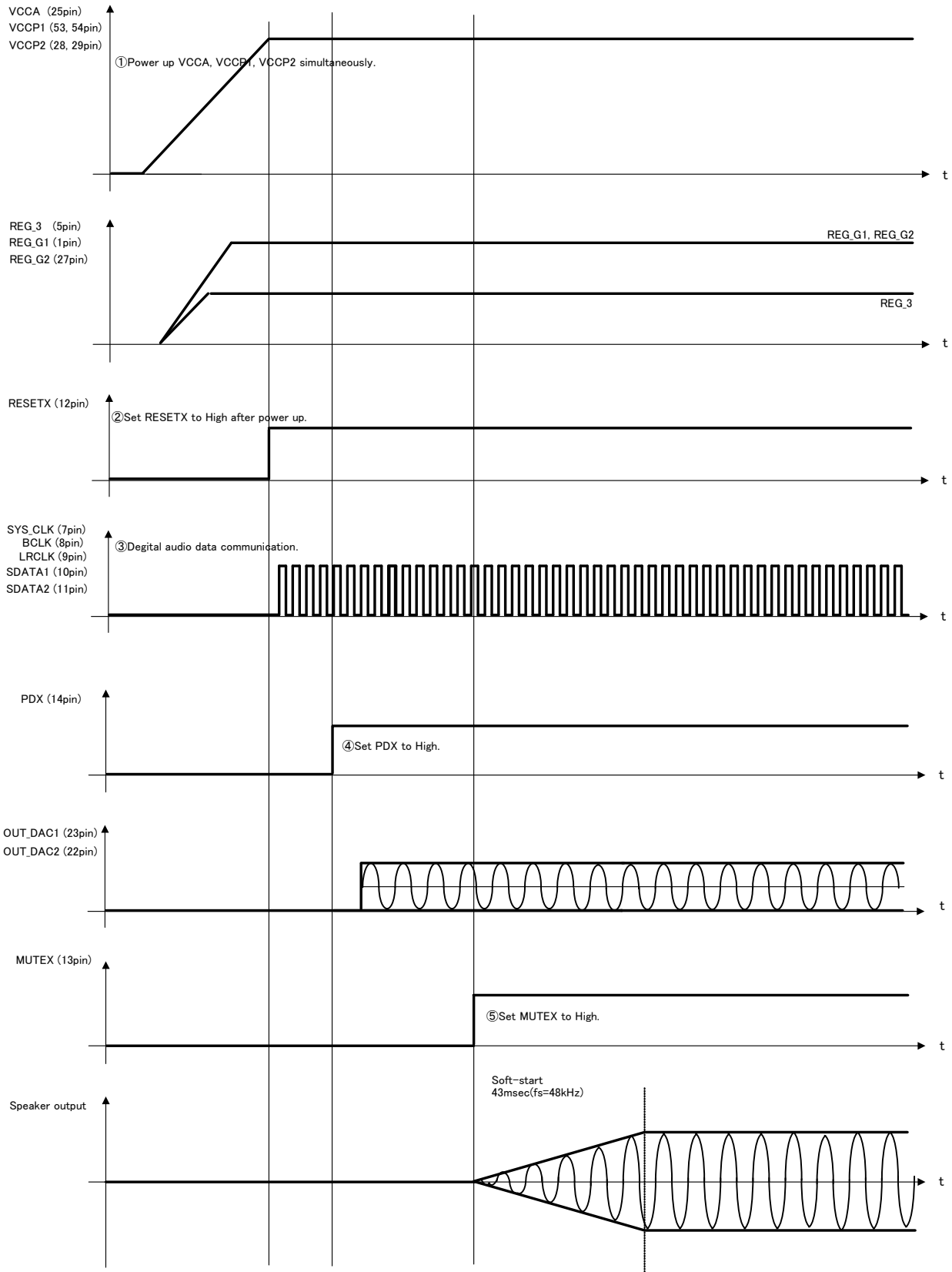
Fig-28 Audio Interface timing (2)

| Parameter | | Symbol | Limit | | Unit |
|-----------|---------------------|----------|-------|--------|------|
| | | | Min. | Max. | |
| 1 | SYS_CLK frequency | fSYS_CLK | 8.192 | 12.288 | MHz |
| 2 | LRCLK frequency | fLRCLK | 32 | 48 | kHz |
| 3 | BCLK frequency | fBCLK | 2.048 | 3.072 | MHz |
| 4 | Setup time, LRCLK※1 | tSU;LR | 20 | — | ns |
| 5 | Hold time, LRCLK※1 | tHD;LR | 20 | — | ns |
| 6 | Setup time, SDATA | tSU;SD | 20 | — | ns |
| 7 | Hold time, SDATA | tHD;SD | 20 | — | ns |
| 8 | Setup time, BCLK※2 | tSU;BC | 2.5 | — | ns |
| 9 | Hold time, BCLK※2 | tHD;BC | 3.5 | — | ns |

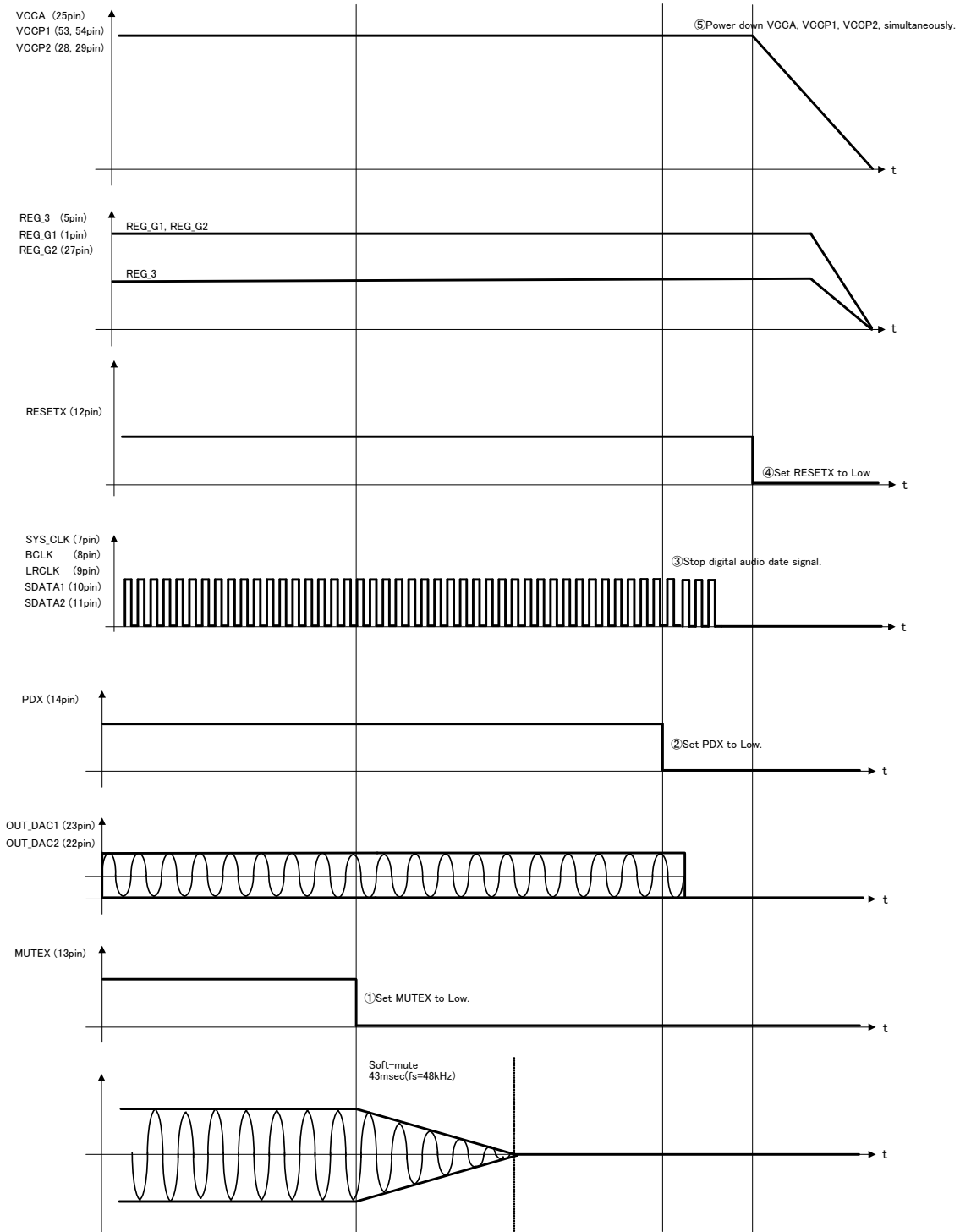
※1 This regulation is to keep rising edge of LRCK and rising edge of BCLK from overlapping.

※2 This regulation is to keep rising edge of SYS_CLK and rising edge of BCLK from overlapping.

● Power supply start-up sequence



● Power supply shut-down sequence



●About the protection function

| Protection function | Detecting & Releasing condition | | DAC Output | PWM Output | ERROR Output |
|--------------------------------------|---------------------------------|---|------------------|------------------|--------------|
| Output short protection | Detecting condition | Detecting current = 10A (TYP.) | Normal operation | HiZ_Low (Latch) | L (Latch) |
| DC voltage protection in the speaker | Detecting condition | PWM output Duty=0% or 100% 43msec(fs=48kHz) above fixed | | HiZ_Low (Latch) | L (Latch) |
| High temperature protection | Detecting condition | Chip temperature to be above 150°C (TYP.) | Normal operation | HiZ_Low | H |
| | Releasing condition | Chip temperature to be below 120°C (TYP.) | | Normal operation | |
| Under voltage protection | Detecting condition | Power supply voltage to be below 8V (TYP.) | Normal operation | HiZ_Low | H |
| | Releasing condition | Power supply voltage to be above 9V (TYP.) | | Normal operation | |
| Clock stop protection | Detecting condition | No change to SYS_CLK more than 1usec (TYP.) | Irregular output | HiZ_Low | H |
| | Releasing condition | Normal input to SYS_CLK | Normal operation | Normal operation | |

* The ERROR pin is Nch open-drain output.

* Once an IC is latched, the circuit is not released automatically even after an abnormal status is removed.

The following procedures ① or ② is available for recovery.

①After the MUTEX pin is made Low once, the MUTEX pin is returned to High again.

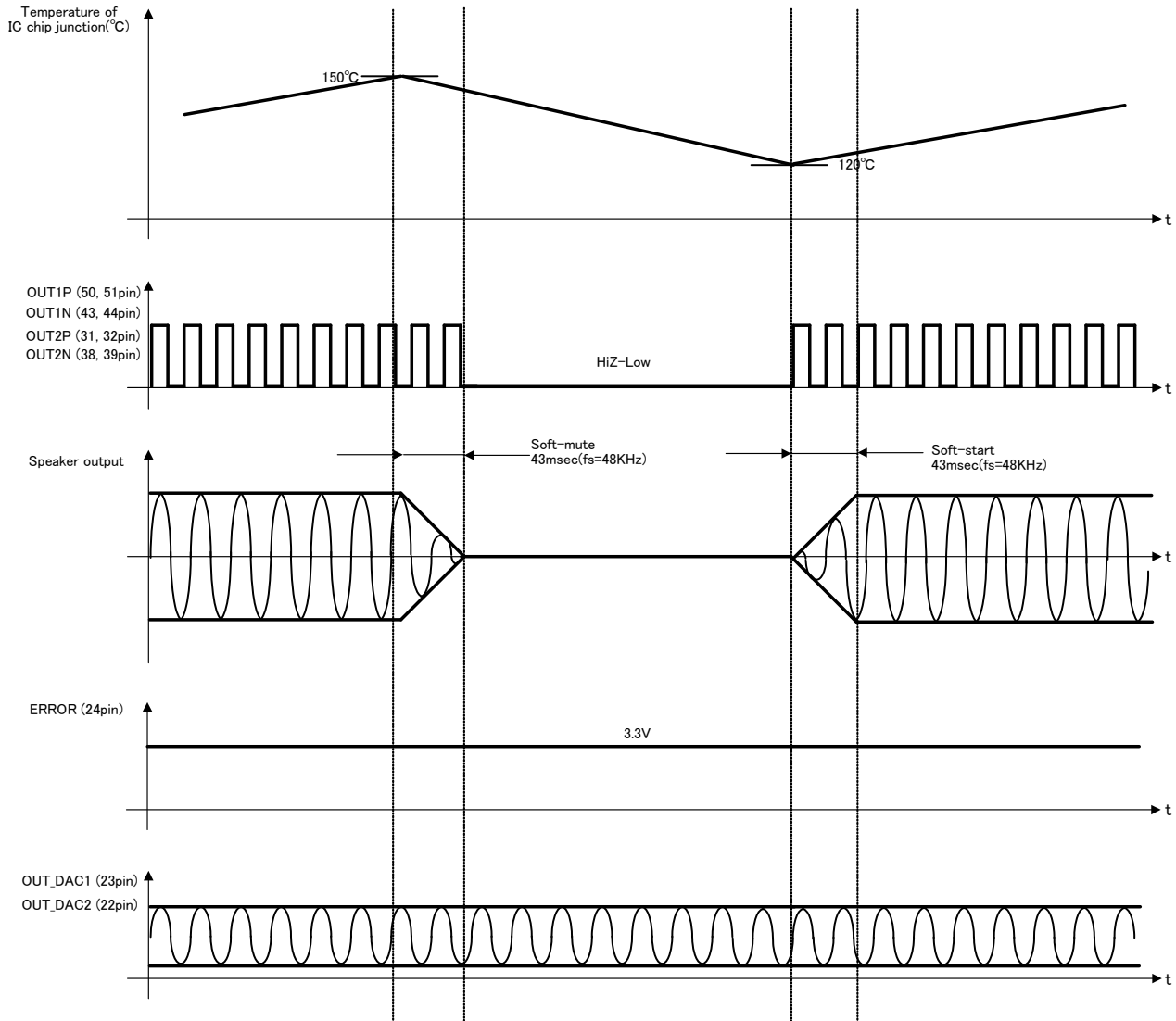
②Turning on the power supply again.

1) High temperature protection

This IC has the high temperature protection circuit that prevents thermal reckless driving under an abnormal state for the temperature of the chip to exceed $T_{jmax}=150^{\circ}\text{C}$.

Detecting condition - It will detect when MUTE pin is set High and the temperature of the chip becomes 150°C (TYP.) or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the temperature of the chip becomes 120°C (TYP.) or less. The speaker output is outputted through a soft-start when released.

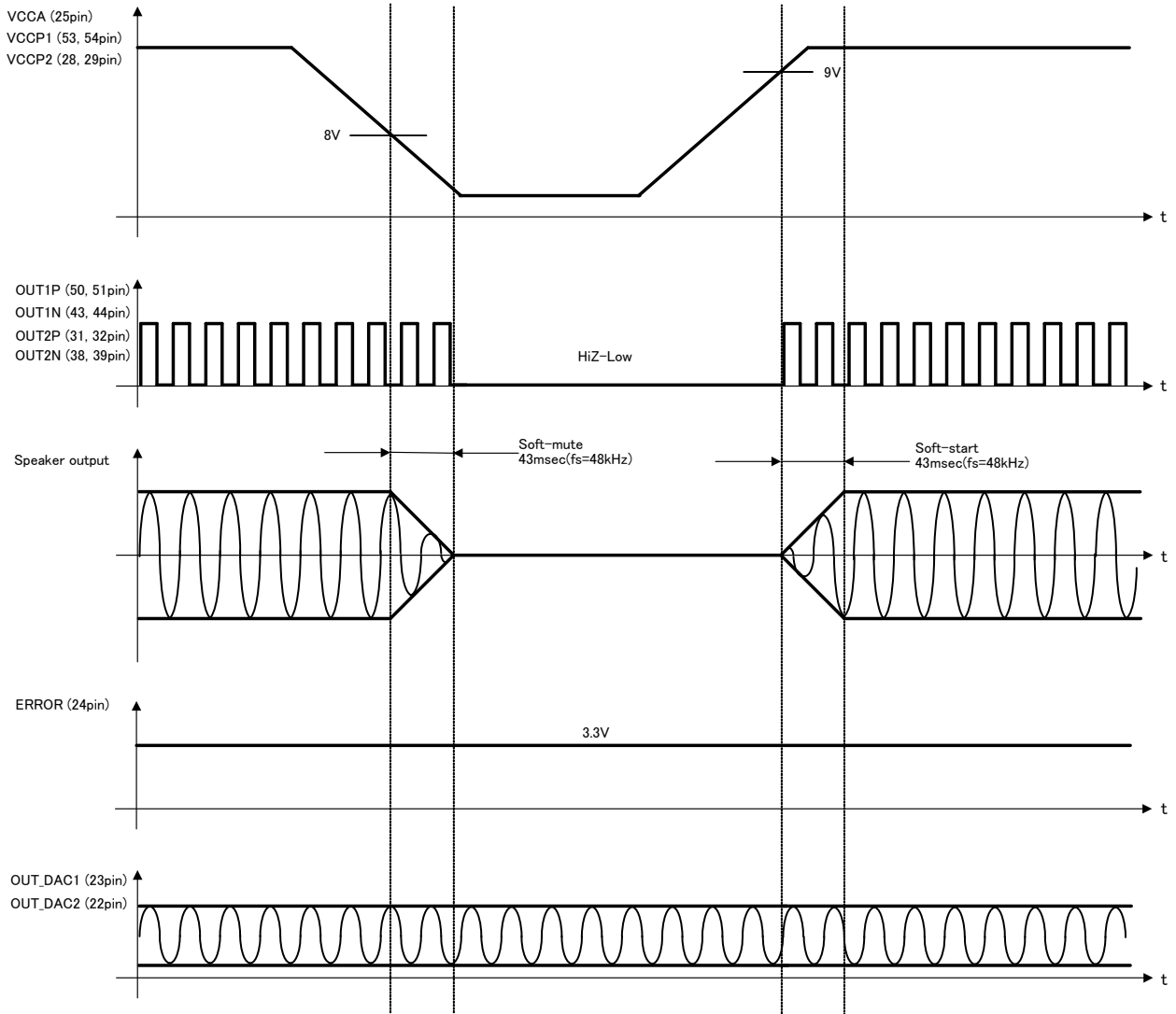


2) Under voltage protection

This IC has the under voltage protection circuit that make speaker output mute once detecting extreme drop of the power supply voltage.

Detecting condition – It will detect when MUTE pin is set High and the power supply voltage becomes lower than 8V.
The speaker output is muted through a soft-mute when detected.

Releasing condition – It will release when MUTE pin is set High and the power supply voltage becomes more than 9V.
The speaker output is outputted through a soft-start when released.

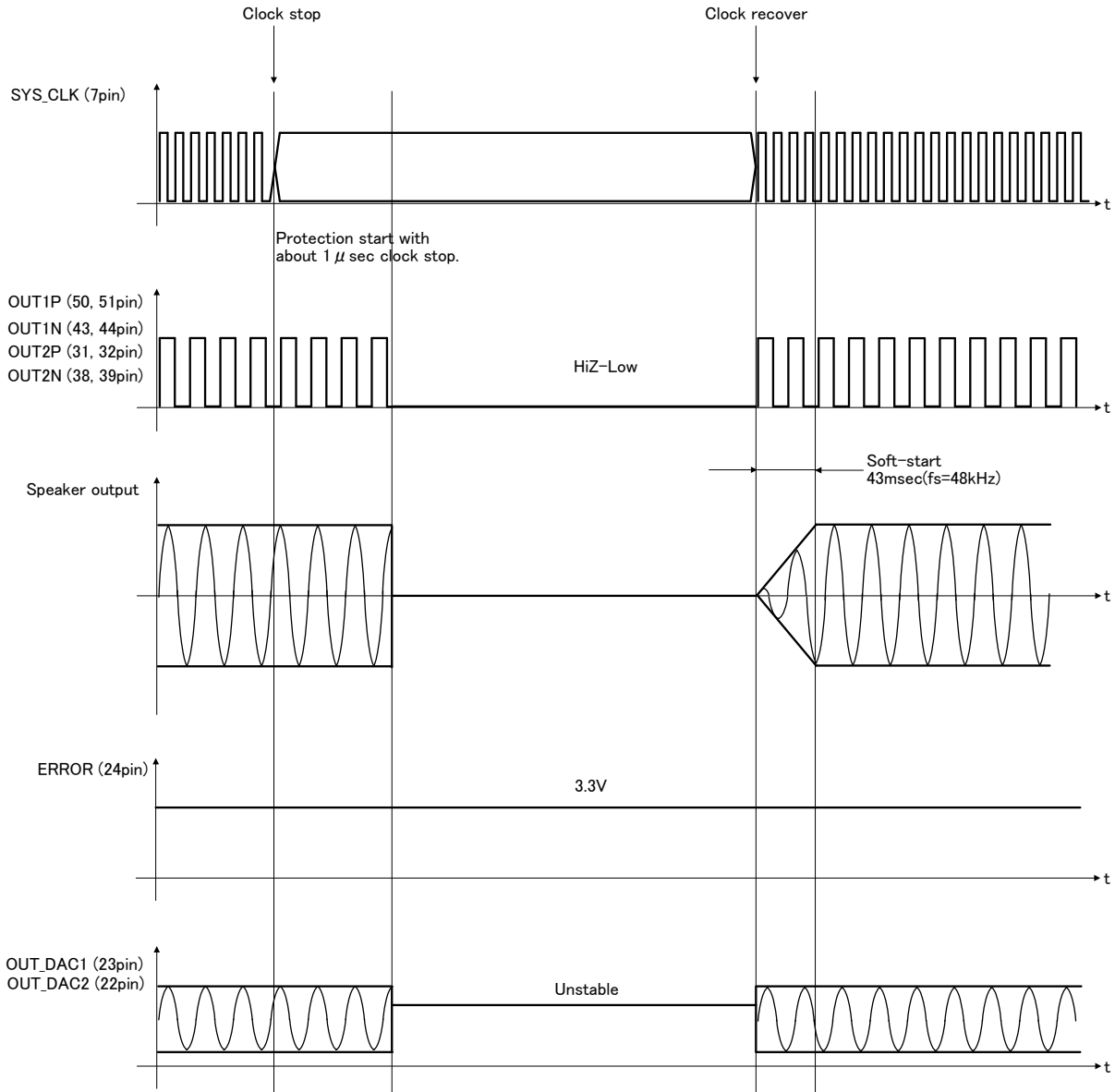


3) Clock stop protection

This IC has the clock stop protection circuit that make the speaker output mute when the SYS_CLK signal of the digital audio input stops.

Detecting condition - It will detect when MUTE pin is set High and the SYS_CLK signal stops for about 1usec or more. The speaker output is muted through a soft-mute when detected.

Releasing condition - It will release when MUTE pin is set High and the SYS_CLK signal returns to the normal clock operation. The speaker output is outputted through a soft-start when released.

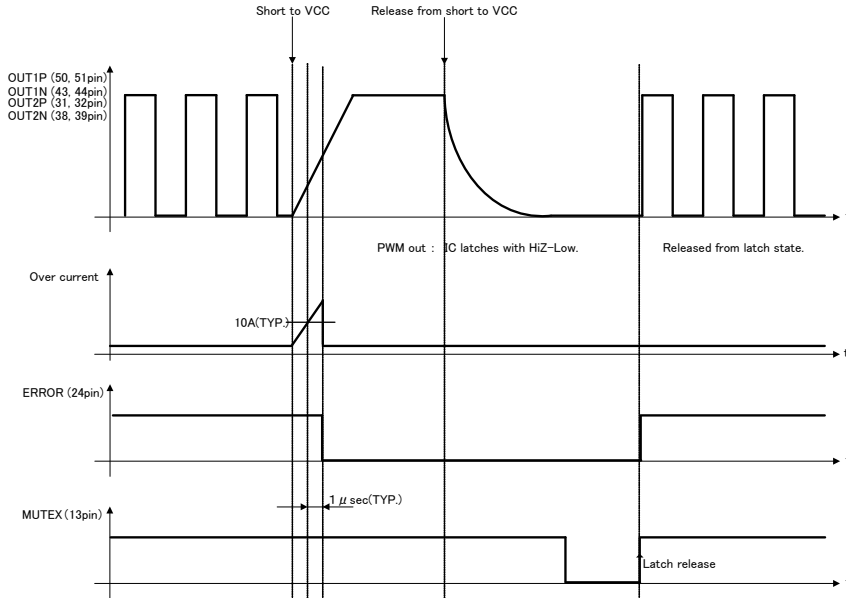


4) Output short protection(Short to the power supply)

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to the power supply due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output pin becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method - ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
 ②Turning on the power supply again.

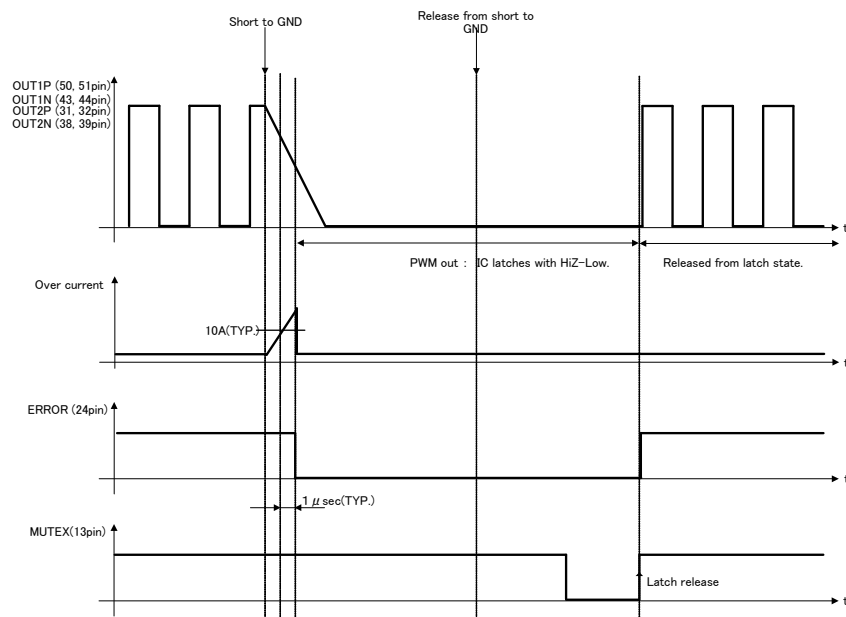


5) Output short protection(Short to GND)

This IC has the PWM output short protection circuit that stops the PWM output when the PWM output is short-circuited to GND due to abnormality.

Detecting condition - It will detect when MUTE pin is set High and the current that flows in the PWM output terminal becomes 10A(TYP.) or more. The PWM output instantaneously enters the state of HiZ-Low if detected, and IC does the latch.

Releasing method – ①After the MUTEX pin is set Low once, the MUTEX pin is set High again.
 ②Turning on the power supply again.

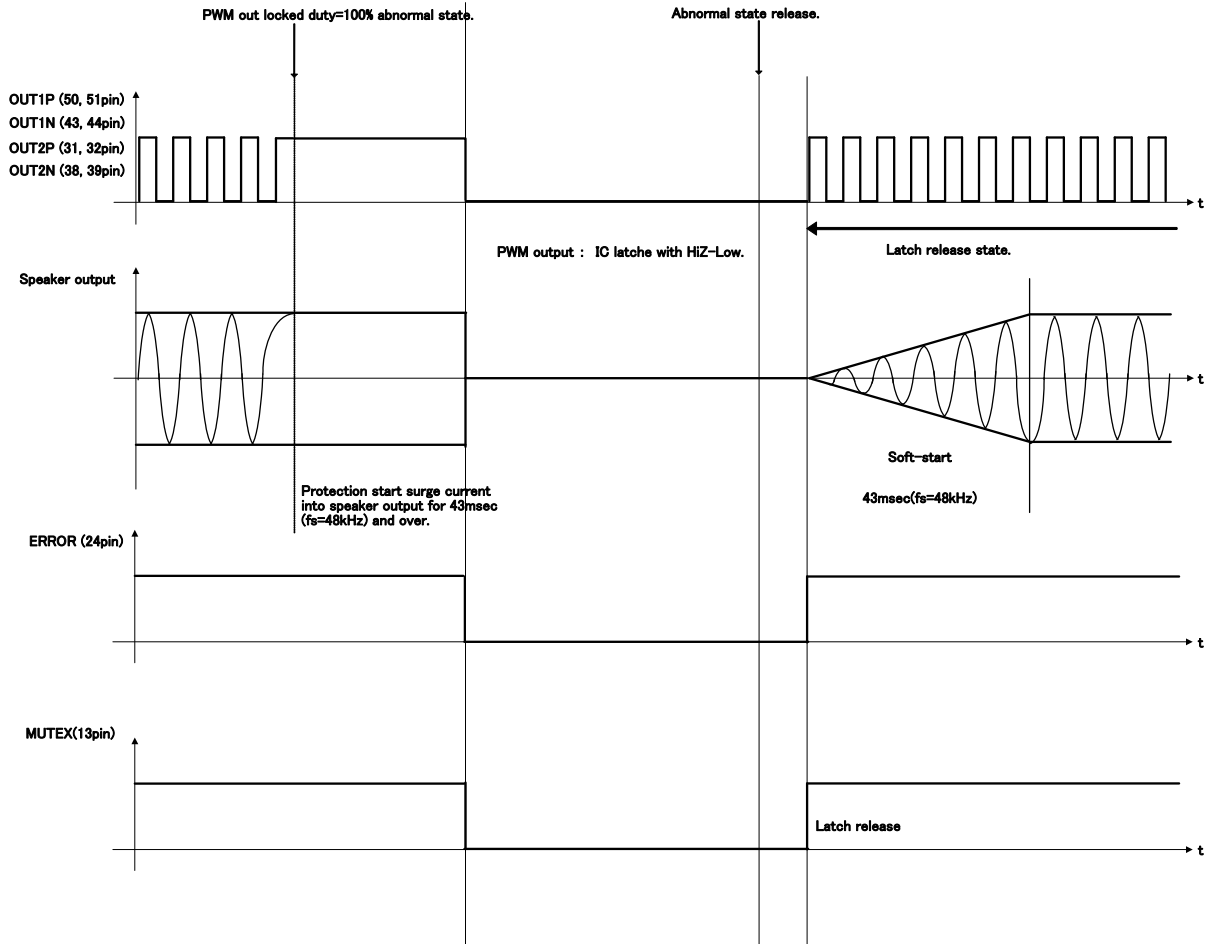


6) DC voltage protection in the speaker

When the DC voltage in the speaker is impressed due to abnormality, this IC has the protection circuit where the speaker is defended from destruction.

Detecting condition - It will detect when MUTE pin is set High or Low and PWM output Duty=0% or 100% , 43msec(fs=48kHz) or above. Once detected, The PWM output instantaneously enters the state of HiZ-Low, and IC does the latch.

Releasing method – ①After the MUTE pin is set Low once, the MUTE pin is set High again.
 ②Turning on the power supply again



●Output power limiter function

This IC is provided with an output power limiter function to protect speakers from destruction by an excessive output. Limiter values are freely specified by changing external resistors R1/R2 as shown in Fig-26. Fig-27 shows a speaker output waveform that is generated with use of the output limiter function. Because the waveform is soft-clipped, unusual noises on audible signals are significantly reduced under operation of limiter.

Use resistors with a high degree of accuracy for R1 and R2 ($\pm 1\%$ or higher accuracy is recommended). The capacitor C is for the noise removal of output power limitation terminal (3pin). Provide grounding with a $1\mu\text{F}$ capacitor. Specify a resistor of $10\text{k}\Omega$ or higher resistor R1 and R2. If the output power limiter function is not used, R1, R2 and C is unnecessary. However, connect 3pin with GNDA.

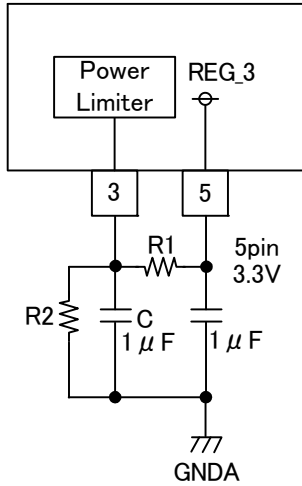


Fig-29

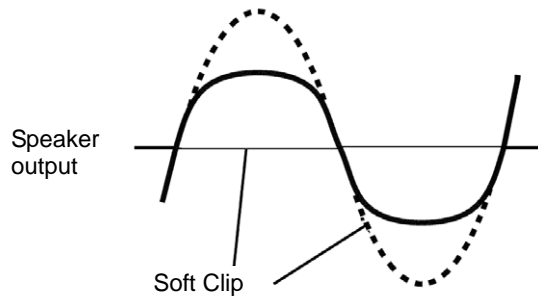


Fig-30

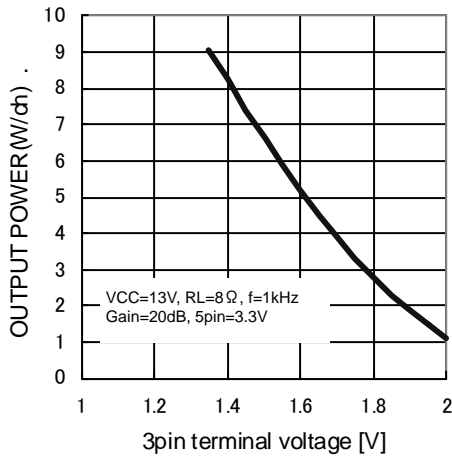
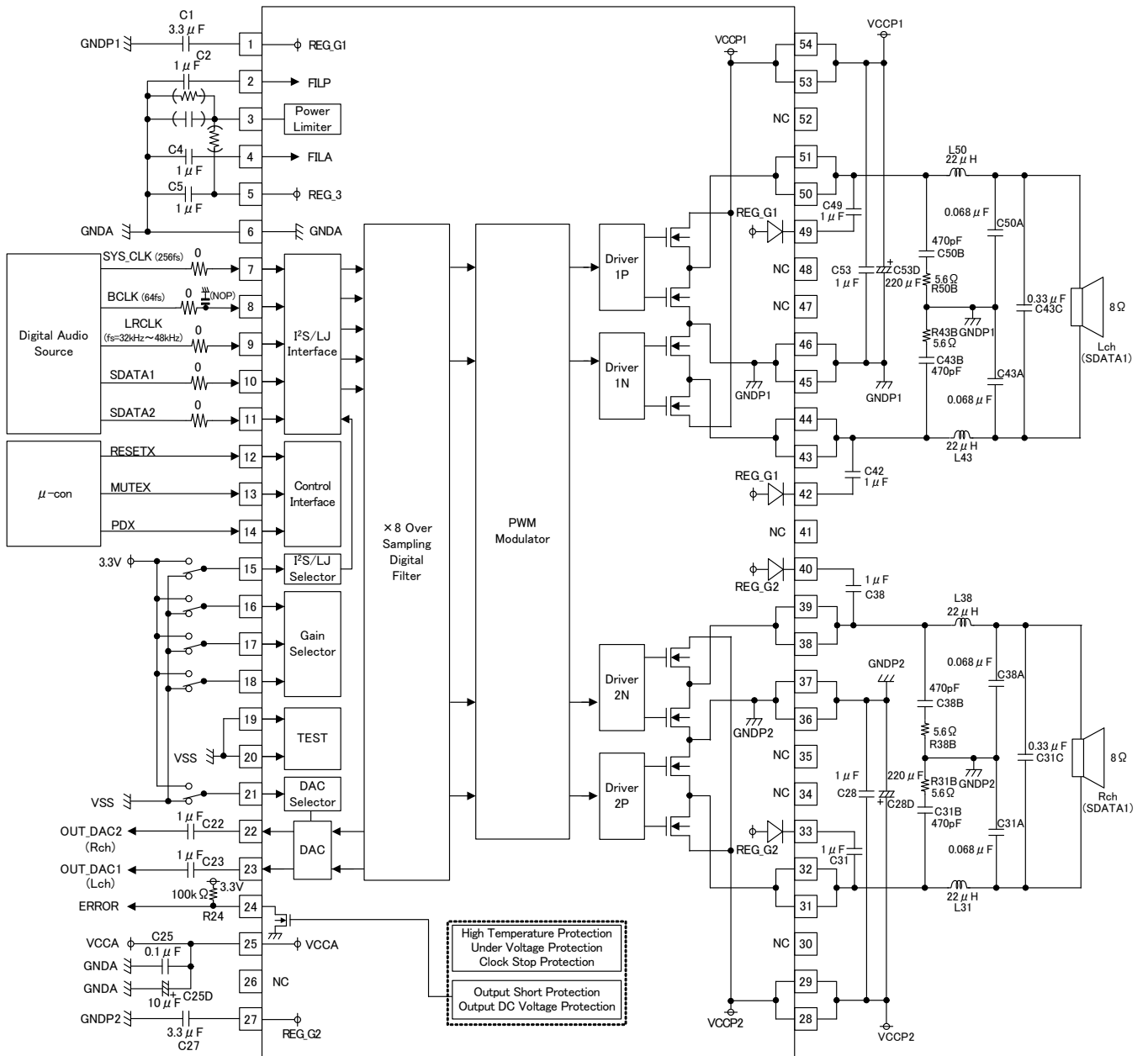


Fig.31

Output power
– 3pin terminal voltage

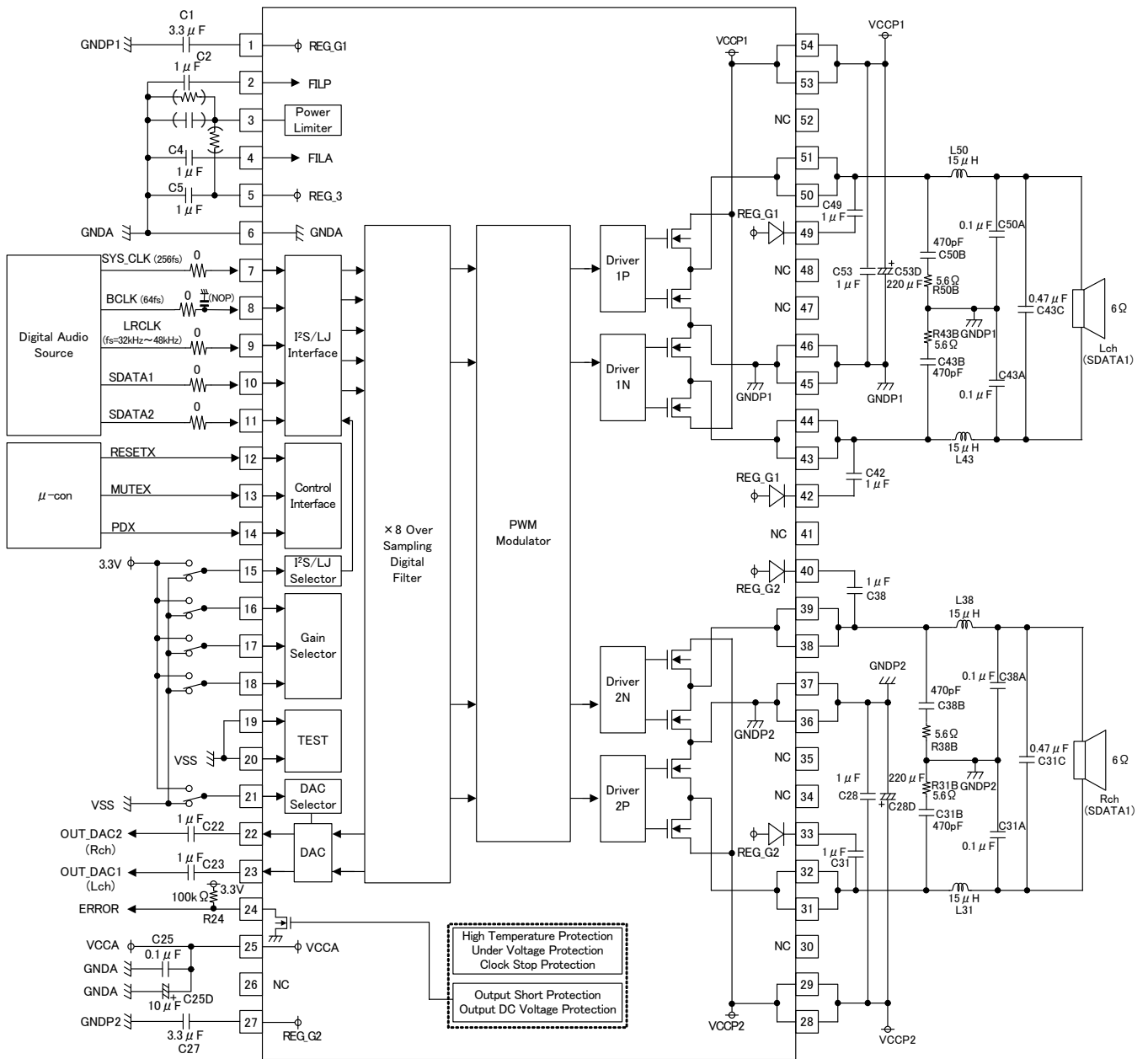
●Application Circuit Example(R_{Lsp}=8Ω)



●BOM list($R_{L_sp}=8\Omega$)

| Parts | Parts No. | Value | Company | Product No. | Rated Voltage | Tolerance | Size |
|------------------------|--------------------------|---------|-----------|-------------------|---------------|-----------|--------------|
| IC | U1 | — | ROHM | BD5446EFV | — | — | 18.5mm×9.5mm |
| Inductor | L31, L38, L43, L50 | 22μH | TOKO | 1168ER-0001 | - | (±20%) | 10.3mm×7.6mm |
| | | | SAGAMI | DBE7210H-220M | - | (±20%) | 10.5mm×6.4mm |
| Resistor | R31B, R38B R43B, R50B | 5.6Ω | ROHM | MCR18PZHFL5R60 | 1/4W | F(±1%) | 3.2mm×1.6mm |
| Capacitor | C31, C38, C42, C49 | 1μF | MURATA | GRM185B31C105KE43 | 16V | B(±10%) | 1.6mm×0.8mm |
| | C25, C28, C53 | 0.1μF | | GRM188B31H104KA92 | 50V | B(±10%) | 1.6mm×0.8mm |
| | C31A, C38A C43A, C50A | 0.068μF | | GRM21BB11H683KA01 | 50V | B(±10%) | 2.0mm×1.25mm |
| | C31C, C43C | 0.33μF | | GRM219B31H334KA87 | 50V | B(±10%) | 2.0mm×1.25mm |
| | C1, C27 | 3.3μF | | GRM188B31A335KE15 | 10V | B(±10%) | 1.6mm×0.8mm |
| | C2, C4, C5 C22, C23 | 1μF | | GRM185B30J105KE25 | 6.3V | B(±10%) | 1.6mm×0.8mm |
| | C31B, C38B C43B, C50B | 470pF | | GRM188B11H471KA | 50V | B(±10%) | 2.0mm×1.2mm |
| Electrolytic Capacitor | C28D, C53D | 220μF | Panasonic | ECA1VMH221 | 35V | ±20% | φ8mm×11.5mm |
| | C25D | 10μF | | EEUFC1H100L | 50V | ±20% | φ5mm×11mm |

●Application Circuit Example(R_{Lsp}=6Ω)



●BOM list($R_{L_sp}=6\Omega$)

| Parts | Parts No. | Value | Company | Product No. | Rated Voltage | Tolerance | Size |
|------------------------|--|--------|-----------|-------------------|---------------|-----------|--------------|
| IC | U1 | — | ROHM | BD5446EFV | — | — | 18.5mm×9.5mm |
| Inductor | L31, L38, L43, L50 | 15μH | SAGAMI | DBE7210H-150M | — | (±20%) | 10.5mm×6.4mm |
| Resistor | R31B, R38B R43B, R50B | 5.6Ω | ROHM | MCR18PZHFL5R60 | 1/4W | F(±1%) | 3.2mm×1.6mm |
| Capacitor | C31, C38, C42, C49 | 1μF | MURATA | GRM185B31C105KE43 | 16V | B(±10%) | 1.6mm×0.8mm |
| | C25, C28, C53, C31A, C38A, C43A, C48A | 0.1μF | | GRM188B31H104KA92 | 50V | B(±10%) | 1.6mm×0.8mm |
| | C31C, C43C | 0.47μF | | GRM21BB31H474KA87 | 50V | B(±10%) | 2.0mm×1.2mm |
| | C1, C27 | 3.3μF | | GRM188B31A335KE15 | 10V | B(±10%) | 1.6mm×0.8mm |
| | C2, C4, C5 C22, C23 | 1μF | | GRM185B30J105KE25 | 6.3V | B(±10%) | 1.6mm×0.8mm |
| | C31B, C38B C43B, C50B | 470pF | | GRM188B11H471KA | 50V | B(±10%) | 2.0mm×1.2mm |
| Electrolytic Capacitor | C28D, C53D | 220μF | Panasonic | ECA1VMH221 | 35V | ±20% | φ8mm×11.5mm |
| | C25D | 10μF | | EEUFC1H100L | 50V | ±20% | φ5mm×11mm |

●Output LC Filter Circuit

An output filter is required to eliminate radio-frequency components exceeding the audio-frequency region supplied to a load (speaker). Because this IC uses sampling clock frequencies from 200kHz to 400kHz in the output PWM signals, the high-frequency components must be appropriately removed.

This section takes an example of an LC type LPF shown in Fig.29, in which coil L and capacitor C compose a differential filter with an attenuation property of -12dB/oct. A large part of switching currents flow to capacitor C, and only a small part of the currents flow to speaker R_L . This filter reduces unwanted emission this way. In addition, coil L and capacitor C_g compose a filter against in-phase components, reducing unwanted emission further.

Filter constants depend on load impedances. The following are formulas to calculate values of L , C , and C_g when $Q=0.707$ is specified.

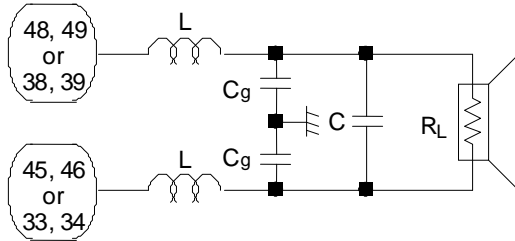


Fig. 29

$$L = \frac{R_L \sqrt{2}}{4 \pi f_c} \text{ (H)}$$

$$C = \frac{1}{2 \pi f_c R_L \sqrt{2}} \text{ (F)}$$

$$C_g = 0.2 C \text{ (F)}$$

R_L : Load impedance (Ω)

f_c : LPF cut off frequency (Hz)

Following presents output LC filter constants with typical load impedances.

| $f_c = 30\text{kHz}$ | | | |
|----------------------|------------------|--------------------|---------------------|
| R_L | L | C | C_g |
| 6 Ω | 22 μH | 0.68 μF | 0.15 μF |
| 8 Ω | 33 μH | 0.47 μF | 0.1 μF |
| 16 Ω | 68 μH | 0.22 μF | 0.047 μF |

| $f_c = 40\text{kHz}$ | | | |
|----------------------|------------------|--------------------|---------------------|
| R_L | L | C | C_g |
| 6 Ω | 15 μH | 0.47 μF | 0.1 μF |
| 8 Ω | 22 μH | 0.33 μF | 0.068 μF |
| 16 Ω | 47 μH | 0.15 μF | 0.033 μF |

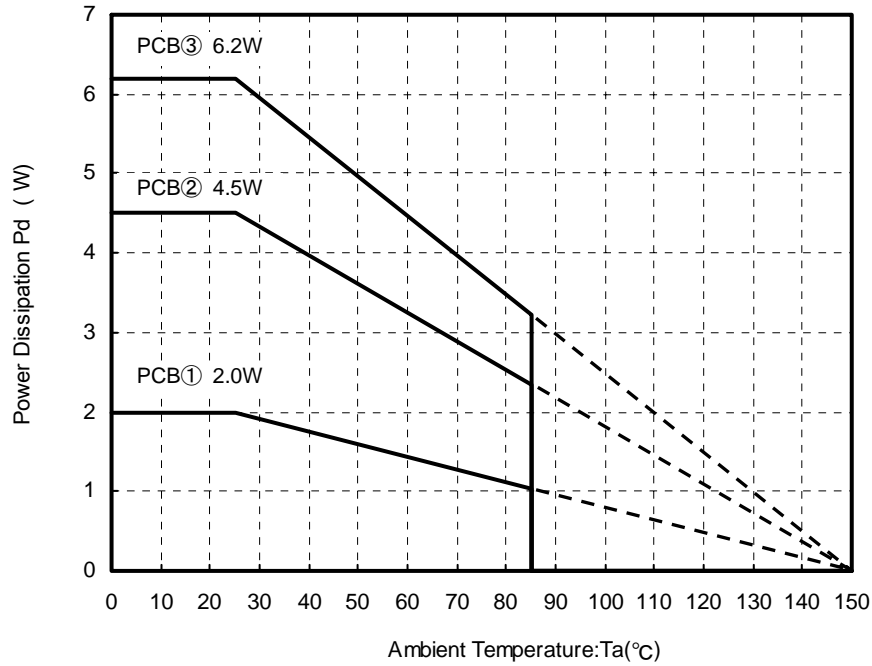
Use coils with a low direct-current resistance and with a sufficient margin of allowable currents. A high direct-current resistance causes power losses. In addition, select a closed magnetic circuit type product in normal cases to prevent unwanted emission.

Use capacitors with a low equivalent series resistance, and good impedance characteristics at high frequency ranges (100kHz or higher). Also, select an item with sufficient withstand voltage because flowing massive amount of high-frequency currents is expected.

●Notes for use

- 1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure such as a fuse should be implemented when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.
- 2) Power supply lines
As return of current regenerated by back EMF of output coil happens, take steps such as putting capacitor between power supply and GND as a electric pathway for the regenerated current. Be sure that there is no problem with each property such as emptied capacity at lower temperature regarding electrolytic capacitor to decide capacity value. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.
- 3) GND potential(Pin 6, 36, 37, 45, 46).
Any state must become the lowest voltage about GND terminal and VSS terminal.
- 4) Input terminal
The parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND and VSS. Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed.
- 5) Setting of heat
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. This IC exposes its frame of the backside of package. Note that this part is assumed to use after providing heat dissipation treatment to improve heat dissipation efficiency. Try to occupy as wide as possible with heat dissipation pattern not only on the board surface but also the backside.
Class D speaker amplifier is high efficiency and low heat generation by comparison with conventional Analog power amplifier. However, In case it is operated continuously by maximum output power, Power dissipation (Pdiss) may exceed package dissipation. Please consider about heat design that Power dissipation (Pdiss) does not exceed Package dissipation (Pd) in average power (Poav). (Tjmax : Maximum junction temperature=150°C, Ta : Peripheral temperature[°C], θja : Thermal resistance of package[°C/W], Poav : Average power[W], η : Efficiency)
Package dissipation : $Pd(W) = (Tjmax - Ta) / \theta ja$
Power dissipation : $Pdiss(W) = Poav \times (1/\eta - 1)$
- 6) Actions in strong magnetic field
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.
- 7) Thermal shutdown circuit
This product is provided with a built-in thermal shutdown circuit. When the thermal shutdown circuit operates, the output transistors are placed under open status. The thermal shutdown circuit is primarily intended to shut down the IC avoiding thermal runaway under abnormal conditions with a chip temperature exceeding Tjmax = 150°C.
- 8) Shorts between pins and misinstallation
When mounting the IC on a board, pay adequate attention to orientation and placement discrepancies of the IC. If it is misinstalled and the power is turned on, the IC may be damaged. It also may be damaged if it is shorted by a foreign substance coming between pins of the IC or between a pin and a power supply or a pin and a GND.
- 9) Power supply on/off (Pin 25, 28, 29, 53, 54)
In case power supply is started up, RESETX(Pin 12), MUTEX(Pin 13) and PDX (Pin 14) always should be set Low. And in case power supply is shut down, it should be set Low likewise. Then it is possible to eliminate pop noise when power supply is turned on/off. And also, all power supply terminals should start up and shut down together.
- 10) ERROR terminal(Pin 24)
A error flag is outputted when Output short protection and DC voltage protection in the speaker are operated. These flags are the function which the condition of this product is shown in.
- 11) N.C. terminal(Pin 26, 30, 34, 35, 41, 47, 48, 52)
N.C. terminal (Non Connection Pin) does not connect to the inside circuit. Therefore, possible to use open.
- 12) TEST terminal(Pin 19, 20)
TEST terminal connects with ground to prevent the malfunction by external noise.
- 13) Precautions for Spealer-setting
If the impedance characteristics of the speakers at high-frequency range while increase rapidly, the IC might not have stable-operation in the resonance frequency range of the LC-filter. Therefore, consider adding damping-circuit, etc., depending on the impedance of the speaker.
- 14) Notes about the phase of SYS_CLK (Pin7) and BCLK (Pin8)
If the rising edge of SYS_CLK (Pin7) and BCLK (Pin8) becomes simultaneous, noise or sound shutdown may occur.
Please cope with it, when the rising edge of CYC_CLK and BCLK becomes simultaneous. (Example: Insert RC filter in BCLK)

● Allowable Power Dissipation



Measuring instrument : TH-156(Shibukawa Kuwano Electrical Instruments Co., Ltd.)

Measuring conditions : Installation on ROHM's board

Board size : 70mm×70mm×1.6mm(with thermal via on board)

Material : FR4

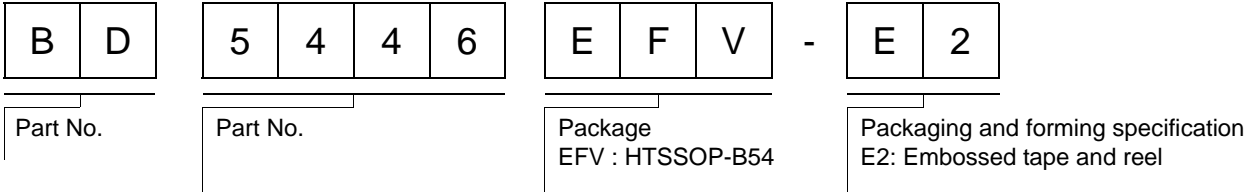
• The board on exposed heat sink on the back of package are connected by soldering.

PCB① : 1-layer board(back copper foil size: 0mm×0mm), $\theta_{ja}=62.5^{\circ}\text{C}/\text{W}$

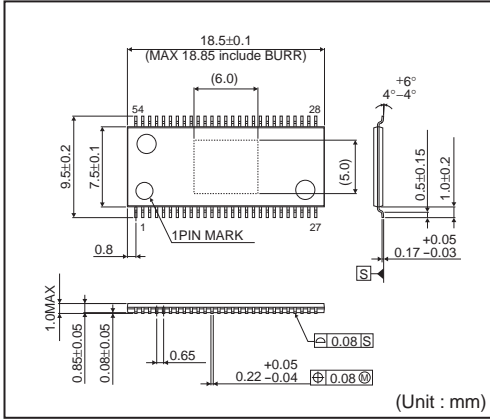
PCB② : 2-layer board(back copper foil size: 70mm×70mm), $\theta_{ja}=27.8^{\circ}\text{C}/\text{W}$

PCB③ : 4-layer board(back copper foil size: 70mm×70mm), $\theta_{ja}=20.2^{\circ}\text{C}/\text{W}$

●Ordering part number

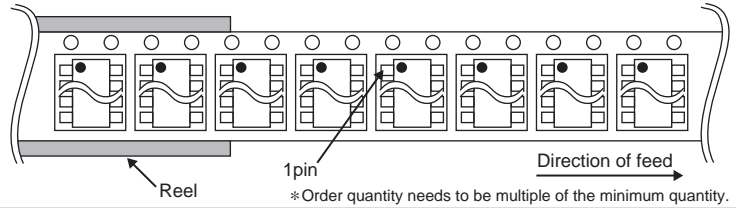


HTSSOP-B54



<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape (with dry pack) |
| Quantity | 1500pcs |
| Direction of feed | E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |



Notice

Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - Installation of protection circuits or other protective devices to improve system safety
 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

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