TS81001

High Efficiency Receiver Controller for Wireless Power Systems

TRIUNE PRODUCTS

Features

- Supports Qi®, PMA and proprietary charging applications
- Dual-mode Qi + PMA functionality using a single LC resonant circuit
- Wireless power systems up to 40W+
- Compatible with variable voltage, variable frequency and variable duty cycle transmitters
- Supports indirect (fixed voltage) and single/multi-cell battery charging applications (>2.0V)
- Integrated controller and FLASH for communications and control
- High precision data converter

Low external component count

Applications

- Qi® , PMA and non-standard wireless chargers for:
  - Cell Phones and Smartphones
  - GPS Devices
  - Digital Cameras
  - Tablets and eReaders
  - Portable Lighting
- Toys
- Medical devices
- Industrial devices Description

Description

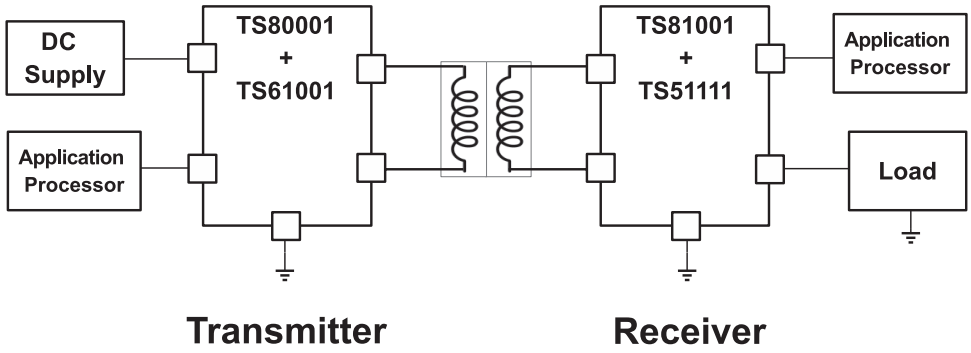
The TS81001 is a power receiver communications and control unit for wireless charging applications. The TS81001 can support systems up to 40W+, and supports Qi® compliant, PMA compliant and proprietary applications.

The TS81001 performs the necessary coding of packets to send commands to the transmitter to adjust the power level accordingly.

Specification

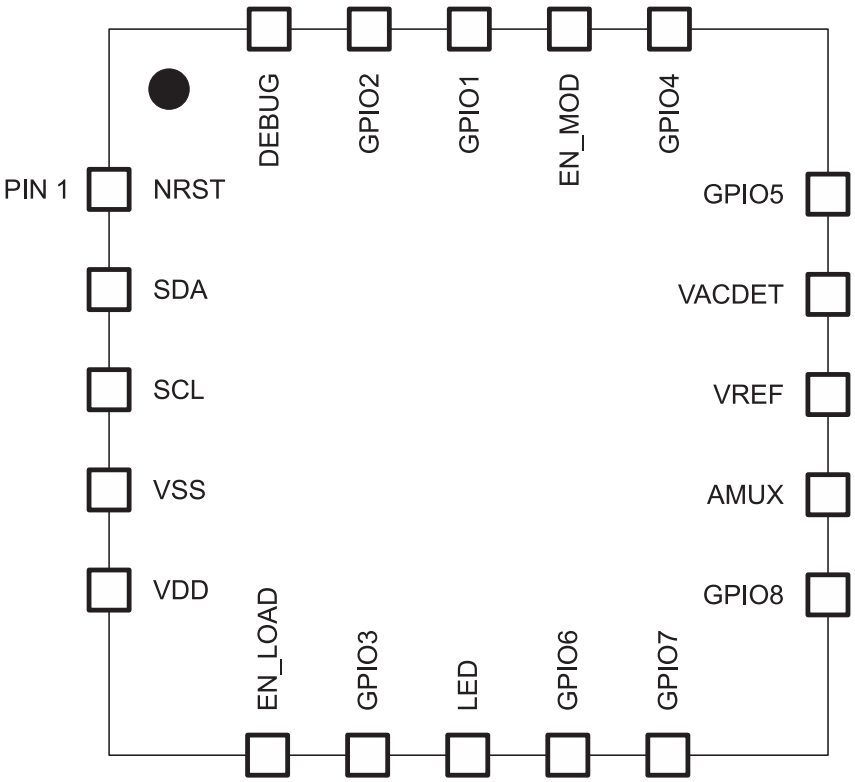
- RISC-based controller core with flash and SRAM memory
- 12-bit A/D converter
- Two 16-bit timers
- 8-bit timer
- Auto-wakeup and watchdog timers
- 8 configurable analog general purpose IOs
- Charging LED output
- I2C interface
- 20 pin 3x3 QFN

Typical Application Circuit



Pinout

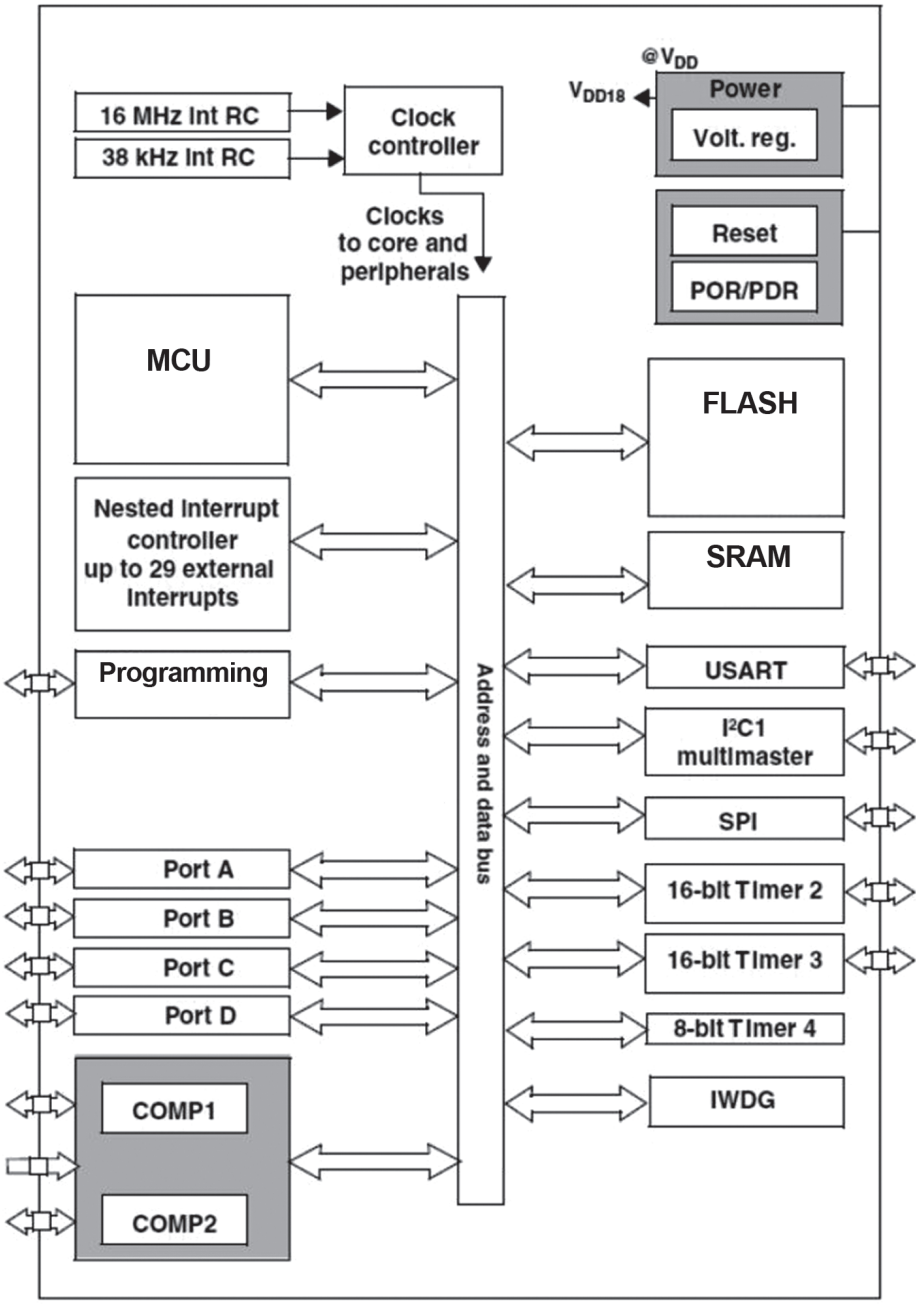
(Top View)



Pin Description

Pin #	Pin Name	Pin Function	Description
1	NRST	Reset	Reset input
2	SDA	I2C Data	I2C data
3	SCL	I2C Clock	I2C clock
4	VSS	Power GND	Power GND
5	VDD	Input power	Input power supply
6	EN_LOAD	Load enable	Output FET enable (some systems)
7	GPIO3	GPIO	GPIO 3
8	LED	LED output	Charging LED control
9	GPIO6	GPIO	GPIO 6
10	GPIO7	GPIO	GPIO 7
11	GPIO8	GPIO	GPIO 8
12	AMUX	Analog GPIO	AMUX input from TS51111
13	VREF	Analog GPIO	VREF input from TS51111
14	VACDET	GPIO	VACDET input from TS51111
15	GPIO5	Open-Drain GPIO	True Open-Drain GPIO 5
16	GPIO4	Open-Drain GPIO	True Open-Drain GPIO 4
17	EN_MOD	GPIO	EN_MOD output to TS51111
18	GPIO1	GPIO	GPIO 1
19	GPIO2	GPIO	GPIO 2
20	DEBUG	Debug	Debug interface

Functional Block Diagram



Absolute Maximum Ratings

Over operating free–air temperature range unless otherwise noted[1, 2, 3]

	MIN	MAX	UNIT
VDD, VSS	-0.3	4.0	V
GPIO1, GPIO2, GPIO3, VACDET, VREF, SCL, SDA, EN_MOD, DEBUG, GPIO6, AMUX, EN_LOAD, GPIO7, LED, GPIO8, NRST	VSS - 0.3	4.0	V
GPIO4, GPIO5	VSS - 0.3	VDD + 4.0	V
Operating Junction Temperature Range, TJ	-40	125	°C
Storage Temperature Range, TSTG	-65	150	°C
Electrostatic Discharge – Human Body Model		±2k	V
Lead Temperature (soldering, 10 seconds)		260	°C

Notes:
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) ESD testing is performed according to the respective JESD22 JEDEC standard.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Input Operating Voltage	1.85		3.6	V
F_{MCU}	Operating Frequency	2		16	MHz
VDD	Decoupling capacitor value		1		uF
LDO	Decoupling capacitor value		1		uF
TA	Operating Free Air Temperature	-40		85	°C
TJ	Operating Junction Temperature	-40		105	°C

Communication Interfaces

I2C or UART communication can only take place in the following cases:

- The Wireless Power Receiver is placed on the Wireless Power Transmitter and power transfer is taking place, or
- External power is applied, either through the system power supply or on the TS51111 USB pin

In both cases, an internal voltage regulator inside the TS51111 provides 3.3V on the VCORE pin for the TS81001 to use.

The Applications Processor can interrogate the TS81001 using the I2C or UART interfaces. The TS81001 acknowledges its I2C Slave Address only if it is powered. No ACK from the TS81001 after its slave address means that power transfer does not take place and power is not applied to the TS51111 USB pin.

I2C

I2C Signal Pins

- ALERT pin (GPIO pin) - optional:
  - Driven high when an event is active in the internal STATUS register
  - Driven low when all the internal events are cleared

Note: The ALERT pin is provided to help with I2C communication, i.e. to signal events to the EC so the EC can interrogate the TS8100x via I2C. The use of the ALERT pin is not mandatory in the application.

- SCL_TXD pin:
  - Clock pin for the I2C interface.
  - True open-drain. Needs external pull-ups.

- SDA_RXD pin:
  - Data pin for the I2C interface.
  - True open-drain. Needs external pull-ups.

I2C Protocol

The TS81001 Wireless Power Receiver acts as an I2C slave peripheral to allow communication with an application microcontroller. The slave address (7 bit) is 0x49. The Embedded Controller is an I2C master and initiates every data transfer.

The TS81001 implements a set of registers available from the I2C bus. It also implements a set of API functions that receive parameters and return values using the I2C bus. Four transfer types are possible:

- Write Register
- Read Register
- Run API Function
- Read API Function Return Buffer

Write Register Operations				**Description**
START				Start of the I2C transfer
M⇨S	Slave Address (7 bits)	**0** (1 bit)	Slave ACK	Slave address + R/nW bit (0x92 as 8-bit).
M⇨S	Register *n* address (8 bits)		Slave ACK	Address of the first register.
M⇨S	Register *n* Data (8 bits)		Slave ACK	Write the first register.
M⇨S	Register *n+1* Data (8 bits)		Slave ACK	Optionally write the following registers.
	...			
M⇨S	Register *n+k* Data (8 bits)		Slave ACK	
STOP				Stop of the I2C transfer.

Read Register Operations				Description
START				Start of the I2C transfer
M⇨S	Slave Address (7 bits)	**0** (1 bit)	Slave ACK	Slave address + 0 as R/nW bit (0x92 as 8-bit).
M⇨S	Register *n* address (8 bits)		Slave ACK	Address of the first register.
START				Repeated Start.
M⇨S	Slave Address (7 bits)	**1** (1 bit)	Slave ACK	Slave address + 1 as R/nW bit (0x93 as 8-bit).
S⇨M	Register *n* Data (8 bits)		Master ACK	Read the first register.
S⇨M	Register *n+1* Data (8 bits)		Master ACK	Optionally read the following registers.
	...			
S⇨M	Register *n+k* Data (8 bits)		Slave ACK	The master should send a nACK after the last data byte was received.
STOP				Stop of the I2C transfer.

Run API Function Operations				Description
START				Start of the I2C transfer
M⇨S	Slave Address (7 bits)	**0** (1 bit)	Slave ACK	Slave address + R/nW bit (0x92 as 8-bit).
M⇨S	API number (8 bits)		Slave ACK	API number.
M⇨S	API input buffer length m (8 bits)		Slave ACK	API input buffer length. Equal to 0 if no input buffer data is required by the API.
M⇨S	Input buffer data[0] (8 bits)		Slave ACK	First byte of the input buffer (optional).
M⇨S	Input buffer data[1] (8 bits)		Slave ACK	Second byte of the input buffer (optional).
	...			
M⇨S	Input buffer data[m-1] (8 bits)		Slave ACK	Last byte of the input buffer (optional).
STOP				Stop of the I2C transfer and execute the API function

Read API Function Return Buffer				Description
START				Start of the I2C transfer
M⇨S	Slave Address (7 bits)	**0** (1 bit)	Slave ACK	Slave address + R/nW bit (0x92 as 8-bit).
M⇨S	Register *n* address (8 bits)		Slave ACK	API number.
START				Repeated Start.
M⇨S	Slave Address (7 bits)	**1** (1 bit)	Slave ACK	Slave address + 1 as R/nW bit (0x93 as 8-bit).
S⇨M	API number (8 bits)		Master ACK	API number for the following return buffer.
S⇨M	API return buffer length n (8 bits)		Master ACK	API return buffer length.
S⇨M	Output buffer data[0] (8 bits)		Master ACK	Read the first byte in the output buffer.
S⇨M	Output buffer data[1] (8 bits)		Master ACK	Optionally read the following bytes.
	...			
S⇨M	Output buffer data[n-1] (8 bits)		Master nACK	The master should send a nACK after the last data byte was received.
STOP				Stop of the I2C transfer.

Internal Registers

Address	Name	Type	Description
0x00	BOOTFW_REV_L	R/W	Bootloader Firmware Revision Low Register
0x01	BOOTFW_REV_H	R/W	Bootloader Firmware Revision High Register
0x02	FW_REV_L	R/W	Firmware Revision Low Register
0x03	FW_REV_H	R/W	Firmware Revision High Register
0x04	MODE_L	R/W	Operating Mode Low Register
0x05	MODE_H	R/W	Operating Mode High Register
0x06	RESET_L	R/W	Reset Low Register
0x07	RESET_H	R/W	Reset High Register
0x08	STATUS	R	Main Status Register
0x09	STATUS0	R	Status0 Register
0x0A	STATUS1	R	Status1 Register
0x0B	STATUS2	R	Status2 Register
0x0C	STATUS3	R	Status3 Register
0x0D-0x7F	RESERVED. Will be defined later.		

Bootloader Firmware Revision Low Register (BOOTFW_REV_L)

Address: 0x00

Reset value: Minor version number of the bootloader firmware

7	6	5	4	3	2	1	0
REV_L[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 **REV_L[7:0]**: Bootloader Firmware Revision Low

These bits contain the minor version number of the bootloader firmware.

Bootloader Firmware Revision High Register (BOOTFW_REV_H)

Address: 0x01

Reset value: Major version number of the bootloader firmware

7	6	5	4	3	2	1	0
REV_H[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 **REV_H[7:0]**: Bootloader Firmware Revision High

These bits contain the major version number of the bootloader firmware.

Firmware Revision Low Register (FW_REV_L)

Address: 0x02

Reset value: Minor version number of the user firmware

7	6	5	4	3	2	1	0
REV_L[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 **REV_L[7:0]**: Firmware Revision Low

These bits contain the minor version number of the user firmware.

Firmware Revision High Register (BOOTFW_REV_H)

Address: 0x03

Reset value: Major version number of the user firmware

7	6	5	4	3	2	1	0
REV_H[7:0]							
r	r	r	r	r	r	r	r

Bits 7:0 **REV_H[7:0]**: Bootloader Firmware Revision High

These bits contain the major version number of the user firmware.

Operating Mode Low Register (MODE_L)

Address: 0x04

Reset value: Depends on the bootloader mode and the firmware type

7	6	5	4	3	2	1	0
Res							BOOTLDR
							r

Bits 7:1 Reserved

Bit 0 BOOTLDR: Bootloader mode

0: The user firmware is running

1: The controller is in bootloader mode

Operating Mode High Register (MODE_H)

Address: 0x05

Reset value: Depends on the bootloader mode and the firmware type

7	6	5	4	3	2	1	0
Res							

Bits 7:0 Reserved

Reset Low Register (RESET_L)

Address: 0x06

Reset value: 0x00

7	6	5	4	3	2	1	0
RESET_KEY_L[7:0]							
w	w	w	w	w	w	w	w

Bits 7:0 RESET_KEY_L[7:0]: Reset Key

0x55: generate a system reset. Both the RESET_L and the RESET_H registers have to be written with the correct key to generate a reset.

Any other value: a system reset is not generated.

Reset High Register (RESET_H)

Address: 0x07

Reset value: 0x00

7	6	5	4	3	2	1	0
RESET_KEY_H[7:0]							
w	w	w	w	w	w	w	w

Bits 7:0 RESET_KEY_H[7:0]: Reset Key

0xAA: generate a system reset. Both the RESET_L and the RESET_H registers have to be written with the correct key to generate a reset.

Any other value: a system reset is not generated.

Main Status Register (STATUS)

Address: 0x08

Reset value: 0xC0

7	6	5	4	3	2	1	0
CTS	CTS_API	Res		STATUS3	STATUS2	STATUS1	STATUS0
rw	rw			rw	rw	rw	rw

Bit 7 CTS: Clear To Send

This bit indicates if a new command can be issued to the controller.

0: The controller is busy processing a previous command. New commands should not be sent to the controller.

1: The controller can accept a new command over the communication interface.

Bit 6 CTS_API: Clear to Send for API

This bit indicates if a new API call can be issued to the controller.

0: The controller is busy processing a previous API call. New API calls should not be sent to the controller.

1: The controller can accept a new API call over the communication interface.

Bits 5:4 Reserved

Bit 3 STATUS3: STATUS3 Event Flag

0: No event is signaled in the STATUS3 register

1: An event is signaled in the STATUS3 register

Bit 2 STATUS2: STATUS2 Event Flag

0: No event is signaled in the STATUS2 register

1: An event is signaled in the STATUS2 register

Bit 1 STATUS1: STATUS1 Event Flag

0: No event is signaled in the STATUS1 register

1: An event is signaled in the STATUS1 register

Bit 0 STATUS0: STATUS0 Event Flag

0: No event is signaled in the STATUS0 register

1: An event is signaled in the STATUS0 register

API Functions

API Number	API Name	Description
0x80	BOOTLOADER_UNLOCK_FLASH	Allow changes to the FLASH memory
0x81	BOOTLOADER_WRITE_BLOCK	Write a page into the FLASH memory
0x82	BOOTLOADER_CRC_CHECK	Check the CRC of the user firmware
0x83-0xFE	RESERVED. Will be defined later.	
0xFF	API_ERROR	Value returned in the API field when a Read API Function Return Buffer command is issued and the API function called previously has generated an error.

Bootloader Unlock Flash (BOOTLOADER_UNLOCK_FLASH)

API number: 0x80
Input buffer size: TBD
Output buffer size: 1

Buffer	Parameter	Length (bytes)	Description
Input buffer	TBD		
Return data buffer	ERROR_CODE	1	

Bootloader Write Block (BOOTLOADER_WRITE_BLOCK)

API number: 0x81
Input buffer size: 66
Output buffer size: 1

Buffer	Parameter	Length (bytes)	Description
Input buffer	Block Number	2	Block index. The first block has an index of 0.
	Block Data	64	Data to be written to the FLASH page.
Return data buffer	ERROR_CODE	1	

Bootloader CRC Check (BOOTLOADER_CRC_CHECK)

API number: 0x82
Input buffer size: 0
Output buffer size: 1

Buffer	Parameter	Length (bytes)	Description
Return data buffer	ERROR_CODE	1	

API Error Codes

Error Code	Error Code Name	Description
0x00	ERROR_GENERIC	Generic error.
0x01	ERROR_OK	Operation succeeded. This is not indicating an error.
0x02	ERROR_INVALID_CRC	CRC error.
0x03	ERROR_FLASH_UNLOCK_FAILED	FLASH unlocking has failed.
0x04	ERROR_API_NOT_IMPLEMENTED	The API number is not implemented.
0x05	ERROR_API_DATA_OVERFLOW	The API input buffer has been filled with more data than its length.
0x06	ERROR_API_INVALID_PARAMETERS	At least one of the API parameters is invalid.
0x07-0xFF	RESERVED. Will be defined later.	

Application Schematic

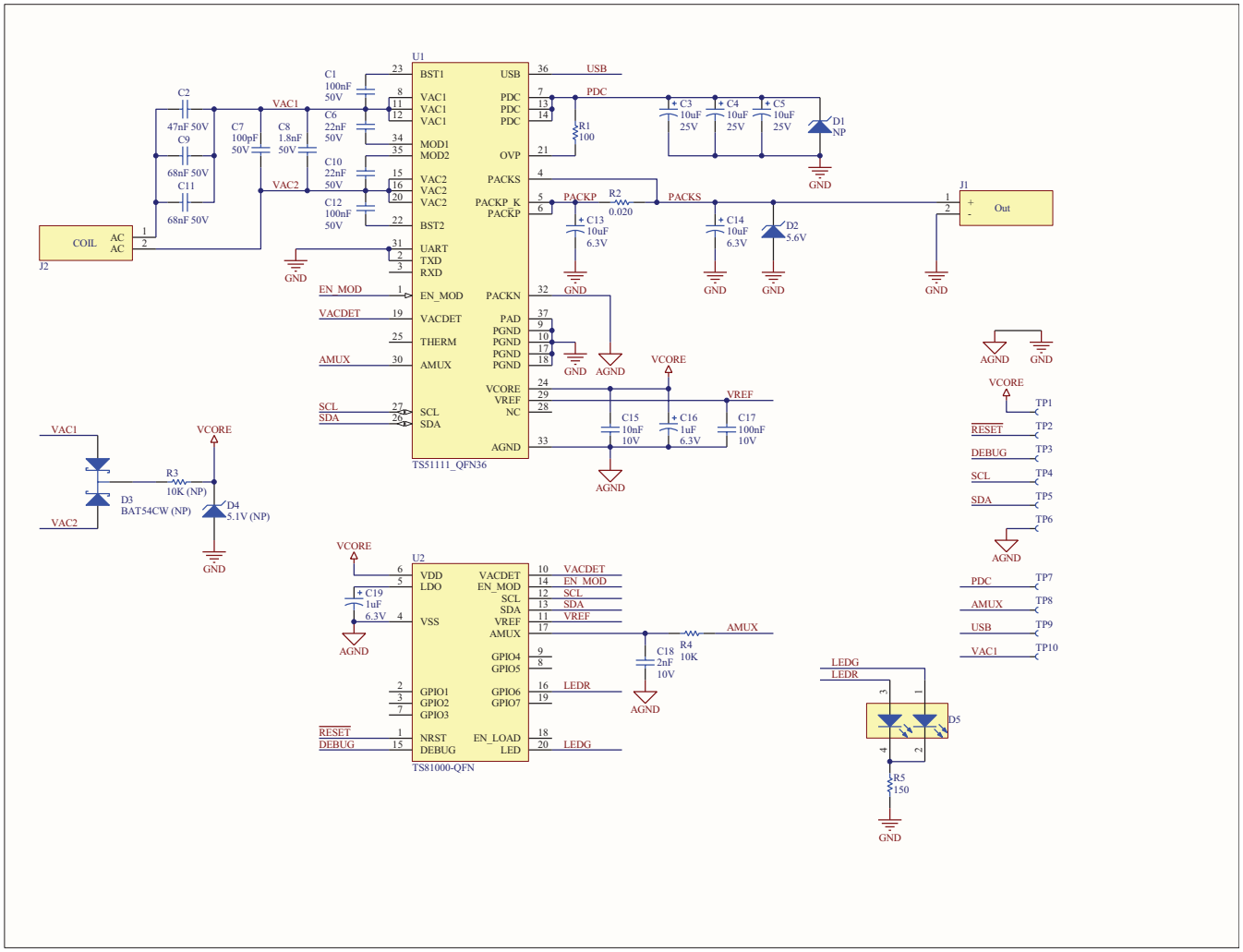
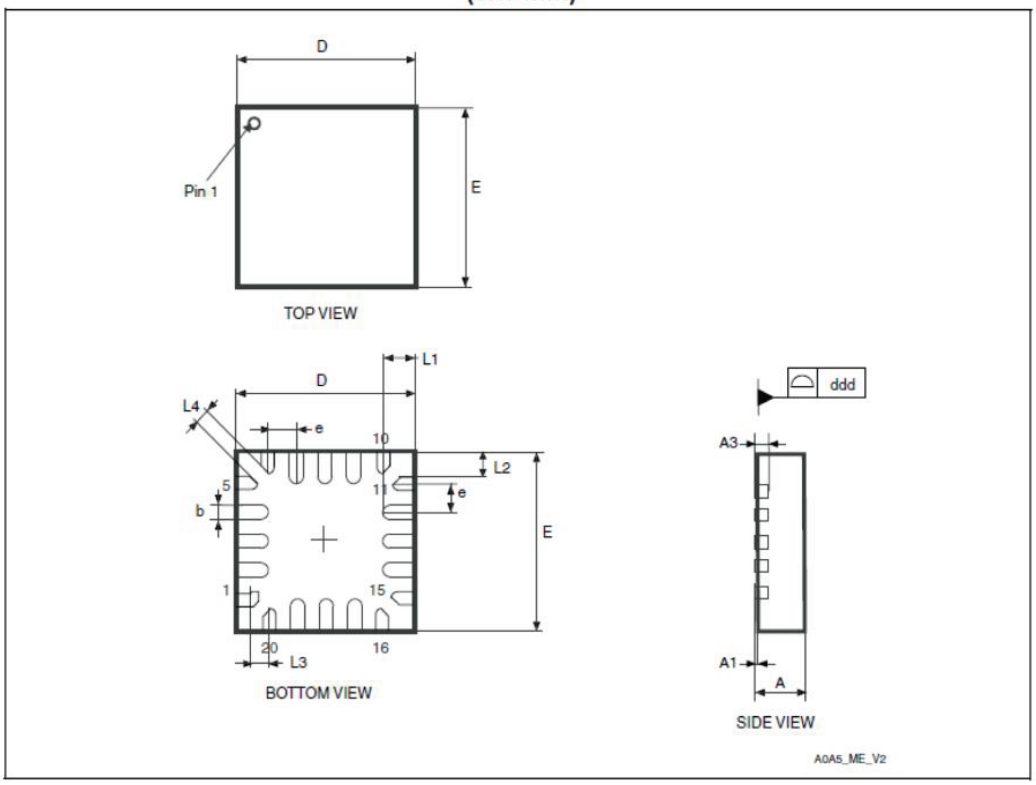


Figure 1: TS81001 Application Schematic

Package Dimensions

Figure 43. UFQFPN20 - 20-lead ulltra thin fine pitch quad flat package outline (3x3 mm)



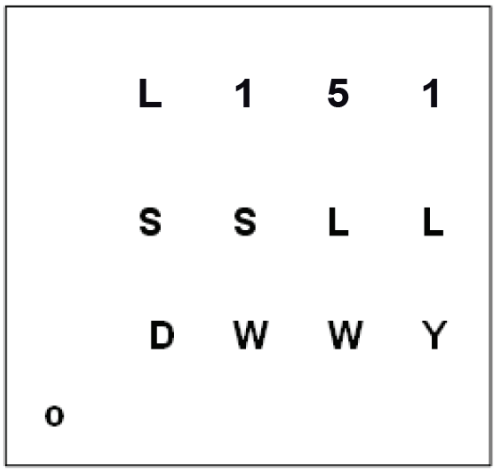
1. Drawing is not to scale.

Table 42. UFQFPN20 - 20-lead ulltra thin fine pitch quad flat package (3 x 3 mm) mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	2.900	3.000	3.100	-	0.1181	-
E	2.900	3.000	3.100	-	0.1181	-
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0	0.020	0.050	0	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
e	-	0.500	-	-	0.0197	-
L1	0.500	0.550	0.600	0.0197	0.0217	0.0236
L2	0.300	0.350	0.400	0.0118	0.0138	0.0157
L3	-	0.375	-	-	0.0148	-
L4	-	0.200	-	-	0.0079	-
b	0.180	0.250	0.300	0.0071	0.0098	0.0118
ddd	-	0.050	-	-	0.0020	-

1. Values in inches are rounded to 4 decimal digits

QFN Package (Top marking)



Legend:

Line 1 Marking:	L151	Internal part code
Line 2 Marking:	SS	Assembly site identifier
	LL	Lot trace code
Line 3 Marking:	D	Assembly year
	WW	Assembly week
	Y	Additional marking
	o	Pin 1 Identifier

Ordering Information

Part Number	Description
TS81001-QFNR	Bootloader programmed device

RoHS and Reach Compliance

Triune Systems is fully committed to environmental quality. All Triune Systems materials and suppliers are fully compliant with RoHS (European Union Directive 2011/65/EU), REACH SVHC Chemical Restrictions (EC 1907/2006), IPC-1752 Level 3 materials declarations, and their subsequent amendments. Triune Systems maintains certified laboratory reports for all product materials, from all suppliers, which show full compliance to restrictions on the following:

- Cadmium (Cd)
- Chlorofluorocarbons (CFCs)
- Chlorinate Hydrocarbons (CHCs)
- Halons (Halogen free)
- Hexavalent Chromium (CrVI)
- Hydrobromofluorocarbons (HBFCs)
- Hydrochlorofluorocarbons (HCFCs)
- Lead (Pb)
- Mercury (Hg)
- Perfluorocarbons (PFCs)
- Polybrominated biphenyls (PBB)
- Polybrominated Diphenyl Ethers (PBDEs)

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