DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ max	I_D max T_A = +25°C
60V	3Ω @ V_{GS} = 5V	0.3A

Description

This MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- Motor Control
- Power Management Functions

Features

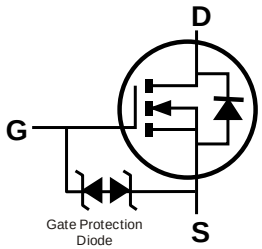
- Dual N-Channel MOSFET
- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Ultra-Small Surface Mount Package
- **ESD Protected Up To 2kV**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

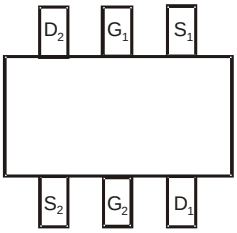
- Case: SOT363
- Case Material: Molded Plastic. "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Matte Tin Finish Annealed over Alloy 42 leadframe (Lead-Free Plating). Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram
- Weight: 0.006 grams (Approximate)

SOT363

Top View



Equivalent Circuit



Top View
Internal Schematic

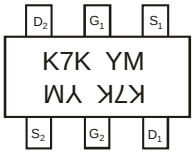
Ordering Information (Note 4)

Part Number	Case	Packaging
DMN601DWK-7	SOT363	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

SOT363



K7K = Product Type Marking Code
YM = Date Code Marking
Y or Y = Year (ex: A = 2013)
M = Month (ex: 9 = September)

Date Code Key

Year	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
Code	S	T	U	V	W	X	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain Source Voltage		V_{DSS}	60	V
Gate-Source Voltage		V_{GSS}	±20	V
Drain Current (Note 5)	Continuous	I_D	305	mA
	Pulsed (Note 6)		800	

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	200	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	625	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-65 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	60	—	—	V	V_{GS} = 0V, I_D = 10μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 60V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.6	2.5	V	V_{DS} = 10V, I_D = 1mA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	— —	2.0 3.0	Ω	V_{GS} = 10V, I_D = 0.5A V_{GS} = 5V, I_D = 0.05A
Forward Transfer Admittance	$\|Y_{fs}\|$	80	—	—	ms	V_{DS} =10V, I_D = 0.2A
Diode Forward Voltage (Note 8)	V_{SD}	0.5	—	1.4	V	V_{GS} = 0V, I_S = 115mA
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	—	50	pF	V_{DS} = 25V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	—	25	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	5.0	pF	

Notes:
5. Device mounted on FR-4 PCB.
6. Pulse width ≤10μS, Duty Cycle ≤1%.
7. Short duration pulse test used to minimize self-heating effect.

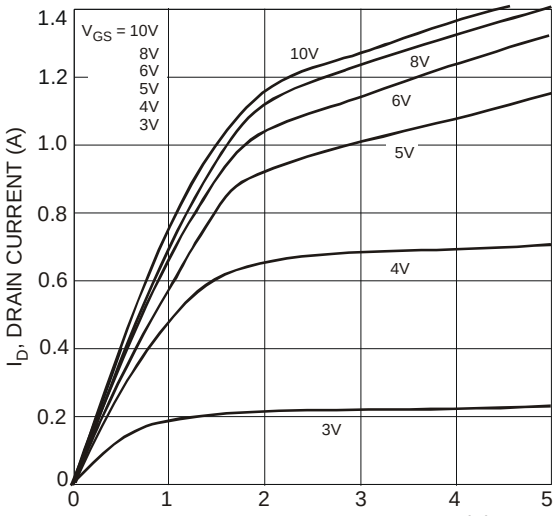


Figure 1 Typical Output Characteristics

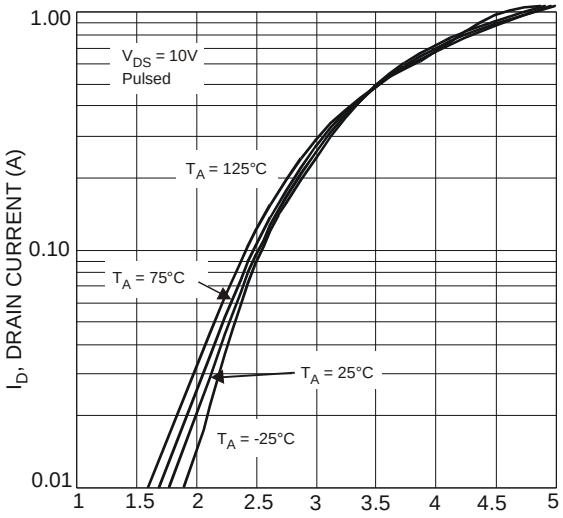


Figure 2 Typical Transfer Characteristics

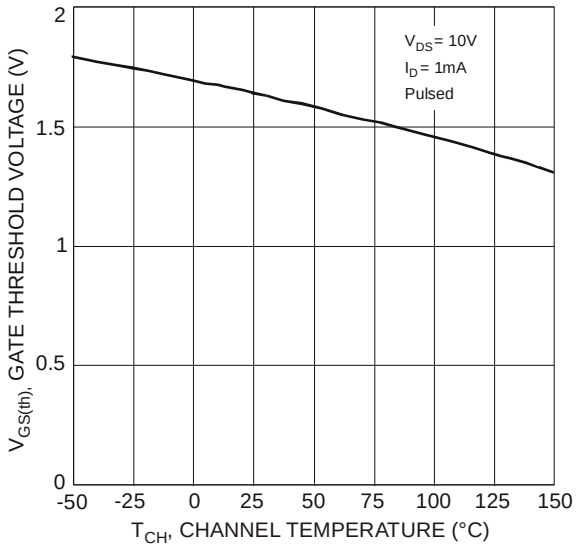


Figure 3 Gate Threshold Voltage vs. Channel Temperature

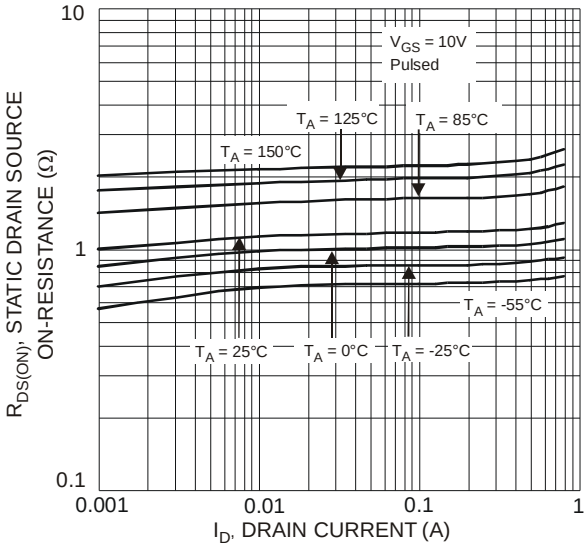


Figure 4 Static Drain-Source On-Resistance vs. Drain Current

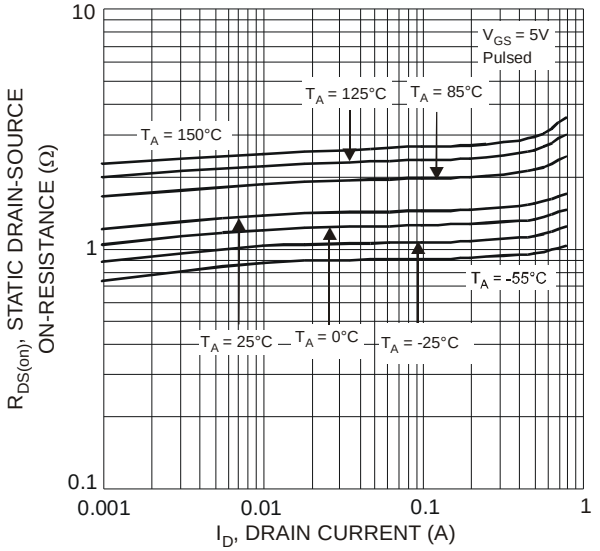


Figure 5 Static Drain-Source On-Resistance vs. Drain Current

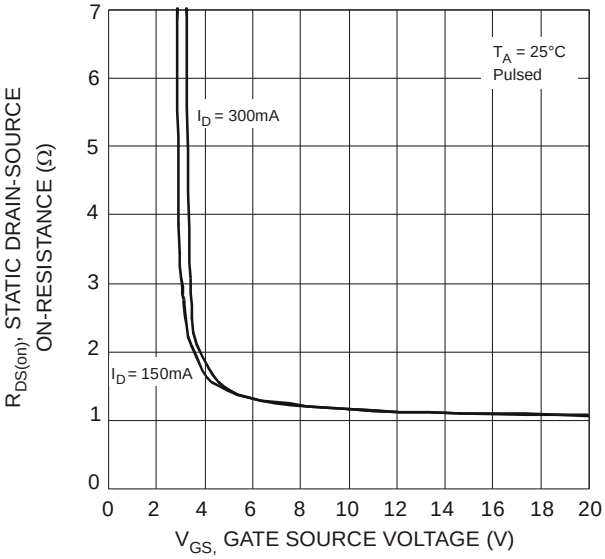


Figure 6 Static Drain-Source On-Resistance vs. Gate-Source Voltage

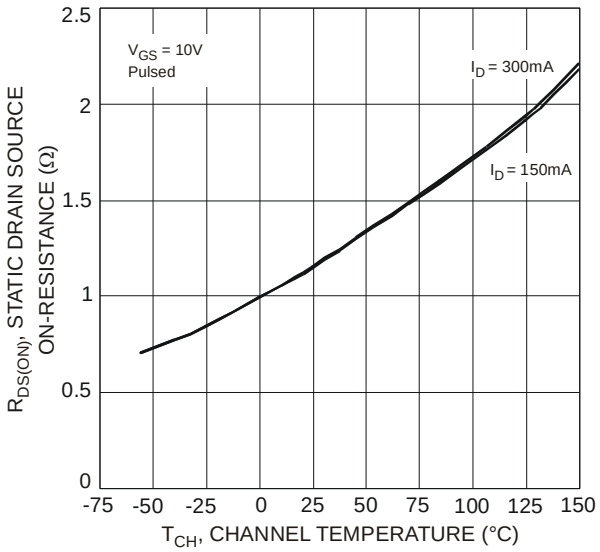


Figure 7 Static Drain-Source On-State Resistance vs. Channel Temperature

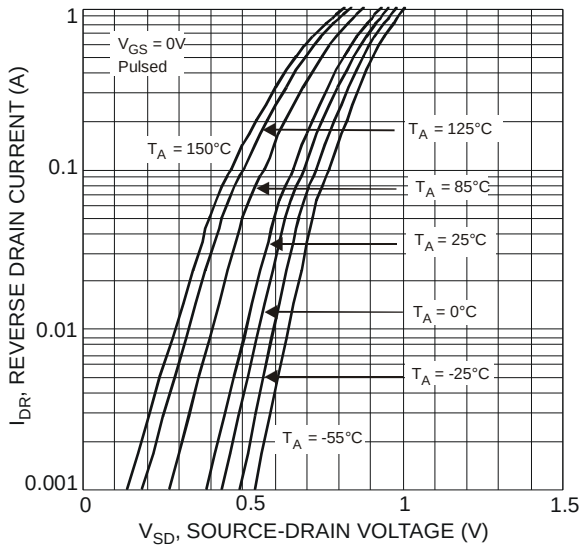


Figure 8 Reverse Drain Current vs. Source-Drain Voltage

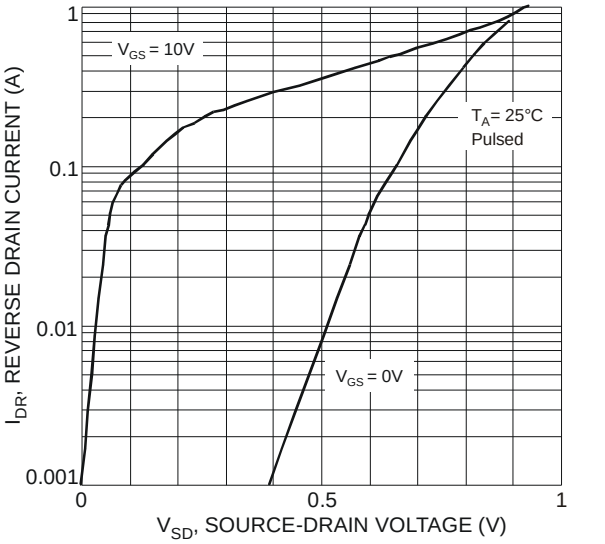


Figure 9 Reverse Drain Current vs. Source-Drain Voltage

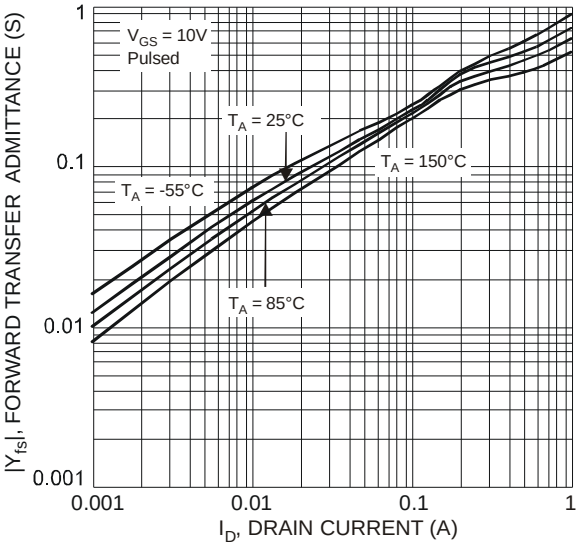


Figure 10 Forward Transfer Admittance vs. Drain Current

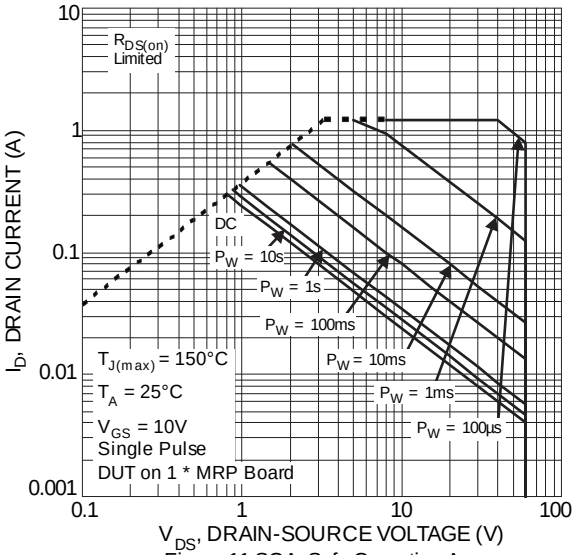
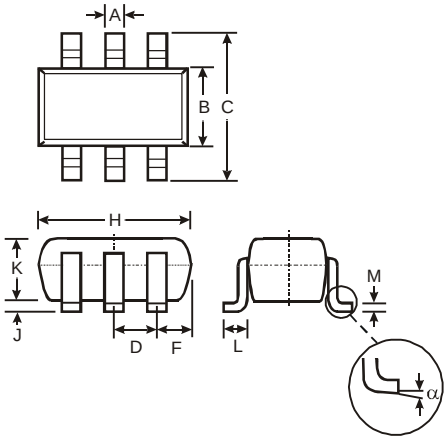


Figure 11 SOA, Safe Operation Area

Package Outline Dimensions

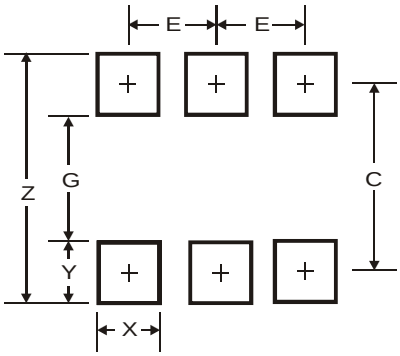
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



SOT363			
Dim	**Min**	**Max**	**Typ**
A	0.10	0.30	0.25
B	1.15	1.35	1.30
C	2.00	2.20	2.10
D	0.65 Typ		
F	0.40	0.45	0.425
H	1.80	2.20	2.15
J	0	0.10	0.05
K	0.90	1.00	1.00
L	0.25	0.40	0.30
M	0.10	0.22	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.5
G	1.3
X	0.42
Y	0.6
C	1.9
E	0.65

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