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Kind regards,

Team Nexperia



# BSS84AKV

50 V, 170 mA dual P-channel Trench MOSFET

Rev. 1 — 19 May 2011

Product data sheet

## 1. Product profile

### 1.1 General description

Dual P-channel enhancement mode Field-Effect Transistor (FET) in an ultra small and flat lead SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 1 kV
- AEC-Q101 qualified

### 1.3 Applications

- Relay driver
- High-speed line driver
- High-side loadswitch
- Switching circuits

### 1.4 Quick reference data

Table 1. Quick reference data

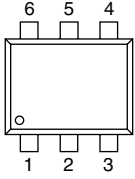
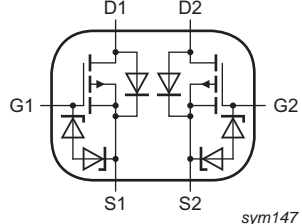
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-50	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-170	mA
<b>Static characteristics (per transistor)</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -100\text{ mA}; T_j = 25\text{ °C}$	-	4.5	7.5	$\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source 1	 <p><b>SOT666 (SOT666)</b></p>	 <p>sym147</p>
2	G1	gate 1		
3	D2	drain 2		
4	S2	source 2		
5	G2	gate 2		
6	D1	drain 1		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BSS84AKV	SOT666	plastic surface-mounted package; 6 leads	SOT666

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code <sup>[1]</sup>
BSS84AKV	EG

[1] % = placeholder for manufacturing site code

## 5. Limiting values

**Table 5. Limiting values**

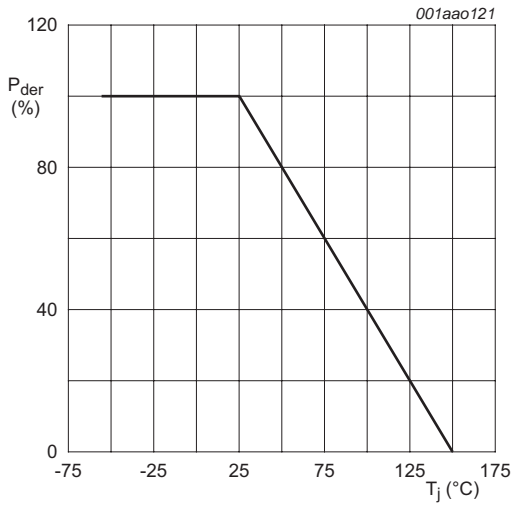
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-50	V	
$V_{GS}$	gate-source voltage		-20	20	V	
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-170	mA
		$V_{GS} = -10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-110	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C};$ single pulse; $t_p \leq 10\text{ }\mu\text{s}$	-	-0.7	A	
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	330	mW
			[1]	-	390	mW
		$T_{sp} = 25\text{ °C}$	-	-	1090	mW
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	500	mW
$T_j$	junction temperature		-55	150	°C	
$T_{amb}$	ambient temperature		-55	150	°C	
$T_{stg}$	storage temperature		-65	150	°C	
<b>Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-170	mA
<b>ESD maximum rating</b>						
$V_{ESD}$	electrostatic discharge voltage	HBM	[3]	-	1000	V

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.

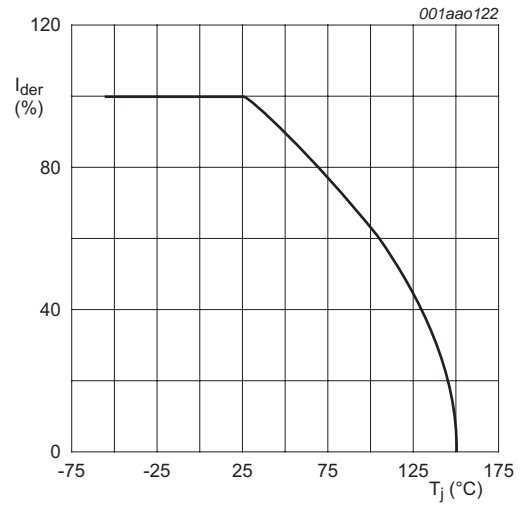
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[3] Measured between all pins.



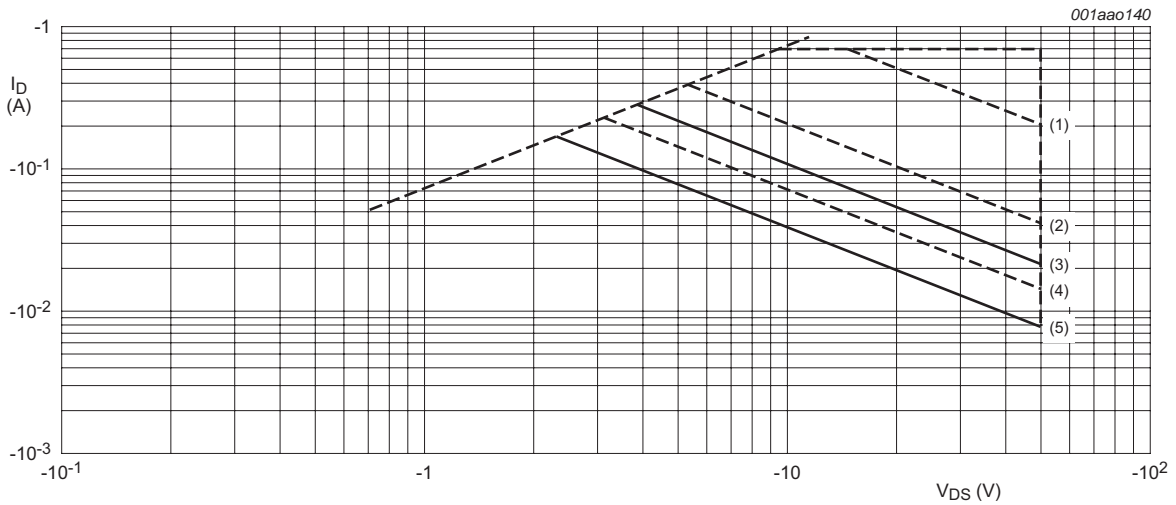
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig. 1. Normalized total power dissipation as a function of junction temperature**



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

**Fig. 2. Normalized continuous drain current as a function of junction temperature**



I<sub>DM</sub> is single pulse

- (1) t<sub>p</sub> = 1 ms
- (2) t<sub>p</sub> = 10 ms
- (3) DC; T<sub>sp</sub> = 25 °C
- (4) t<sub>p</sub> = 100 ms
- (5) DC; T<sub>amb</sub> = 25 °C; drain mounting pad 1 cm<sup>2</sup>

**Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

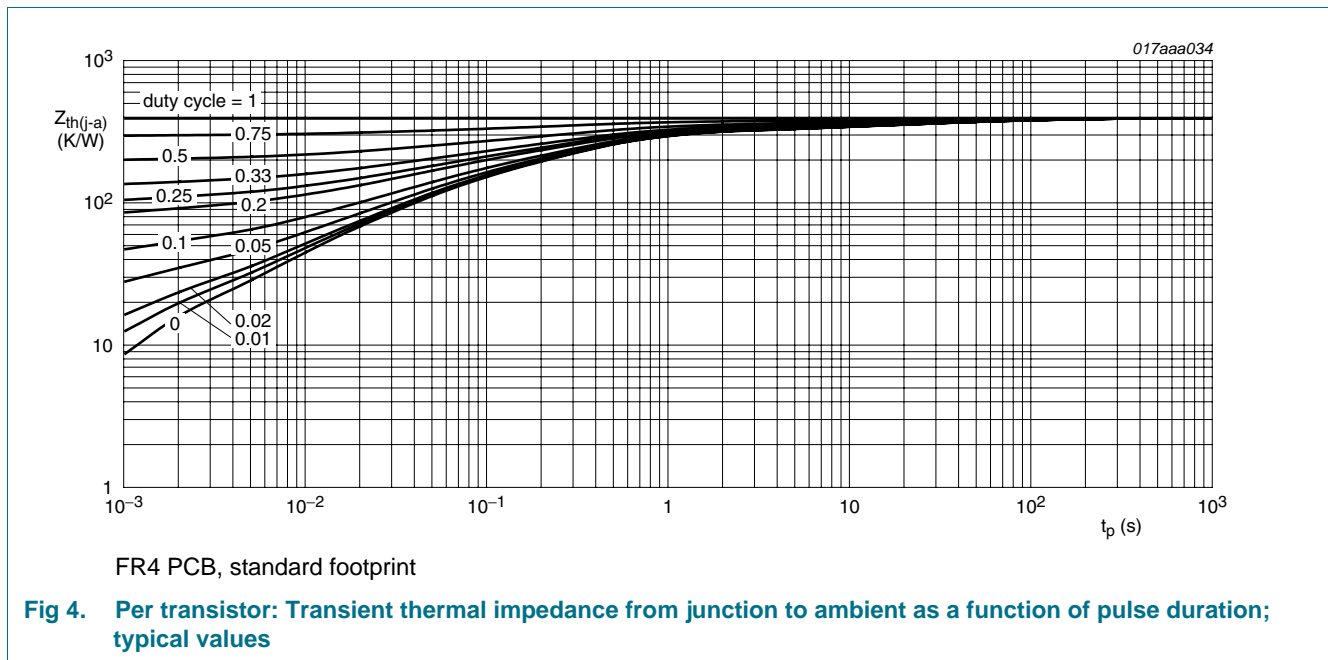
## 6. Thermal characteristics

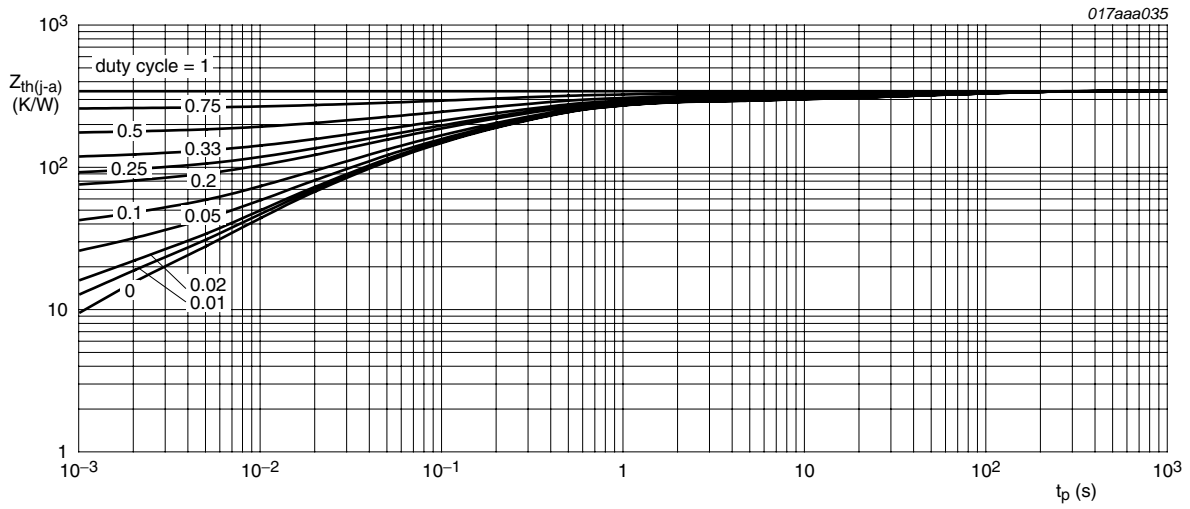
**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per device</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250 K/W
<b>Per transistor</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	330	380 K/W
			[2]	-	280	320 K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	115	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm<sup>2</sup>.





FR4 PCB, mounting pad for drain 1 cm<sup>2</sup>

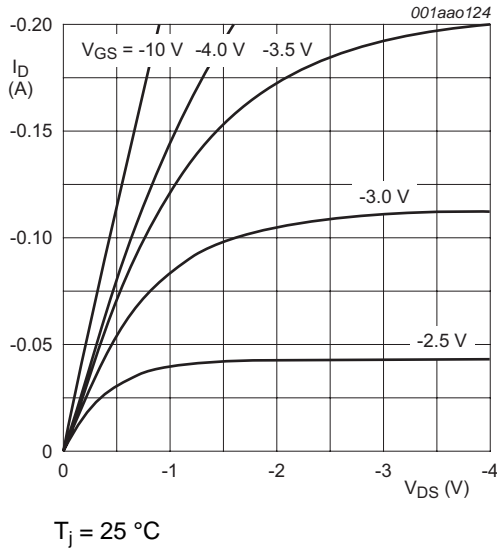
**Fig 5. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 7. Characteristics

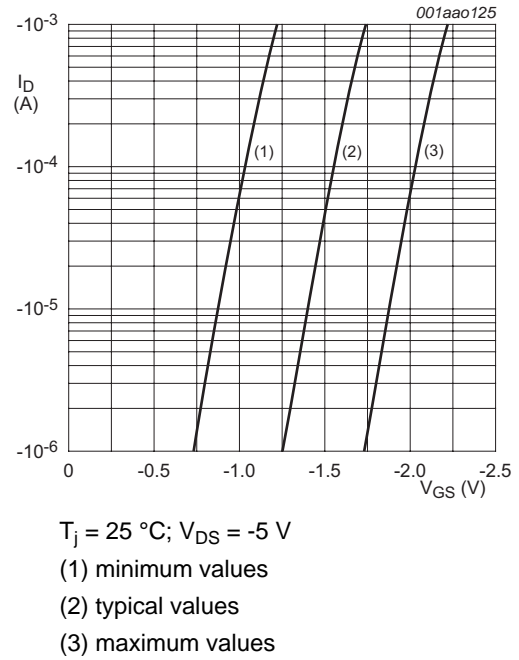
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -10 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-50	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-1.1	-1.6	-2.1	V
$I_{DSS}$	drain leakage current	$V_{DS} = -50 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
		$V_{DS} = -50 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	-2	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
		$V_{GS} = 20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 \text{ V}$ ; $I_D = -100 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	4.5	7.5	$\Omega$
		$V_{GS} = -10 \text{ V}$ ; $I_D = -100 \text{ mA}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	8	13.5	$\Omega$
		$V_{GS} = -5 \text{ V}$ ; $I_D = -100 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	5.7	8.5	$\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -100 \text{ mA}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	150	-	mS
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -25 \text{ V}$ ; $I_D = -200 \text{ mA}$ ; $V_{GS} = -5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.26	0.35	nC
$Q_{GS}$	gate-source charge		-	0.12	-	nC
$Q_{GD}$	gate-drain charge		-	0.09	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -25 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	24	36	pF
$C_{oss}$	output capacitance		-	4.5	-	pF
$C_{rss}$	reverse transfer capacitance		-	1.3	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -30 \text{ V}$ ; $R_L = 250 \Omega$ ; $V_{GS} = -10 \text{ V}$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	13	26	ns
$t_r$	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	48	96	ns
$t_f$	fall time		-	25	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = -115 \text{ mA}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-0.48	-0.85	-1.2	V

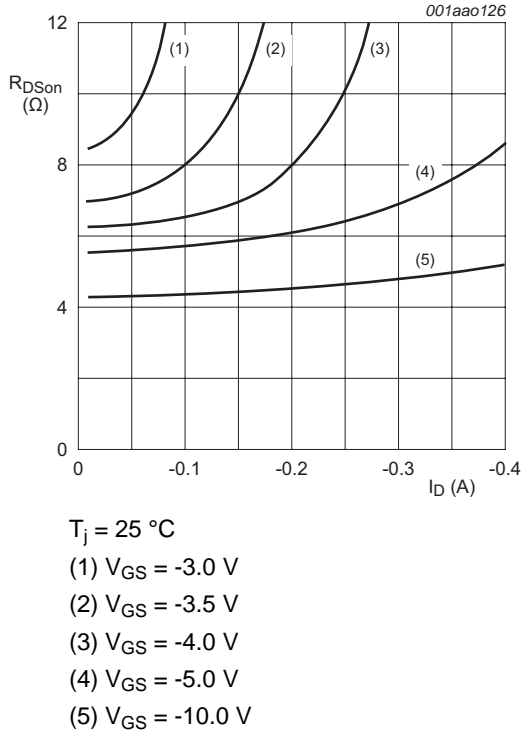




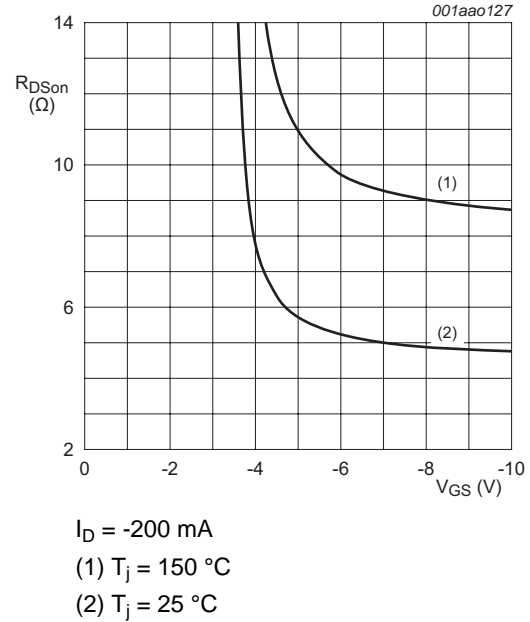
**Fig 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



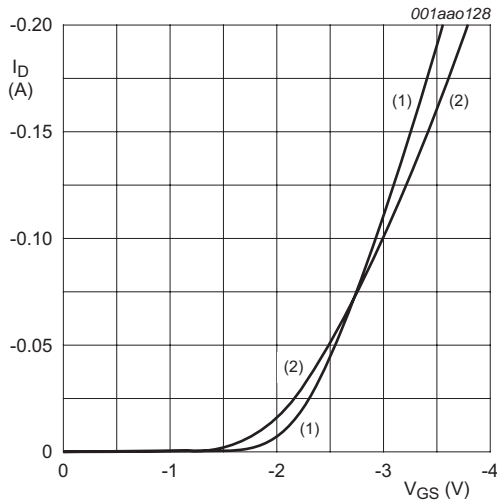
**Fig 7. Sub-threshold drain current as a function of gate-source voltage**



**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**

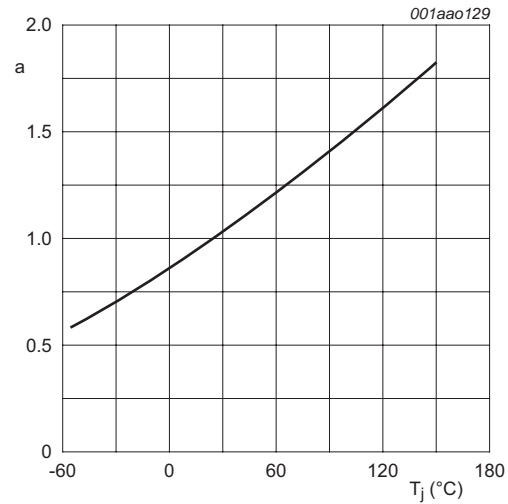


**Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



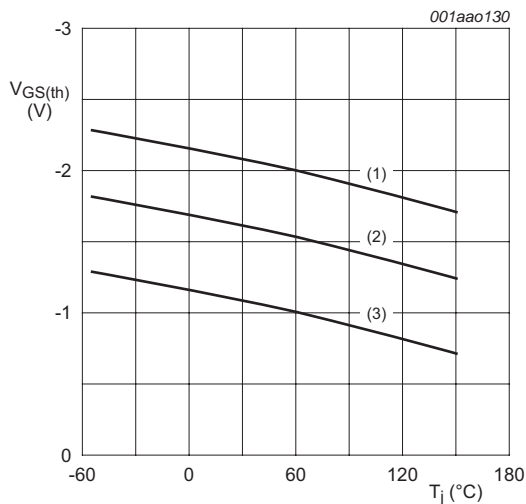
$V_{DS} > I_D \times R_{DSon}$   
 (1)  $T_j = 25\text{ °C}$   
 (2)  $T_j = 150\text{ °C}$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



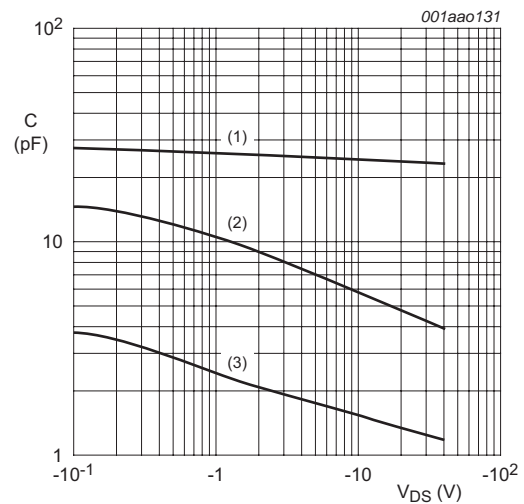
$$a = \frac{R_{DSon}}{R_{DSon(25\text{°C})}}$$

**Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



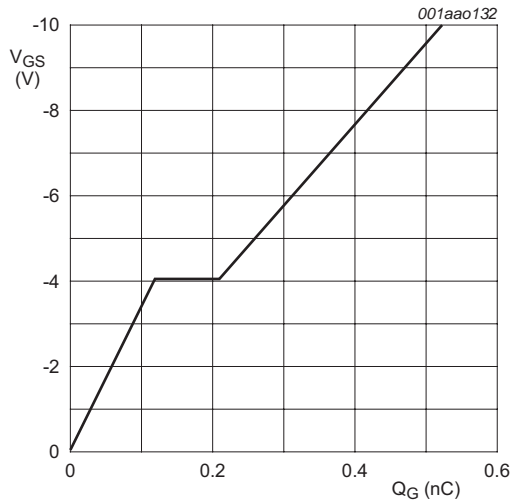
$I_D = -0.25\text{ mA}$ ;  $V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

**Fig 12. Gate-source threshold voltage as a function of junction temperature**



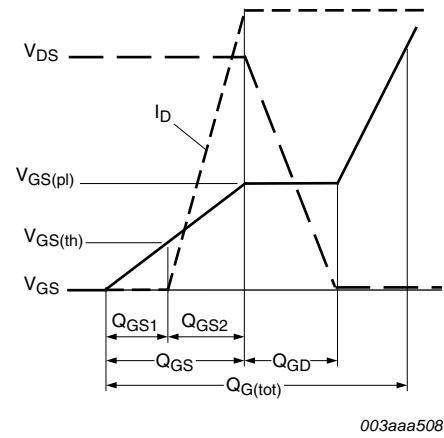
$f = 1\text{ MHz}$ ,  $V_{GS} = 0\text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

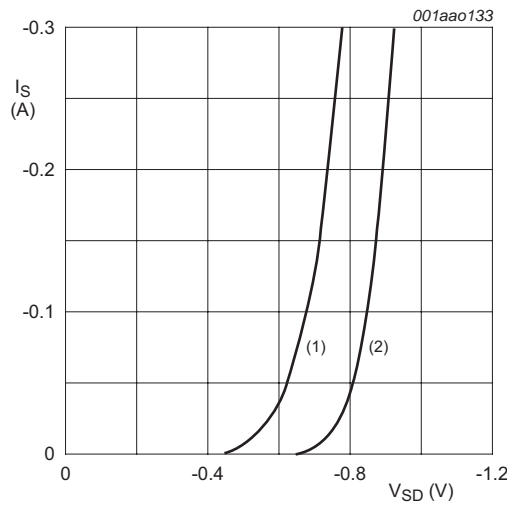


$I_D = -0.2 \text{ A}; V_{DS} = -25 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values**



**Fig 15. Gate charge waveform definitions**



$V_{GS} = 0 \text{ V}$   
 (1)  $T_j = 150 \text{ }^\circ\text{C}$   
 (2)  $T_j = 25 \text{ }^\circ\text{C}$

**Fig 16. Source current as a function of source-drain voltage; typical values**

## 8. Test information

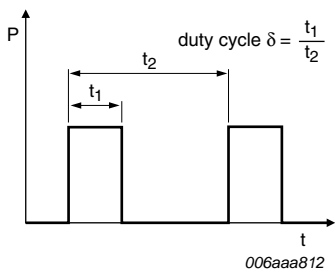


Fig 17. Duty cycle definition

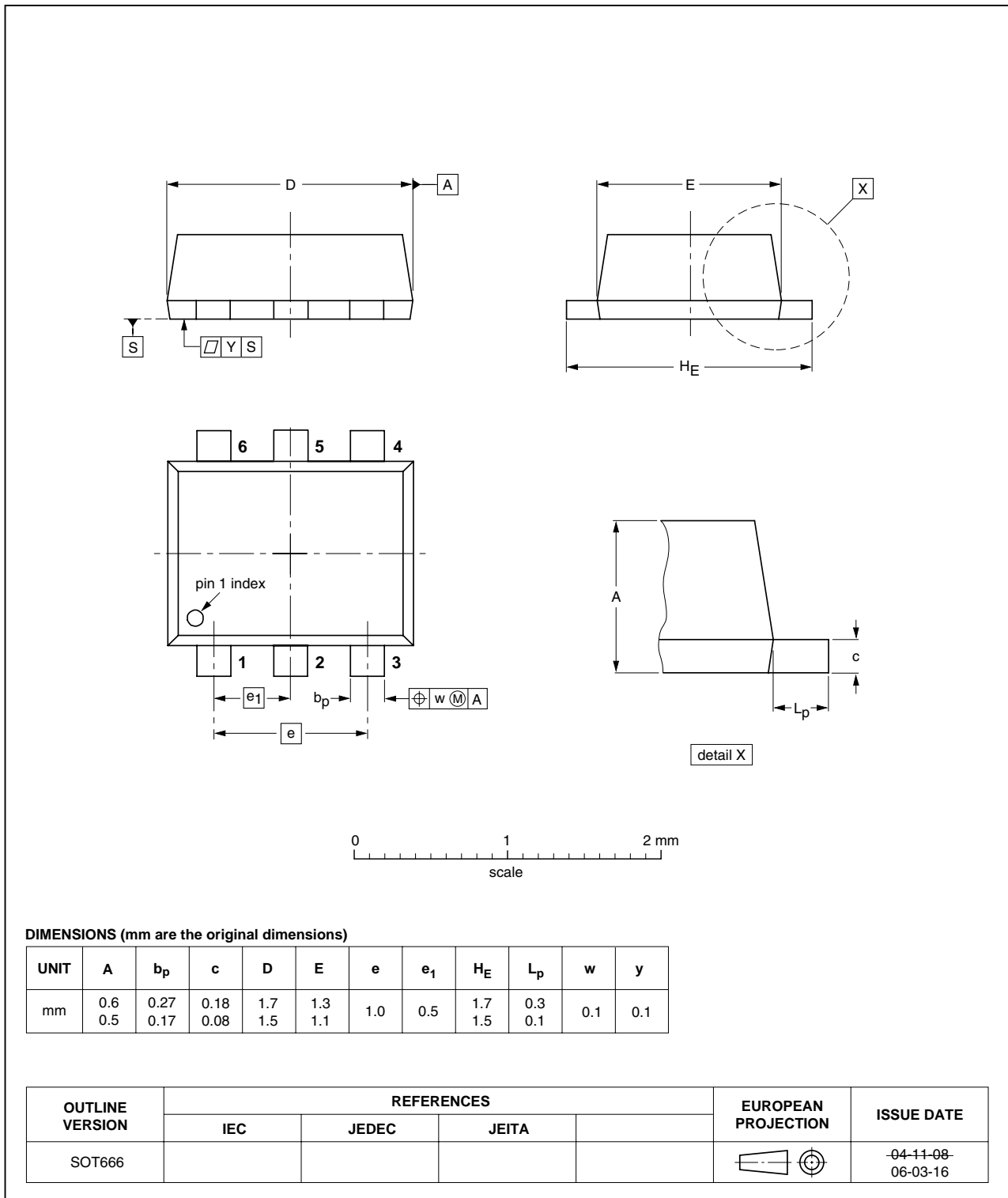
### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

**9. Package outline**

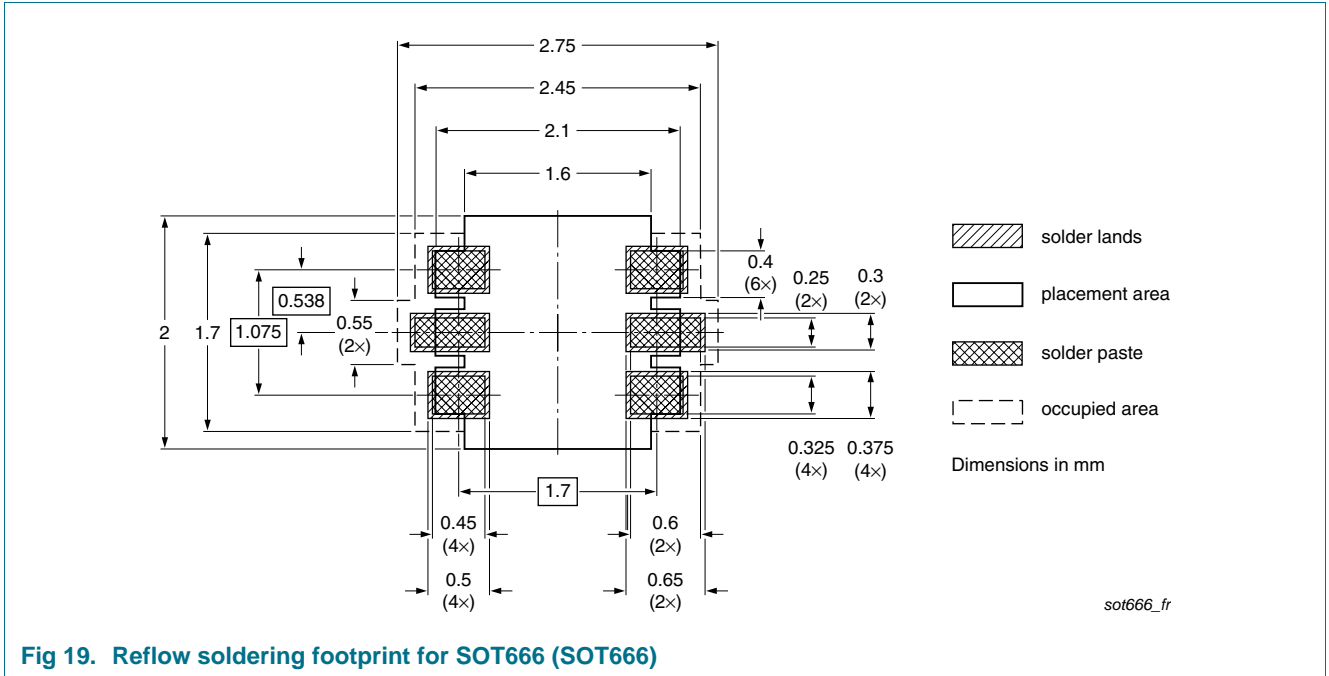
Plastic surface-mounted package; 6 leads

SOT666



**Fig 18. Package outline SOT666 (SOT666)**

**10. Soldering**



**Fig 19. Reflow soldering footprint for SOT666 (SOT666)**

## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BSS84AKV v.1	20110519	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <a href="#">[1]</a> <a href="#">[2]</a>	Product status <a href="#">[3]</a>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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