ALPHA & OMEGA SEMICONDUCTOR

AOTF4185

40V P-Channel MOSFET

General Description

The AOTF4185 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for load switch and battery protection applications.

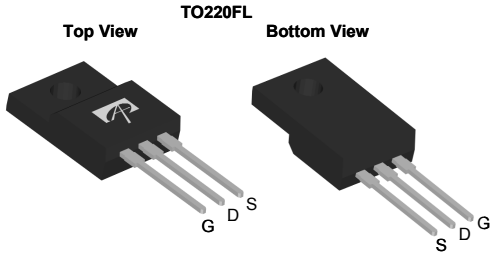
Product Summary

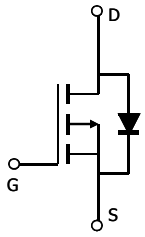
V_{DS}	-40V
I_D (at V_{GS}=10V)	-34A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 16mΩ
$R_{DS(ON)}$ (at V_{GS} = 4.5V)	< 20mΩ

100% UIS Tested
100% R_g Tested

RoHS Compliant

TO220FL





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C=25°C	I_D	-34	A
	T_C=100°C		-27	
Pulsed Drain Current [C]		I_{DM}	-100	
Avalanche Current [C]		I_{AS}, I_{AR}	-42	A
Avalanche energy L=0.1mH [C]		E_{AS}, E_{AR}	88	mJ
Power Dissipation [B]	T_C=25°C	P_D	33	W
	T_C=100°C		16	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A D]	Steady-State		10	13	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	3	4.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D = -250µA, V_{GS} = 0V	-40			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -40V, V_{GS} = 0V			-1	µA
		T_J = 55°C			-5	
I_{GSS}	Gate-Body leakage current	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = -250µA	-1.7	-1.85	-2.5	V
$I_{D(ON)}$	On state drain current	V_{GS} = -10V, V_{DS} = -5V	-120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -10V, I_D = -20A		13	16	mΩ
		T_J=125°C		19	23	
		V_{GS} = -4.5V, I_D = -15A		16	20	
g_{FS}	Forward Transconductance	V_{DS} = -5V, I_D = -20A		50		S
V_{SD}	Diode Forward Voltage	I_S = -1A,V_{GS} = 0V		-0.72	-1	V
I_S	Maximum Body-Diode Continuous Current				-20	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-20V, f=1MHz		2550		pF
C_{oss}	Output Capacitance			280		pF
C_{rss}	Reverse Transfer Capacitance			190		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	2.5	4	6	Ω
SWITCHING PARAMETERS						
Q_g (10V)	Total Gate Charge	V_{GS}=-10V, V_{DS}=-20V, I_D=-20A		42	55	nC
Q_g (4.5V)	Total Gate Charge			18.6		nC
Q_{gs}	Gate Source Charge			7		nC
Q_{gd}	Gate Drain Charge			8.6		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=-10V, V_{DS}=-20V, R_L= 1Ω, R_{GEN}=3Ω		9.4		ns
t_r	Turn-On Rise Time			20		ns
$t_{D(off)}$	Turn-Off DelayTime			55		ns
t_f	Turn-Off Fall Time			30		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=-20A, dI/dt=500A/µs		25	33	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=-20A, dI/dt=500A/µs		75		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25° C.
B. The power dissipation P_D is based on $T_{J(MAX)}$=175° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300 µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175° C.
G. The maximum current rating is limited by bond-wires.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

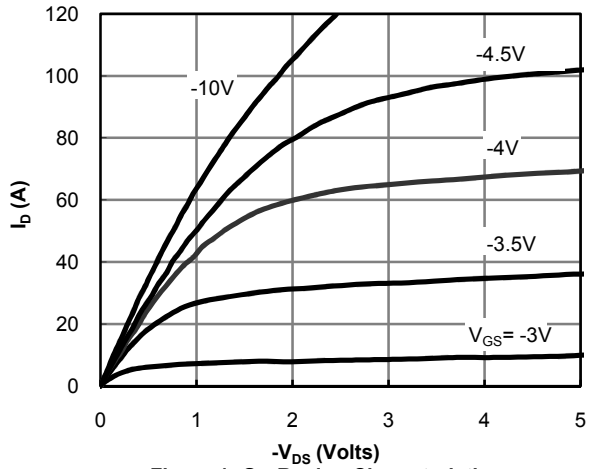


Figure 1: On-Region Characteristics

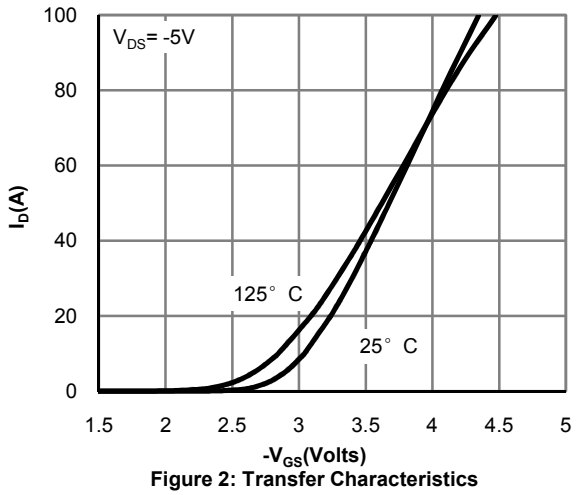


Figure 2: Transfer Characteristics

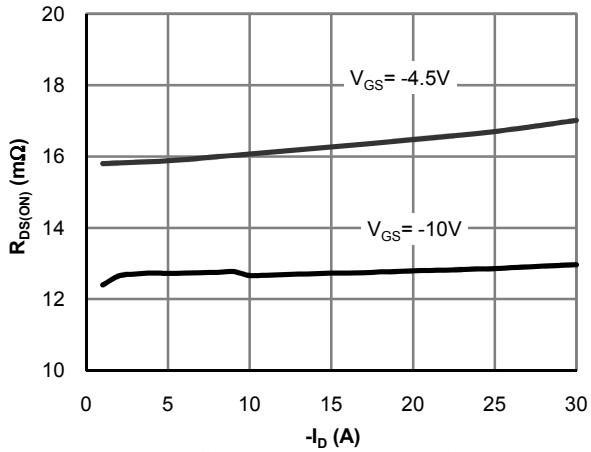


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

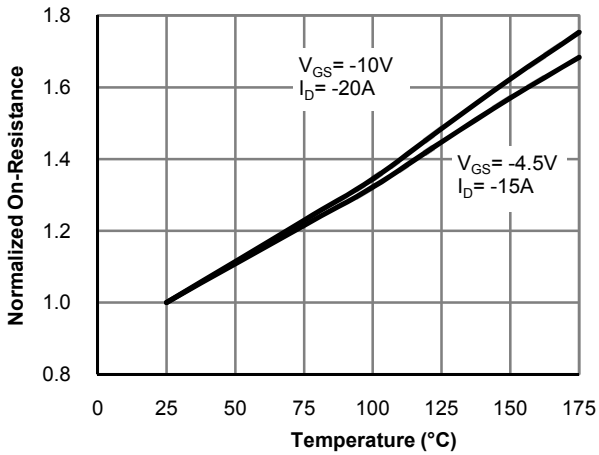


Figure 4: On-Resistance vs. Junction Temperature

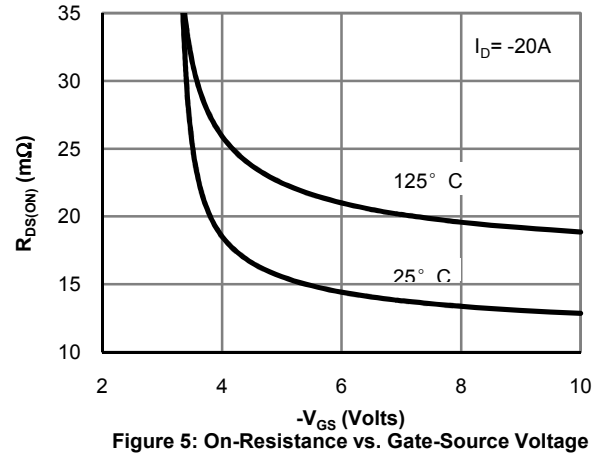


Figure 5: On-Resistance vs. Gate-Source Voltage

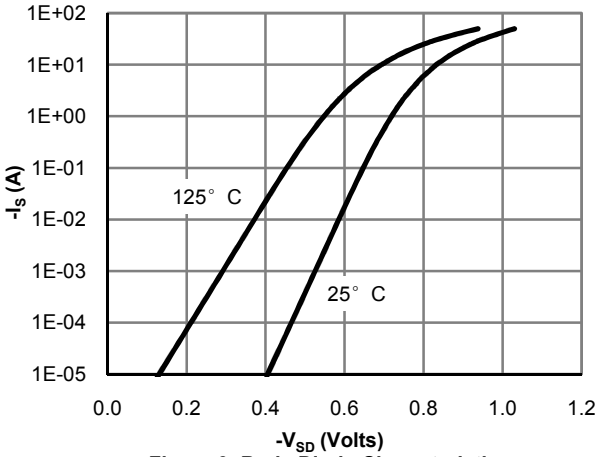


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

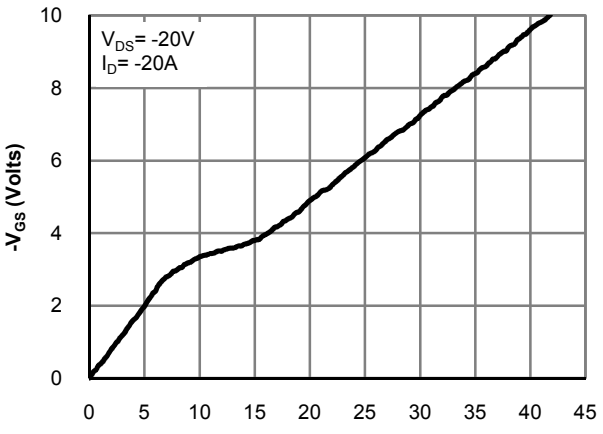


Figure 7: Gate-Charge Characteristics

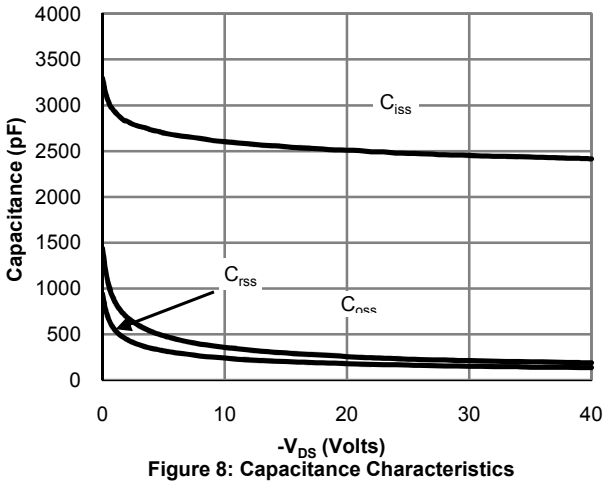


Figure 8: Capacitance Characteristics

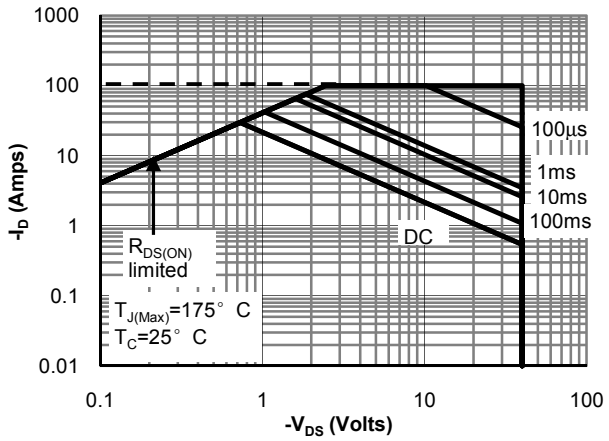


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

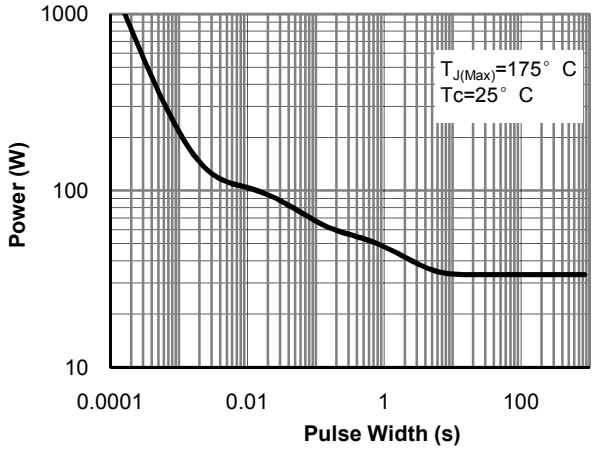


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

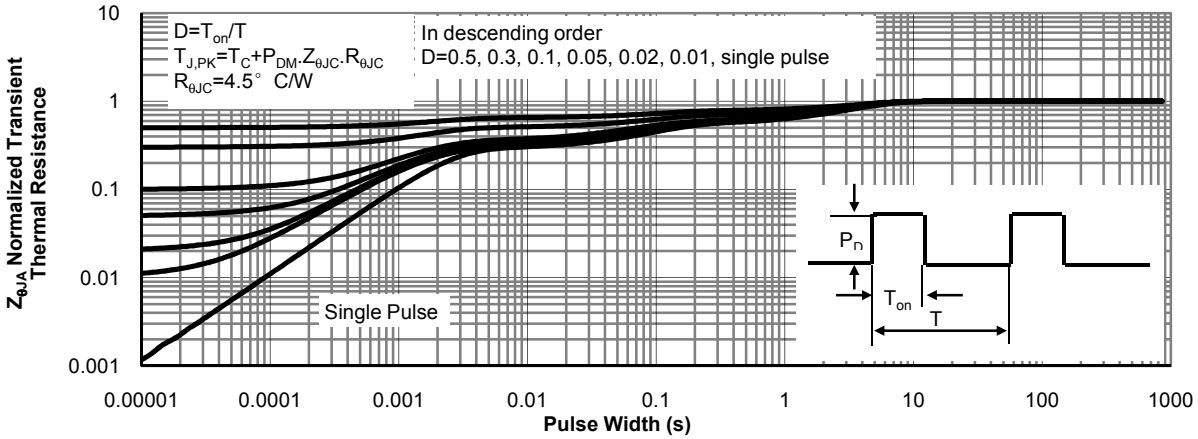


Figure 11: Normalized Maximum Transient Thermal Impedance(Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

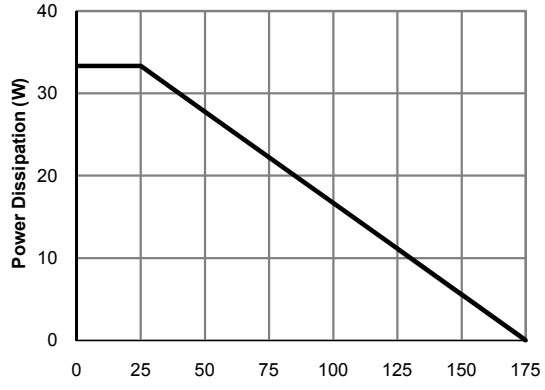


Figure 12: Power De-rating (Note B)

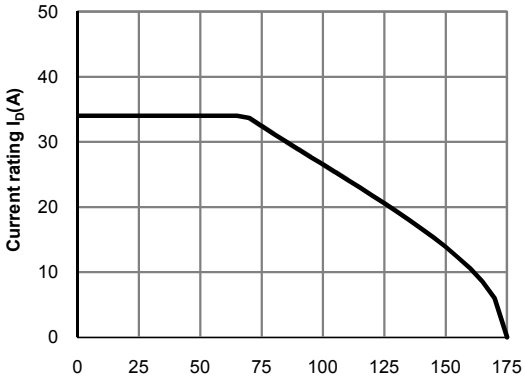


Figure 13: Current De-rating (Note B)

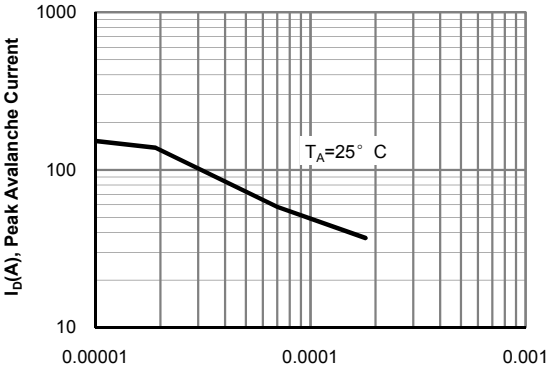
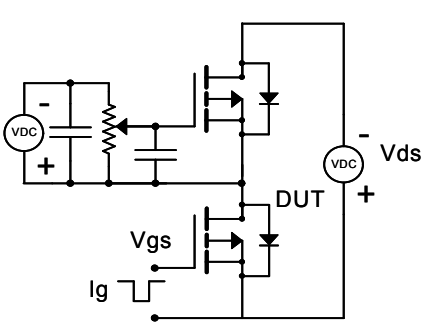
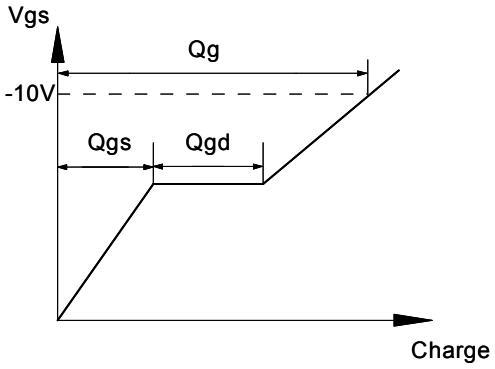


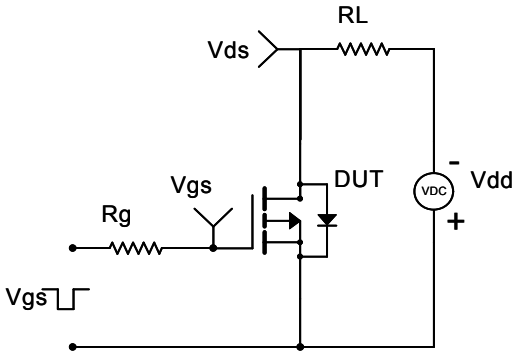
Figure 14: Single Pulse Avalanche capability

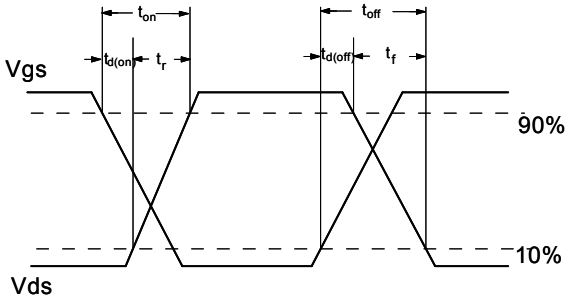
Gate Charge Test Circuit & Waveform



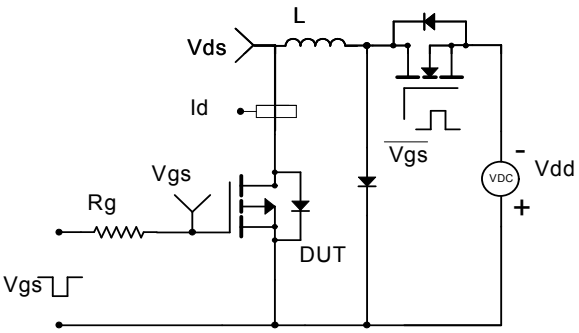


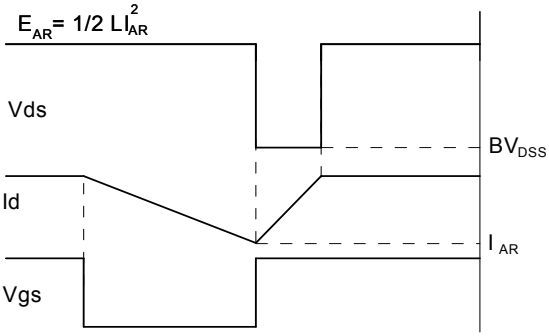
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching (UIS) Test Circuit & Waveforms





Diode Recovery Test Circuit & Waveforms