# QUICK START GUIDE FOR DEMONSTRATION CIRCUIT 998A
## NEGATIVE HOT SWAP CONTROLLER WITH ADC AND I2C MONITORING

## LTC4261CGN

## DESCRIPTION

Demonstration Circuit 998A showcases the LTC®4261 negative Hot Swap controller with ADC and I2C monitoring in a 200W, 36 to 72V application. Included on board is isolation for power good control pins and the single wire interface output. LEDs indicate the presence of -48V input and output, as well as the state of numerous I/O pins. Jumpers allow maximum flexibility in examining the many features of the LTC4261.

The -48V input, RTN and -48V output are separated from each other by at least 55 mils spacing. Input and output connections are made by 93 mil turrets which if removed, accommodate insertion of up to 12 gauge wires for in-situ testing.

**Design files for this circuit board are available. Call the LTC factory.**

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**Table 1. Performance Summary ($T_A$ = 25°C)**

| SYMBOL | PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| | UV ON | | 42.5 | 43 | 43.5 | V |
| -48V | UV OFF | | 37.5 | 38.5 | 39.5 | V |
| INPUT | OV OFF | | | 77 | | V |
| | OV ON | | | 68 | | V |
| $I_{OUT}$, CB | CIRCUIT BREAKER TRIP CURRENT | | 5.5 | 6.25 | 7 | A |

## OPERATING PRINCIPLES

The top of the board contains the components germane to a typical application, along with indicating LEDs, connection turrets, and jumpers to configure various features and I/O pins. The 93-mil turrets are not swaged and may be removed for attachment of up to 12 gauge wire. The board can deliver 200W over the full operating range.

The bottom of the board contains components not associated with the LTC4261 typical application, such as optional I2C bus monitoring, scaling resistors for the A/D inputs, and protection resistors to make the demo circuit more resistant to careless mistakes in a bench-testing environment. Two important components are located on the bottom of the board; bypass capacitors for INTVCC and VIN are placed there to achieve short, direct path.

Clamps on the input and output prevent avalanche in the MOSFET.

### Changing Current Levels

The board may be modified for other current levels. The LTC4261 current sense voltage range is 45 to 55mV, and space is provided for up to three, 1W sense resistors corresponding to a current of about 50A. Copper loss is about 1.2 milliohms, equivalent to about 2 squares of 1-ounce copper; this excludes MOSFET and sense resistor losses.

A clear line of demarcation separates RTN, -48V INPUT, and -48V OUTPUT, with a spacing of at least 55 mils to any adjacent trace. Since the LTC4261 uses a shunt regulated supply, there is no high voltage present across any package pins. DRAIN con-

nects to the output through RD, which serves to block the high voltage sometimes present there. RAMP reaches the output through capacitor, CR. Similarly, RIN1-3 stand off high voltage at RTN.

Although PGIO and PG# are designed to withstand 100V, they lack 55 mil spacing to adjacent package pins. Nevertheless, care has been taken to situate these pins at one corner of the package, and EN# has been placed as a guard to minimize leakage issues into surrounding circuitry. In addition if flashover occurs, PGIO and PG# are used with series resistors (in this case 24 kohms) which limit the flow of current and readily stand off the operating voltage and any transients.

**Jumpers**

DC998A contains 11 jumpers, and a 14-pin connector for I2C interface (discussed later in the I2C Interface section). The jumpers either configure a pin or provide a means for bringing the associated pin out to a turret for external connections. A description of each jumper follows. The purpose of this section is not to replicate the data sheet. For further details refer to that document.

JP10 and JP4, I2C Address ADR0 and ADR1. These jumpers program the I2C address for the board. The address pins ADR0 and ADR1 are 3-state inputs; they can be LOW (VEE), OPEN, or HIGH (INTVCC). The default stuffing is low-low, which corresponds to a device write address of 0010000 (20h). An address of ADR0=low and ADR1=high puts the LTC4261 in Single-Wire Broadcast Mode, and free-running serial data appears at "Single Wire Interface" (connect a separate, 5V supply to power opto U2).

JP8, ON. Selects between forcing the ON pin HIGH (INTVCC), LOW (VEE), or EXT, which passes the pin through to the adjacent ON turret. The default is ON=high, which allows the part to turn on independent of I2C control.

J1, I2C INTERFACE. See separate section covering this topic.

JP7, SDA. The LTC4261 has a split SDA function, appearing as the SDAI (input) and SDAO (output) pins. These two pins facilitate optical isolation. JP7 is initially jumpered in the COM (common) position, which shorts SDAI and SDAO together and allows the board to operate with DC590A. If JP4 is moved to the SPLIT position, these pins are separated.

JP3, INTERFACE. Selects between I2C and SINGLE WIRE interface modes. This jumper moves SDAO between JP3 (I2C) and the HCPL-0300 optical isolator.

JP2, EN#. Connects EN# HIGH (INTVCC, disable), LOW (VEE, enable), or EXT (adjacent turret). Default is low to enable the LTC4261 on power up.

JP5, UV/OV. Connects top of UV and OV dividers to RTN or adjacent SHORT PIN turret. Default is RTN.

JP1, PGIO. PGIO pin has three possible functions; it can be an I2C programmable open collector output, a logic input read by I2C or (the default) a power good output. JP1 gives the choice of connecting PGIO to an opto isolator (OPTO, default jumper position), or to the PGIO turret (EXT).

JP6, PGI#. The LTC4261 monitors a down-stream DC-DC converter by watching for PGI# to go low within a timer interval during power up. If PGI# does not go low, the LTC4261 shuts down. JP6 offers connections to an opto isolator (OPTO) or connects PGI# to VEE (BYPASS). BYPASS is the default jumper position, which ignores the state of the opto isolator.

JP9, ADIN. Moves ADIN between the ADIN turret (EXT) and a divider to the -48V output (default) which measures VDS.

JP11, ADIN2. Moves ADIN2 between the ADIN2 turret (EXT) and the 0V divider (default) which measures the input voltage.

**J1, I2C INTERFACE**

A simple means of exercising the I2C port is provided at J1, to be used in conjunction with a PC and DC590A. DC590A acts as in intermediary between DC998A and a PC, complete with optical isolation. Simply plug in the 14-wide DC590A interface cable to J1. The software is found on the LTC website, www.linear.com. There is a "personality" EEPROM on the bottom of the board which is read by DC590A and used to automatically bring up the correct software. From there all of the LTC4261 registers can be read from or written to, allowing full control over all of the device's features.

If you experience trouble getting the I2C interface running with DC590A, verify the following: JP10=LOW, JP4=LOW, JP7=COM, and JP3=I2C. Of course the following conditions must be met in order for the output to turn on automatically: JP8=LOW and JP5=RTN or SHORT PIN connected to RTN.

To connect an external I2C interface, disconnect DC590A and use J1, or use the SDAO, SDAI and SCL turrets directly. Note that the I2C lines are referred to VEE as a common.

**SINGLE WIRE INTERFACE**

It is possible to operate the LTC4261 autonomously, yet still retain the monitoring functions by placing it in Single-Wire Broadcast Mode. To do this, connect JP3=SINGLE WIRE, disconnect J1, and disconnect any connections to the I2C turrets. Set the I2C ADDRESS jumpers to JP4=HIGH and JP10=LOW.

Next, turn your attention to the fully floating SINGLE WIRE INTERFACE turrets. Connect an outboard 5V supply to the HCPL-0300 opto isolator (+5V, 0V). A serial data stream then appears on the OUTPUT turret, between +5V and 0V.

**Other Turrets**

FLTIN#. This input is available at a turret along the left margin of the board. It is pulled up to INTVCC by a 100 kohm resistor. FLTIN# is really just a logic input that can be read via I2C, and has no other effect on the operation of the LTC4261.

INTVCC. Allows examination of the INTVCC pin. Used as a supply for pullups to PGI#, FLTIN#, EN#, ON, ADR0, ADR1, ALERT#, SDAO, SDAI and SCL. Note that the aforementioned pins are limited to INTVCC+300mV absolute maximum. If INTVCC is loaded, provision must be made to supply this current by increasing the bias to VIN.

VEE (located close to the LTC4261). This is the common reference and substrate for the LTC4261. If, and only if you are using a floating bench supply and floating load, then -48V INPUT can be made "ground" to facilitate testing. In this case VEE serves as a quiet, small signal ground for a scope probe.

VEE (located close to other turrets). These are connected to the LTC4261 VEE pin, and serve as a common reference for the adjacent turrets, such as PGIO, ON, EN#, FLTIN#, ADIN, and ADIN2.

VIN. Allows examination of the VIN pin.

PGI# INPUT. This is the LED side of a MOC207 opto isolator (U4). Connect to the output of a downstream dc-dc converter to detect proper power up. There is a 100 ohm resistor in series with the opto's LED. Move JP6 to OPTO to use this feature.

PG# OUTPUT. This is the phototransistor side of a MOC207 opto isolator (U3). The phototransistor turns on when PG# goes low. The base is floating. Drive to the opto isolator is indicated by adjacent LED D2.

PGIO OUTPUT. This is the phototransistor side of a MOC207 opto isolator. The phototransistor turns on when PGIO goes low. The base is floating. Drive to the opto isolator is indicated by adjacent LED D1. Move JP1 to OPTO to use this feature. If JP1 is placed in the EXT position, the PGIO pin is connected directly to the PGIO turret.

## QUICK START PROCEDURE

1. Connect -48V to -48V INPUT, with the common return connected to RTN. The output is taken at -48V/200W OUTPUT.
2. The LTC4261 can be turned on by either I2C control, or by jumper selection. In either case, EN# (JP2 or the adjacent turret) must be low before the LTC4261 will turn on. Autonomous operation is accomplished by setting ON (JP8) high, EN# (JP2) low, and then pulling UV/OV (JP5) to RTN. The condition of JP1, JP3, JP4, JP6, JP7, JP9, JP10 and JP11 just don't matter as far as turn-on is concerned. If PGI# is not pulled low before the timeout interval, the LTC4261 will power up briefly and then shut down. Place JP6 in the BYPASS position to avoid this behavior.
3. To control the LTC4261 through $I^2C$, install the QuickEval™ System software on a computer with an available USB port. The download website is http://www.linear.com/software. Connect DC590A between the computer and DC998A, and open the QuickEval software. If already installed, update the software to obtain the LTC4261/DC998A driver.

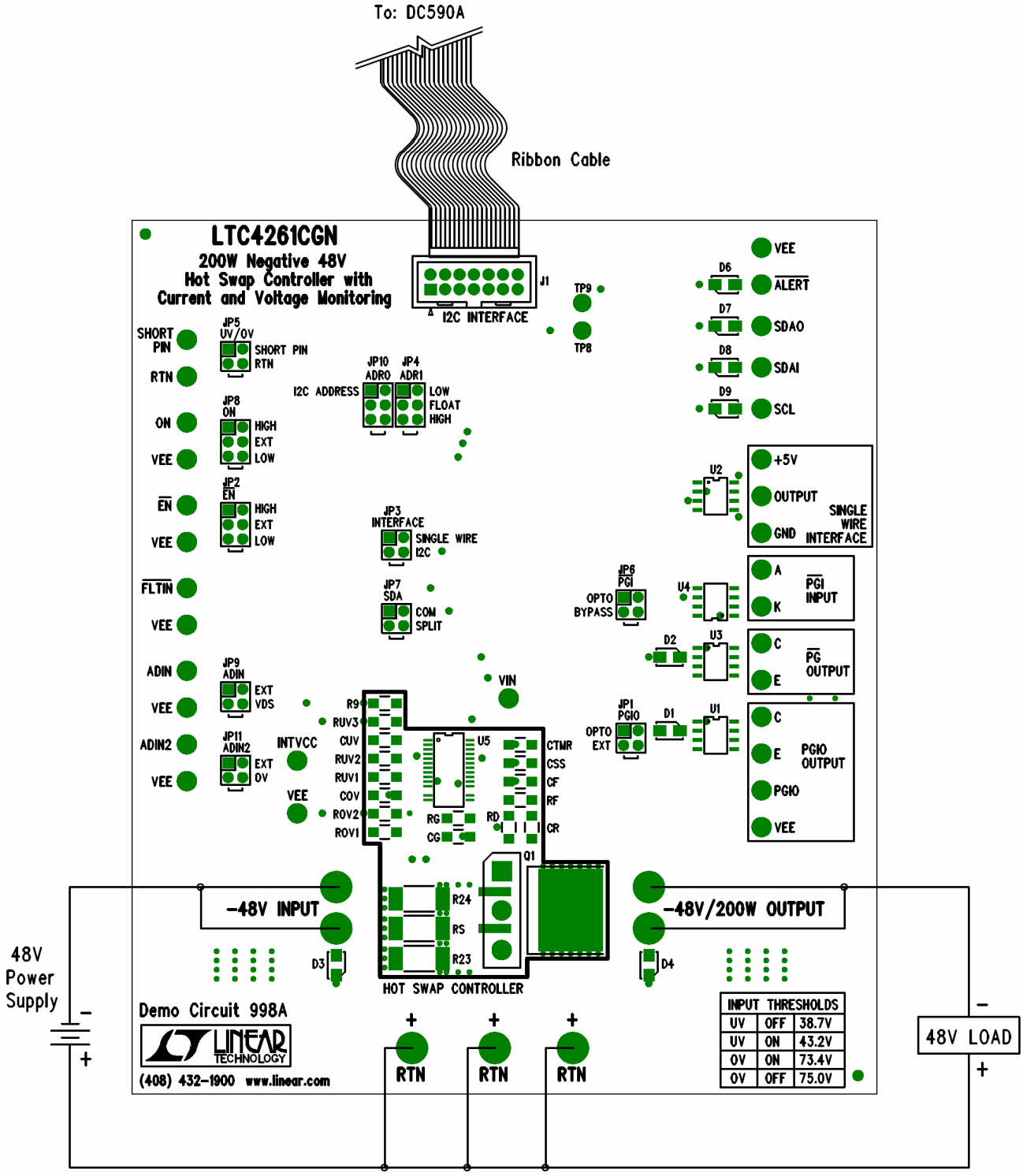
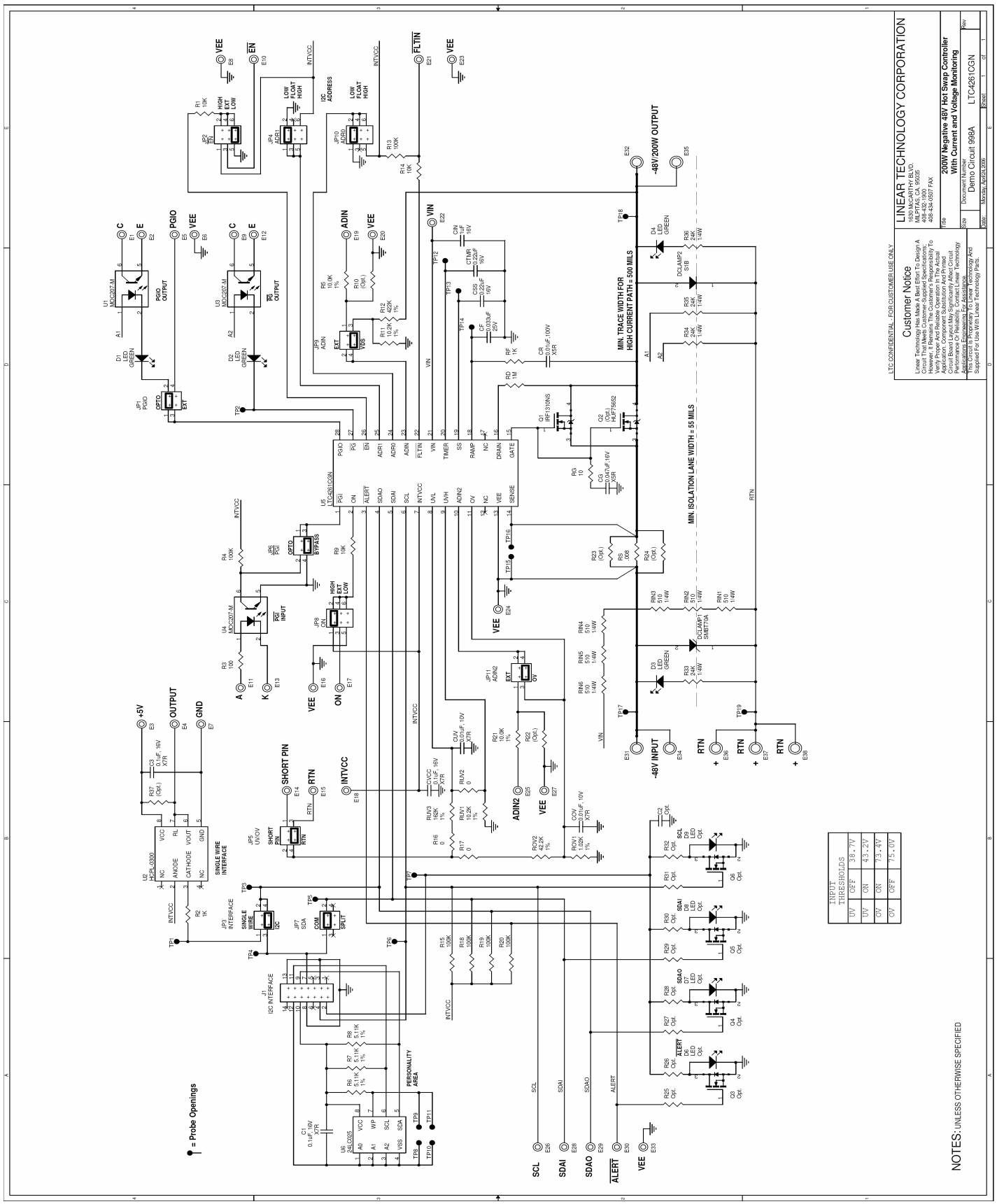



**Figure 1. Proper Measurement Equipment Setup**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200W Negative 48V Hot Swap Controller With Current and Voltage Monitoring
Size
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LTC4261CGN
Rev
Date:
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Sheet 1 of 1
-48V/200W OUTPUT
-48V INPUT
MIN. TRACE WIDTH FOR HIGH CURRENT PATH = 500 MILS
MIN. ISOLATION LANE WIDTH = 55 MILS
INPUT THRESHOLDS
UV OFF 38.7V
UV ON 43.2V
OV ON 73.4V
OV OFF 75.0V
= Probe Openings
NOTES: UNLESS OTHERWISE SPECIFIED