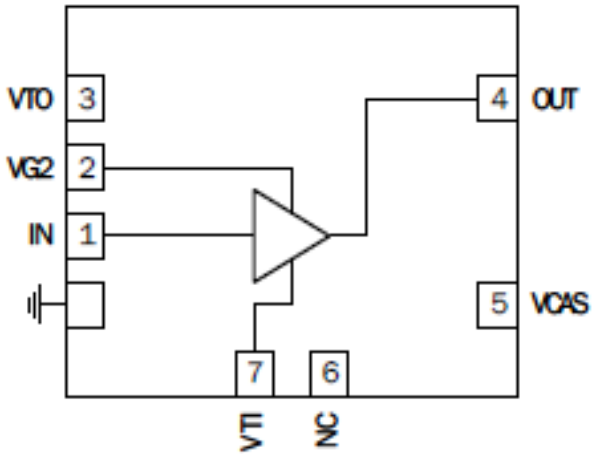
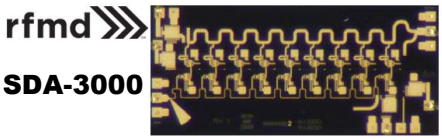
SDA-3000

GaAs Distributed Amplifier

RFMD's SDA-3000 is a directly coupled (DC) GaAs microwave monolithic integrated circuit (MMIC) driver amplifier die designed for use as a Mach Zehnder Modulated (MZM) laser driver employing single-ended (SE) architectures with V_{Π} (V-pi) ranging from 4V to 7V, clock driver for return-to-zero (RZ) and carrier select (CS) Carver Modulators, broadband automated test equipment (ATE), instrumentation, military, and aerospace applications.



Functional Block Diagram



Package: Die, 3.10mm x 1.45mm x 0.102mm

Features

- DC to 24GHz Operation
- +25dBm P_{3dB}
- Gain = 16dB Typical
- Noise Figure = 2.1dB at 10GHz
- Output Voltage to $7V_{PP}$
- Single Supply Voltage
- 160mA Total Current

Applications

- Driver for Single-ended (SE) MZM, NRZ, DPSK, ODB, RZ
- Clock Driver for RZ and CS Pulse Carver
- Broadband ATE
- Instrumentation
- Military
- Aerospace

Ordering Information

SDA-3000	GaAs Distributed Amplifier, GelPak, 10 pieces or more
SDA-3000SB	GaAs Distributed Amplifier, GelPak, 2 pieces

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421

For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Bias Voltage (V_{DD})	+9.0	V_{DC}
Gate Bias Voltage (V_{TI})	-2 to +0	V_{DC}
Gate Bias Voltage (V_{G2})	(V_{DD}-8.0) V_{DC} to V_{DD}	V
RF Input Power (V_{DD} = +8.0V_{DC})	15	dBm
Operating Channel Temperature (T_J)	+175	°C
Continuous Power Dissipation (T = +85°C)	1.7	W
Thermal Resistance (Pad to Die Bottom)	50	°C/W
Storage Temperature	-40 to +150	°C
Operating Temperature	-40 to +85	°C
ESD JESD22-A114 Human Body Model (HBM)	Class 0 (All Pads)	

Caution! ESD sensitive device.

RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, <1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony solder.

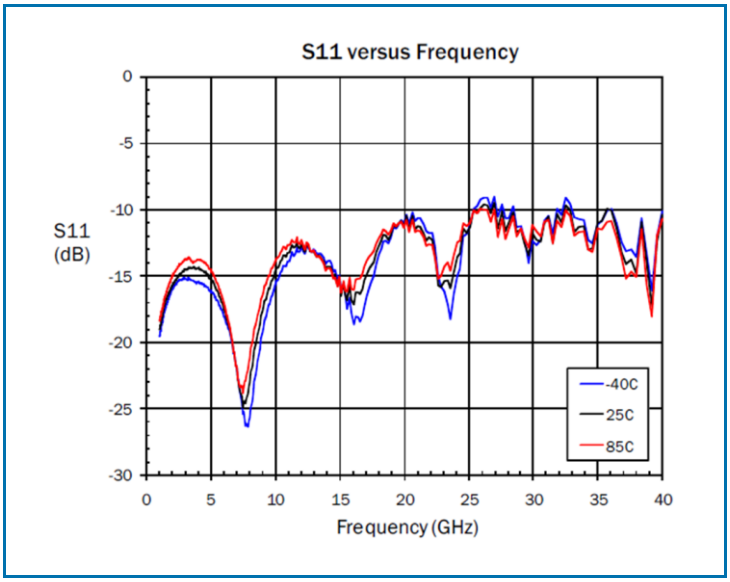
Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

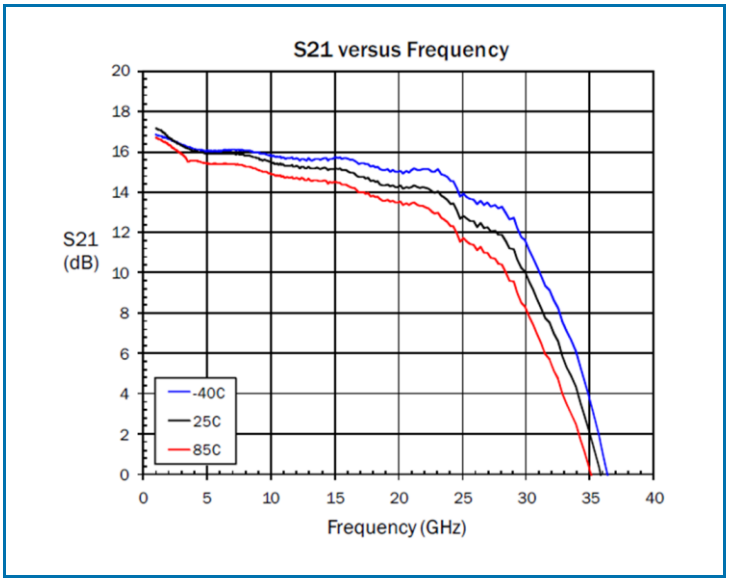
Nominal Operating Parameters

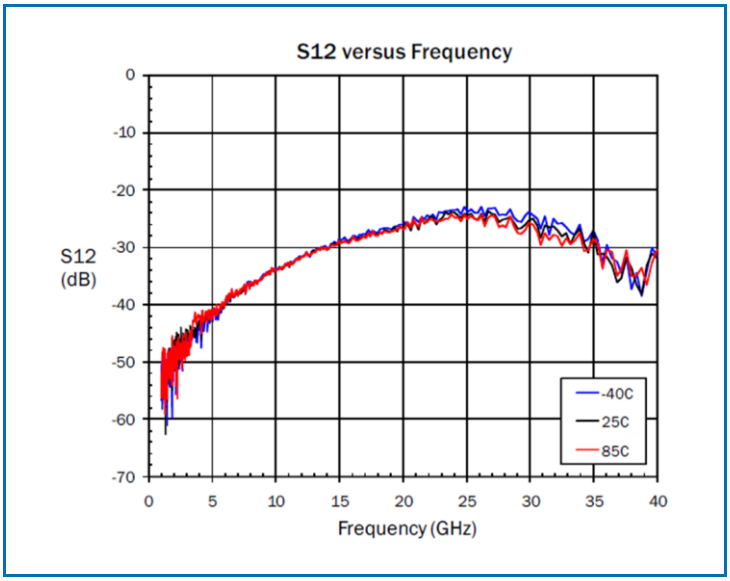
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Performance					**T_A = +25°C, V_{DD} = +8V_{DC}, V_{G2} = +3.5V_{DC}, I_{DD} = 160mA***
Operating Frequency	0		24	GHz	3dB BW
Gain	15.8	16.8		dB	10GHz
Output Voltage		8		V_{P-P}	
IP3 at 10GHz		32		dBm	P_{OUT} +10dBm
P1dB		23		dBm	10GHz
P_{3dB}		25		dBm	10GHz
Noise Figure at Mid-Band		2.1		dB	10GHz
Input Return Loss		12		dB	
Output Return Loss		15			
Supply Current		160		mA	
Supply Voltage		8		V_{DC}	

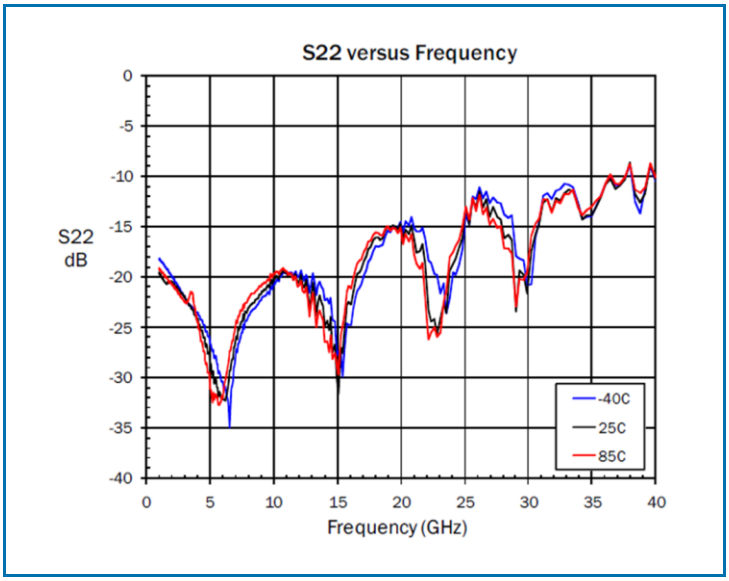
*Adjust VTI between -1.5V_{DC} to +0.2V_{DC} to achieve I_{DD} = 160mA typical., V_{G2} = 3.5V_{DC}

Typical Performance

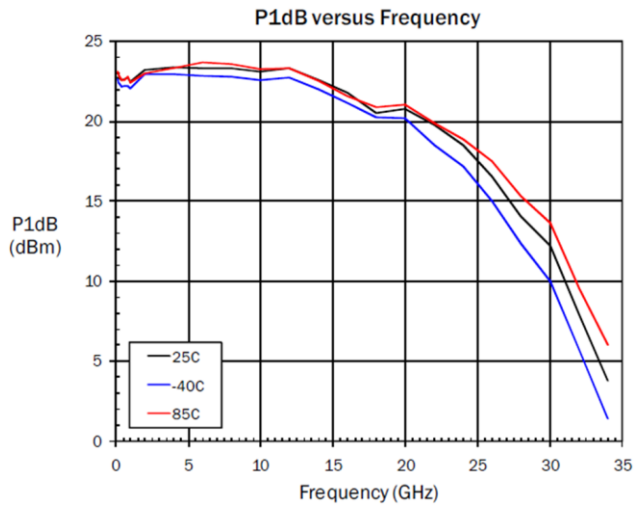


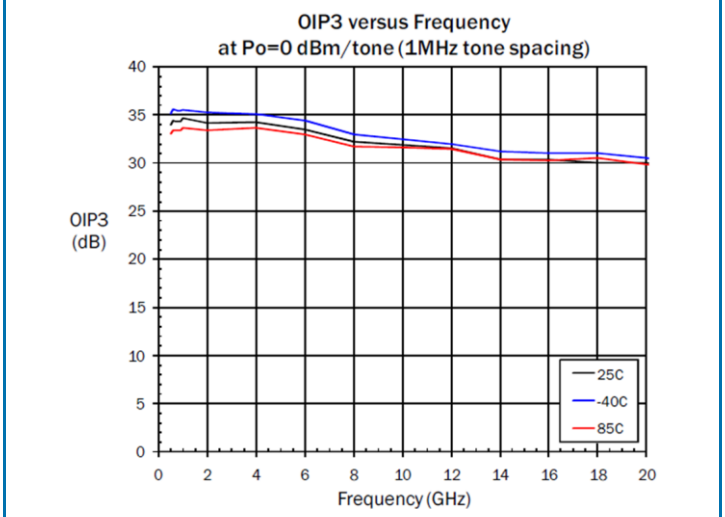


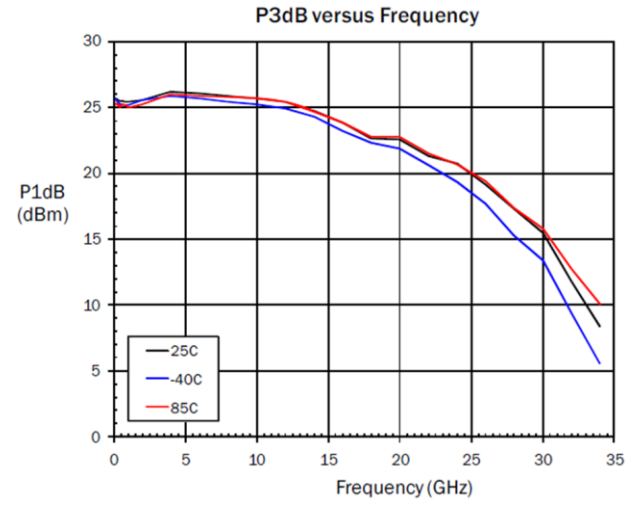


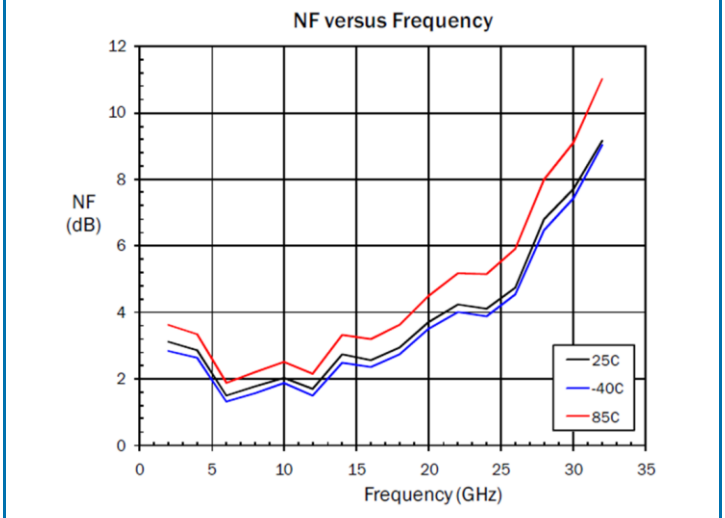


Typical Performance (Continued)

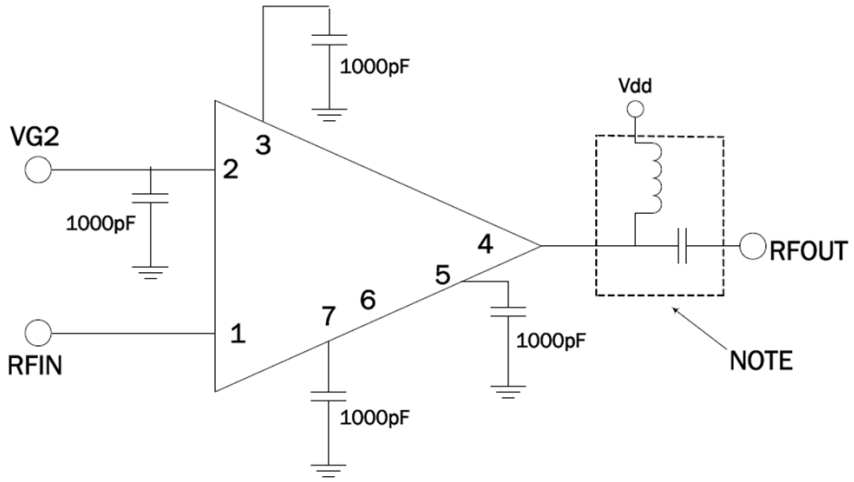






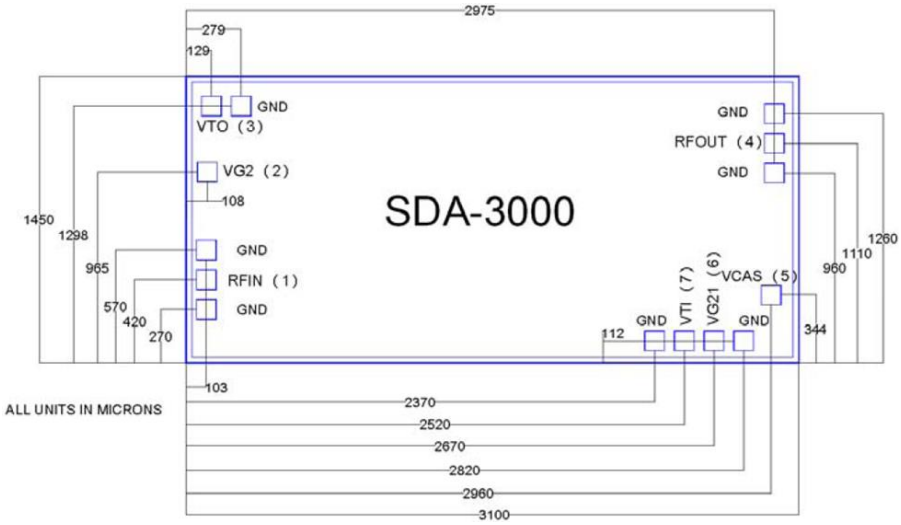


Application Schematic



NOTE: Drain Bias (V_{DD}) must be applied through a broadband bias tee or external bias network.

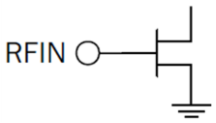
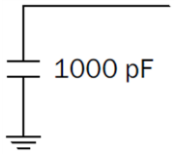
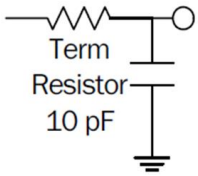
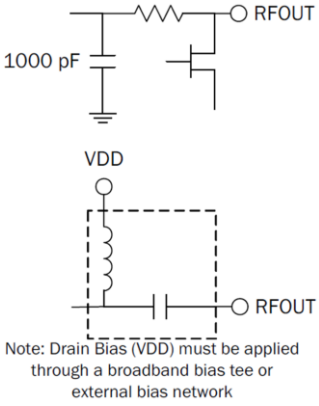
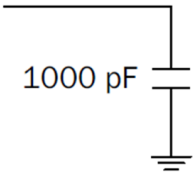
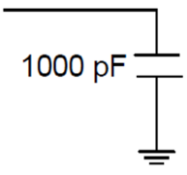
Die Drawing (Dimensions in millimeters)



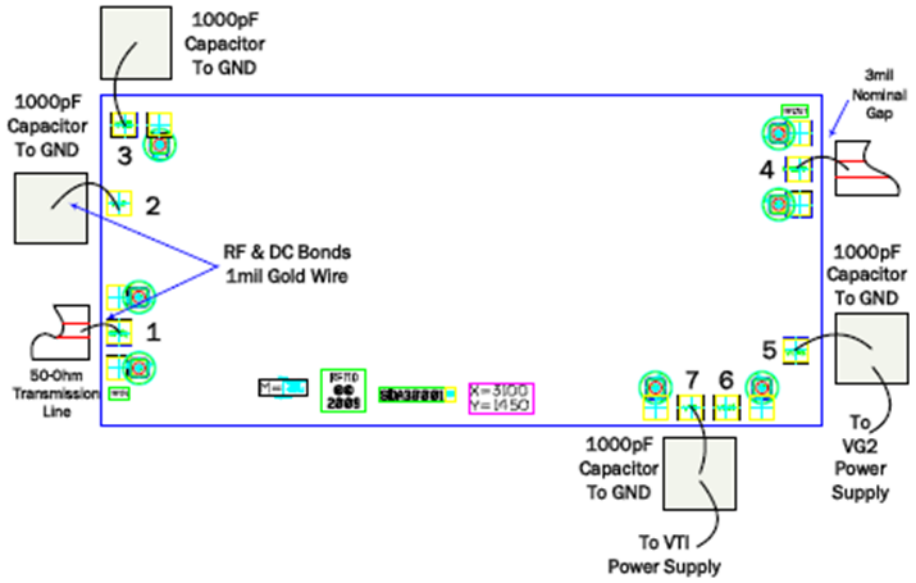
Notes:

1. No connection required for unlabeled bond pads
2. Die thickness is 0.102mm (4mil)
3. Typical bond pad is 0.100mm square
4. Backside metallization: gold
5. Backside metal is ground
6. Bond pad metallization: gold
7. Refer to drawing posted at www.rfmd.com for tolerances

Pin Names and Descriptions

Pin	Name	Description	Interface Schematic
1	RFIN	RF Input. This pad is DC coupled and matched to 50Ω from DC to 24GHz. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output.	
2	VG2	VG2 is an optional pad. It may be used to bias the cascode gate of the amplifier. If this port is used, a 1000pF bypass capacitor with the shortest wirebond length possible is recommended to prevent low frequency gain ripple.	
3	VTO	The output drain termination pad. This pad requires a suggested 1000pF bypass capacitor with the shortest wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	
4	RFOUT and VDD	RF Output. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output. Connect the DC bias (V_{DD}) network to provide drain current (I_{DD}).	
5	VCAS	Provides VG2 gate voltage to the cascode amplifier. The value is ~ (V_{CC}/2 – absolute value of VTI).	
6	VG21	Not connected.	
7	VTI	Input gate voltage, used to bias the amplifier. The value is between -1.5V_{DC} (device is pinched OFF) to +0.2V_{DC} (fully ON). This pad requires a bypass capacitor to ground with the shortest possible wirebond length to prevent low frequency gain ripple. The value of the external capacitance limits the low frequency response of the amplifier.	
Die	GND	Ground connection. Connect die bottom directly to ground plane for best performance. NOTE: The die should be connected directly to the ground plane with conductive epoxy.	

Assembly Diagram



Measurement Technique

All specifications and typical performances reported in this document were measured in the following manner. Data was taken using a temperature controlled probe station utilizing 150µm pitch GSG probes. The interface between the probes and integrated circuit was made with a coplanar to microstrip ceramic test interface. The test interface was then wire bonded to the die as shown in the figure below using 1 mil diameter bondwires. The spacing between the test interface and the die was 200µm, and the bond wire loop height was 100µm. The thickness of the test interface is 125µm (5mil). The calibration of the test fixture included the probes and test interfaces, so that the measurement reference plane was at the point of bond wire attachment. Therefore, all data represents the integrated circuit and accompanying bond wires.