MX852EB0027

Ultra-Low Jitter XTAL Oscillator with Fanout

ClockWorks® FUSION

General Description

MX852EB0027 CMIC™ (clock management IC) is a member of the ClockWorks® FUSION family of devices that integrates the crystal, synthesizer and fanout buffers in a single 5mm x 7mm LGA Package.

Integrating the entire clock chain delivers 200fs typical phase noise performance including fanout and crosstalk.

The device operates from a 2.5V or 3.3V power supply.

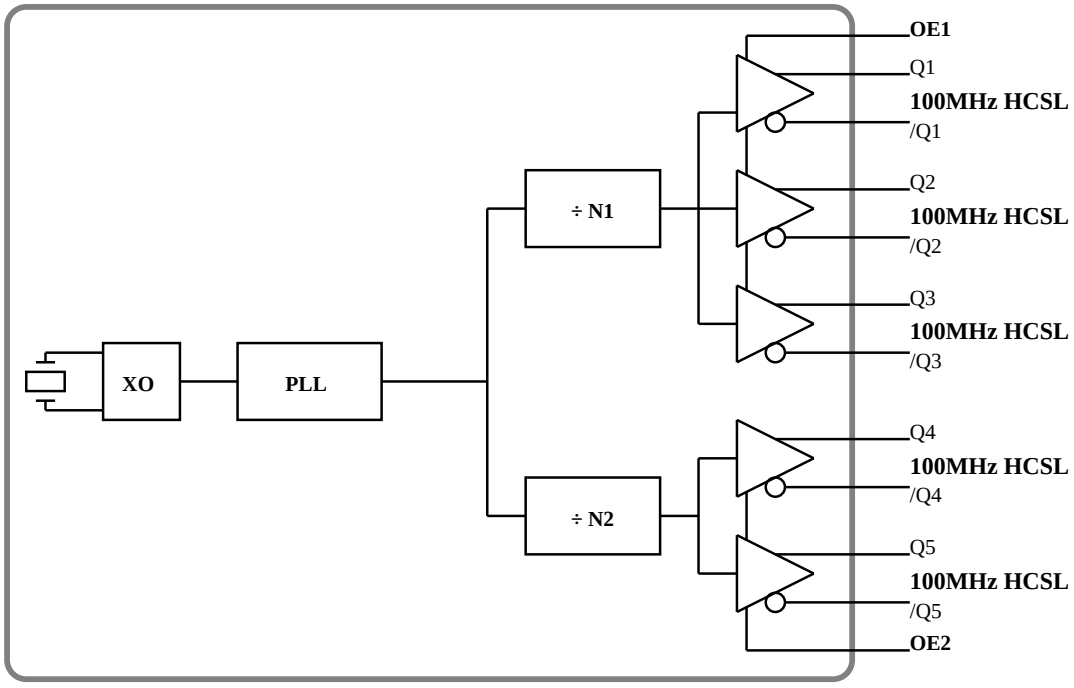
Applications

- PCI-Express
- Storage

Features

- Generates 5 output clocks
- Frequency and output logic:
  -100MHz HCSL x 5
- Integrated quartz crystal for frequency reference
- Typical phase noise:
  -100fs (Integration range: 1.875MHz-20MHz)
  -200fs (Integration range: 12kHz-20MHz)
- Complete ultra-low jitter clocking solution
- OE on banks 1 and 2
- 2.5V or 3.3V operating voltage range
- ±50ppm total stability
- -40°C to +85°C temperature range
- 38-Pin 5mm x 7mm LGA package

Block Diagram



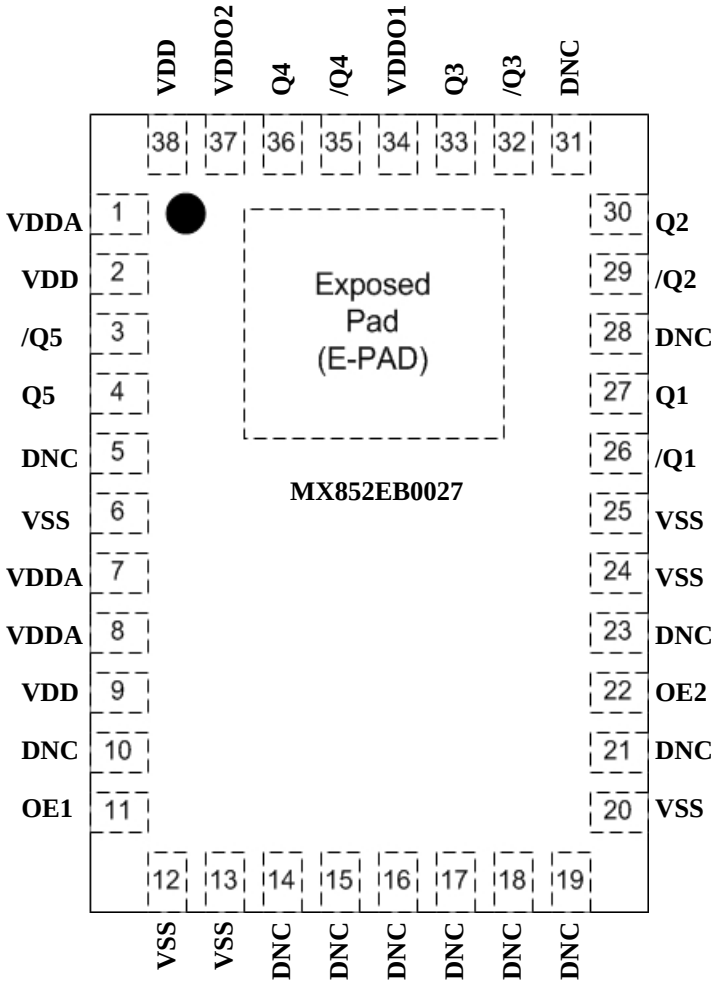
Micrel Inc. • 2180 Fortune Drive • San Jose, CA 95131 • USA • tel +1 (408) 944-0800 • fax + 1 (408) 474-1000 • http://www.micrel.com

Ordering Information

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX852EB0027	MX852E	B0027	Tube	38-Pin 5mm x 7mm LGA
MX852EB0027 TR	MX852E	B0027	Tape and Reel	38-Pin 5mm x 7mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

Pin Configuration



38-Pin 5mm x 7mm LGA

Pin Description

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1, 7, 8	VDDA	PWR		Analog Power Supply
2, 9, 38	VDD	PWR		Power Supply
3, 4	/Q5, Q5	O, Diff	HCSL	Bank 2 Clock Output Frequency = 100MHz
5, 14, 15, 16, 17 18, 19, 21, 23, 28, 31	DNC			Do not connect anything to these pins.
6, 24, 25 EPAD	VSS (Exposed Pad)	PWR		Power Supply Ground. The exposed pad must be connected to the VSS ground plane.
10	DNC			Do not connect
11	OE1	I, SE	LVCMOS	Output Enable, Bank 1 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45k Ohms Pull-Up
12, 13, 20	VSS	PWR		Crystal Ground
22	OE2	I, SE	LVCMOS	Output Enable, Bank 2 outputs disable to tri-state, 0 = Disabled, 1 = Enabled, 45k Ohms Pull-Up
26, 27	/Q1, Q1	O, Diff	HCSL	Bank 1 Clock Output Frequency = 100MHz
29, 30	/Q2, Q2	O, Diff	HCSL	Bank 1 Clock Output Frequency = 100MHz
32, 33	/Q3, Q3	O, Diff	HCSL	Bank 1 Clock Output Frequency = 100MHz
34	VDDO1	PWR		Power Supply for the Outputs on Bank 1
35, 36	/Q4, Q4	O, Diff	HCSL	Bank 2 Clock Output Frequency = 100MHz
37	VDD02	PWR		Power Supply for the Outputs on Bank 2

Absolute Maximum Ratings[1]

Supply Voltage (VDDA, VDD, VDDOx).....+4.6V
Input Voltage (VIN).....-0.5V to VDD + 0.5V
Lead Temperature (soldering, 20s).....260°C
Storage Temperature (T_S).....-65°C to +150°C

Operating Ratings[2]

Supply Voltage (VDDOx, VDD, VDDA)
.....+2.375V to +3.465V
Ambient Temperature (TA).....-40°C to +85°C
Junction Thermal Resistance
LGA (T_{JA}) Still Air.....38.5°C/W

Electrical Characteristics[3]

VDD = VDDA = VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
VDD = VDDA = 3.3V ±5%, VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VDDX	2.5V Operating Voltage 3.3V Operating Voltage		2.375 3.135	2.5 3.3	2.625 3.465	V
IDD	Core Supply Current	Outputs not loaded			204.0	mA
FO	Output Frequency	Bank 1 and 2		100		MHz
Fstability	Frequency Stability	Note 4. Frequency stability over temperature Total stability			±20 ±50	ppm
Tstart	Start-Up Time				20	ms
Tskew	Output-to-Output Skew	Note 5			50	ps
TR/TF	Output Rise/Fall time	20% - 80% HCSL ouput	150	300	450	ps
ODC	Output Duty Cycle	<350MHz output frequencies	48	50	52	%
Tjit(Ø)	RMS Phase Noise	100MHz HCSL Integration range (12kHz-20MHz) Integration range (1.5MHz-20MHz) Integration range (12kHz-40MHz)		 254 118 260		fs
	Period Jitter	Pk-Pk (E5001A, 100Hz-40MHz) RMS (E5001A, 100Hz-40MHz) PK-PK (10K Samples, DSA80000B)		1.6 135 5	 10	ps fs ps

LVCMOS Inputs DC Electrical Characteristics (OE1, OE2)[3]

VDD = 3.3V ±5% or 2.5V ±5%, TA = -40°C to +85°C

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VIH	Input High Voltage		2		VDD + 0.3	V
VIL	Input Low Voltage		-0.3		0.8	V
IIH	Input High Current	VDD = VIN = 3.465V			150	µA
IIL	Input Low Current	VDD = 3.465V, VIN = 0V	-150			µA

Notes:
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The datasheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. The circuit is designed to meet the AC and DC specifications shown in the Electrical Characteristics table after thermal equilibrium has been established.
4. Inclusive of temperature drift, aging, initial accuracy, shock, and vibration. Operating temperature range dependent on part number configuration.
5. Skew between output buffers. Measured at the output differential crossing points. Applies to outputs at the same supply voltage using same output format.

HCSL DC Electrical Characteristics[3]

VDD = VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
VDD = 3.3V ±5%, VDDO1 = VDDO2 = 3.3V ±5% or 2.5V ±5%
TA = -40°C to +85°C, RL = 50 Ohms to VSS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
VOH	Output High Voltage		660	700	850	mV
VOL	Output Low Voltage		-150	0	27	mV
Vcross	Crossing Point Voltage		250	350	550	mV

Application Information

Output Traces

Design the traces for the output signals according to the output logic requirements. If LVCMOS is unterminated, add a 30 Ohms resistor in series with the output, as close as possible to the output pin and start a 50 Ohms trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50 Ohms traces.

For EMI reasons, it is better to use a balanced differential design.

LVDS can be AC coupled or DC coupled to its termination.

Power Supply Decoupling

Place the smallest value decoupling capacitor (4.7nF below) between the VDD and VSS pins, as close as possible to those pins and at the same side of the PCB as the IC. The shorter the physical path from VDD to capacitor and back from capacitor to VSS, the more effective the decoupling.

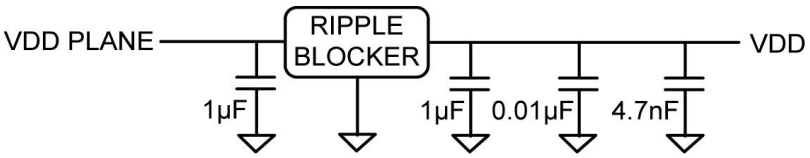
Use one 4.7nF capacitor for each VDD pin.

The impedance value of the Ferrite Bead (FB) needs to be between 240 Ohms and 600 Ohms with a saturation current >=150mA.

The VDDO1 and VDDO2 pins connect directly to the VDD Plane. All VDD pins connect to VDD after the power supply filter.

Power Supply Filtering Recommendations

Preferred filter, using Micrel MIC94300 or MIC94310 Ripple Blocker:



Alternative, traditional filter, using a ferrite bead:

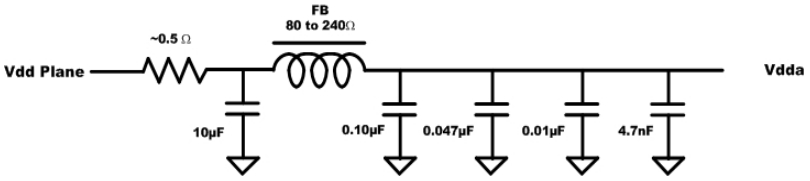


Figure 1. VDDA (Analog) traditional Pi filter

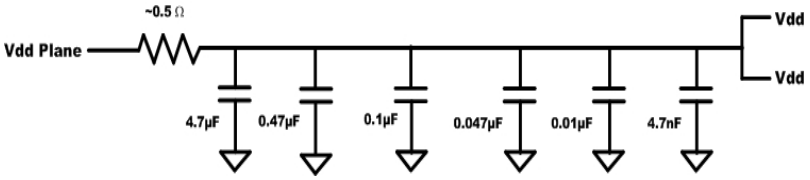


Figure 2. Recommended Power Supply Filtering

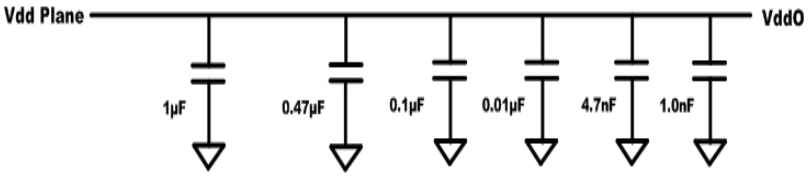


Figure 3. Recommended decoupling for each VDDO

Timing Diagrams

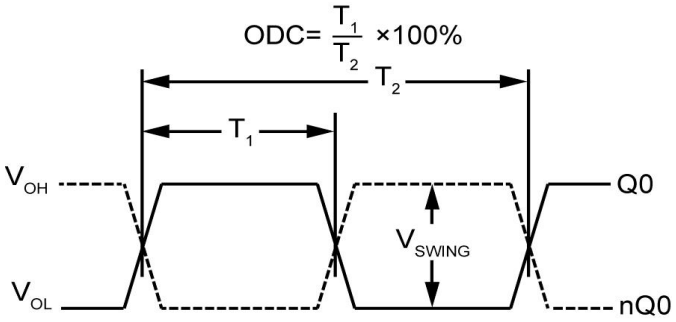


Figure 4. Duty Cycle Timing

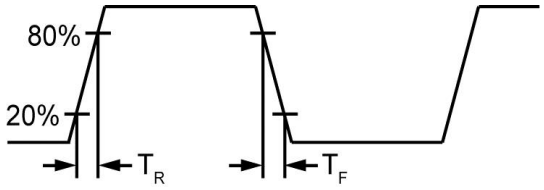


Figure 5. All Outputs Rise/Fall Time

RMS Phase/Noise/Jitter

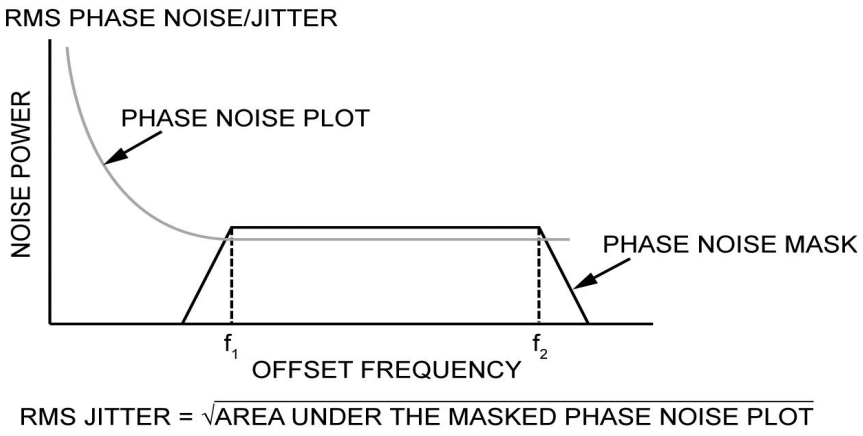


Figure 6. RMS Phase/Noise/Jitter

Output Termination

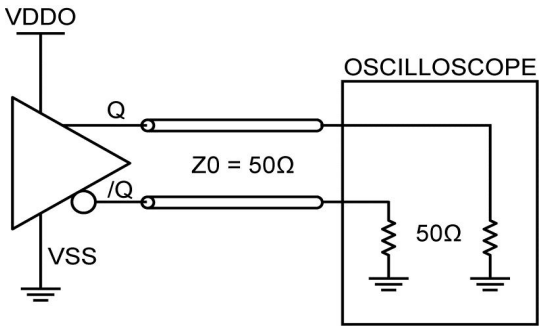


Figure 7. HCSL Output Load and Test Circuit

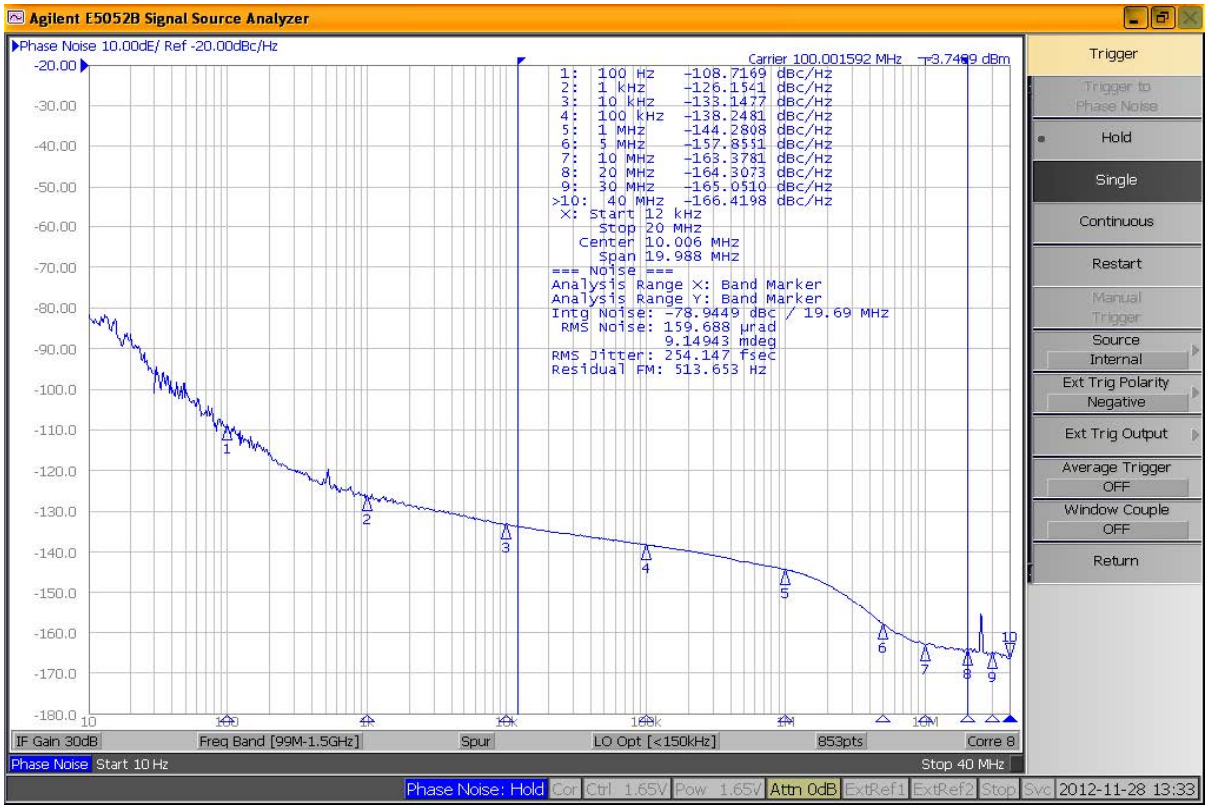


Figure 8. 100MHz HCSL Output, 12kHz-20MHz 254fs

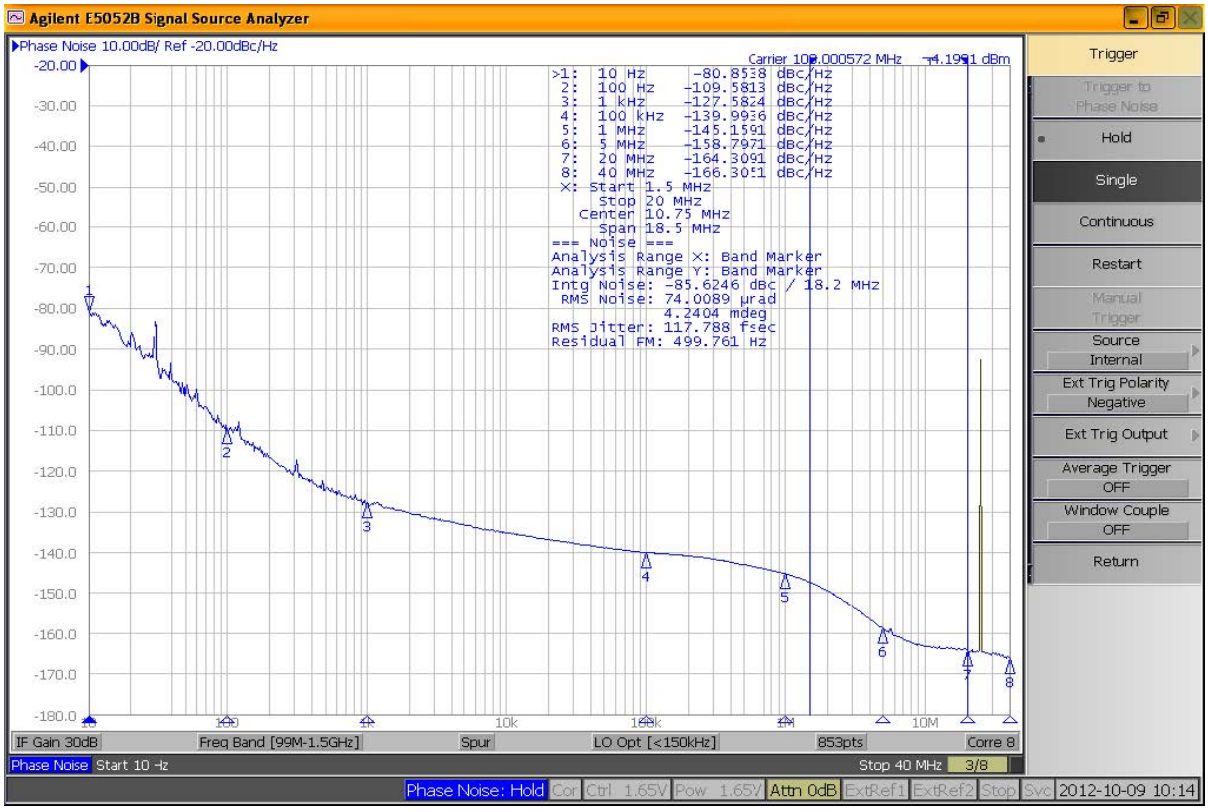


Figure 9. 100MHz HCSL Output, 1.5MHz-20MHz 118fs

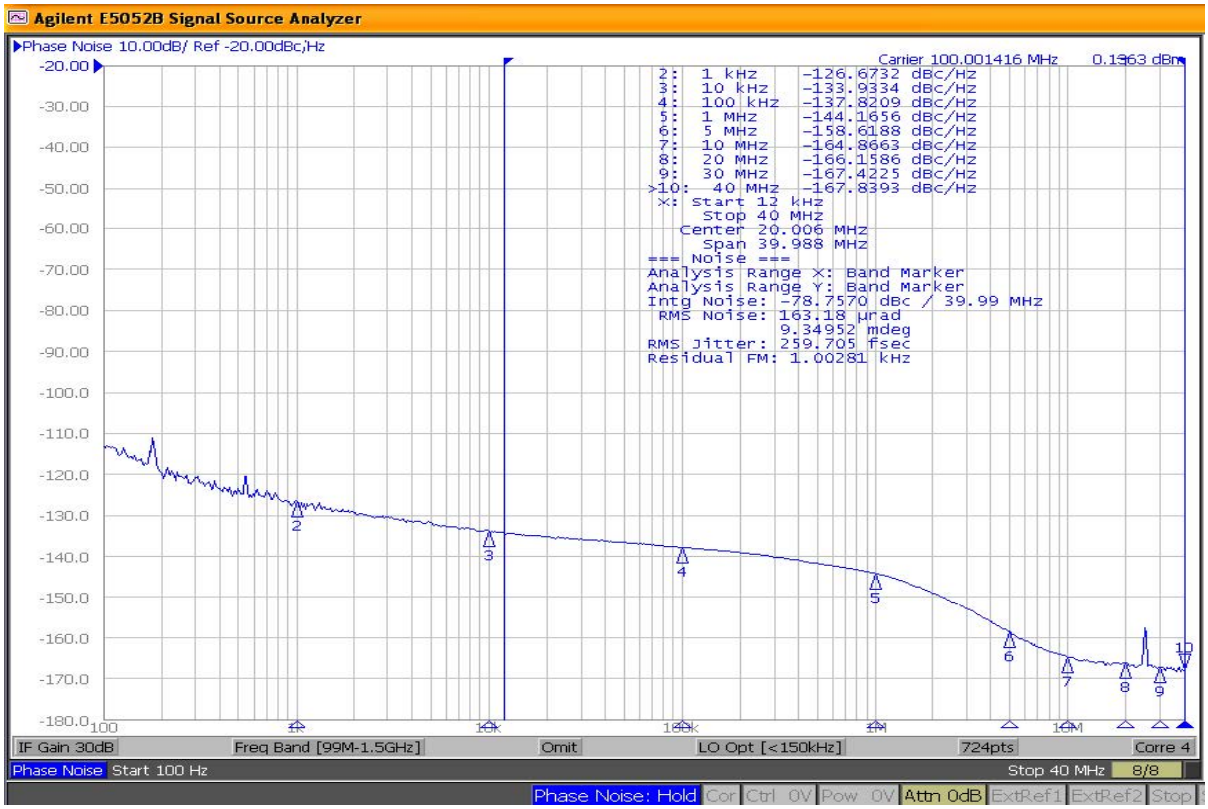


Figure 10. 100MHz HCSL Output, 12kHz-40MHz 260fs

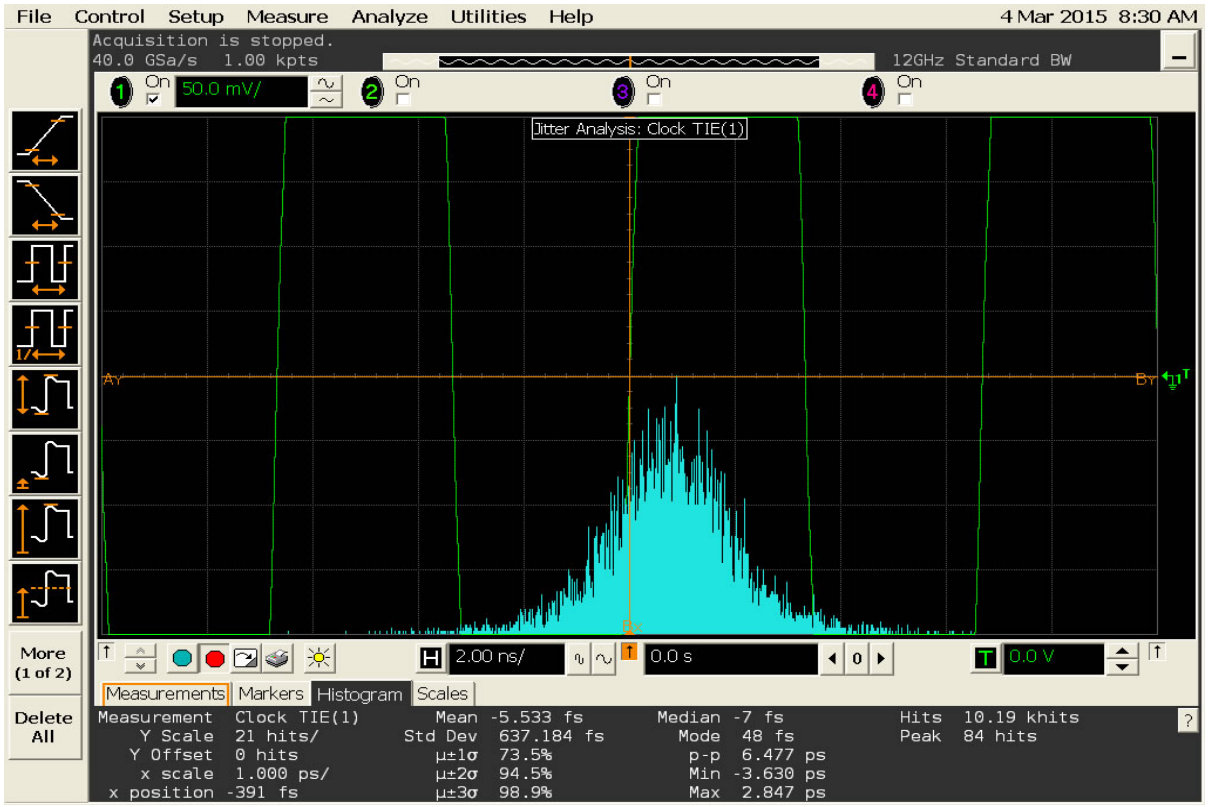


Figure 11. TIE Jitter (10K samples)

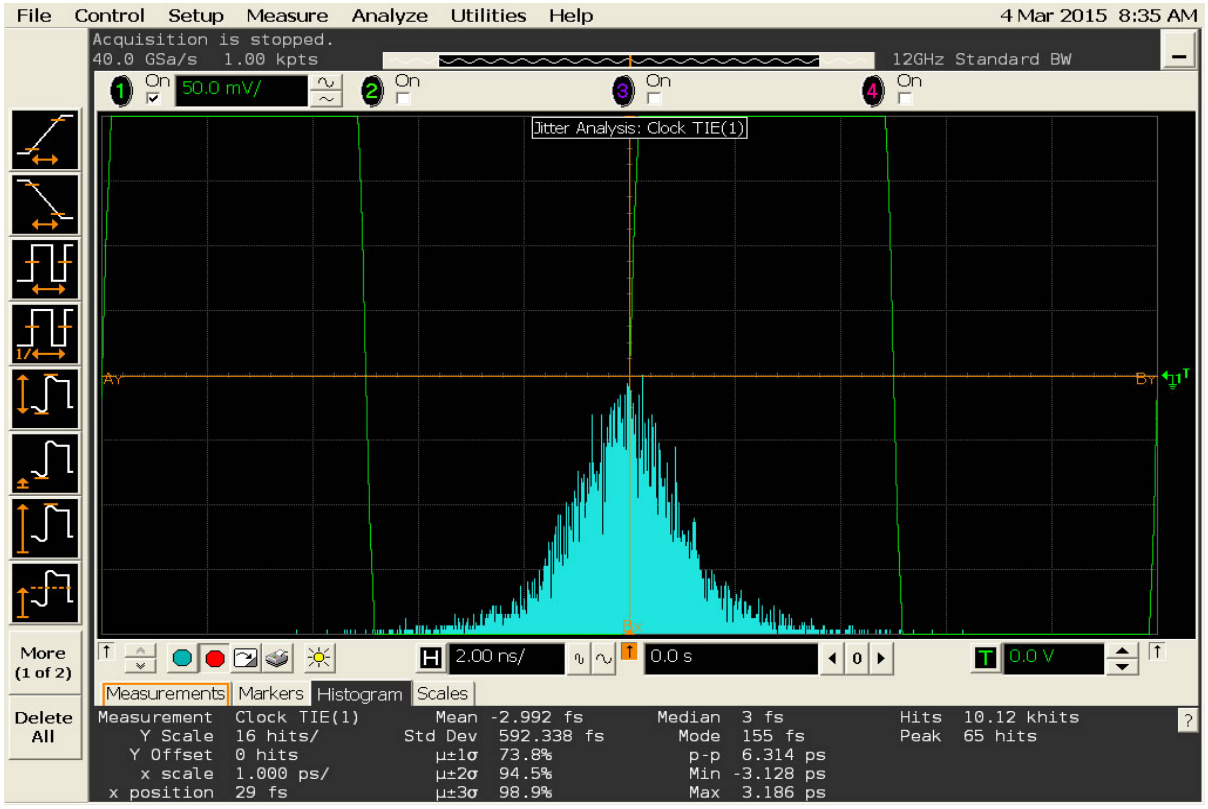
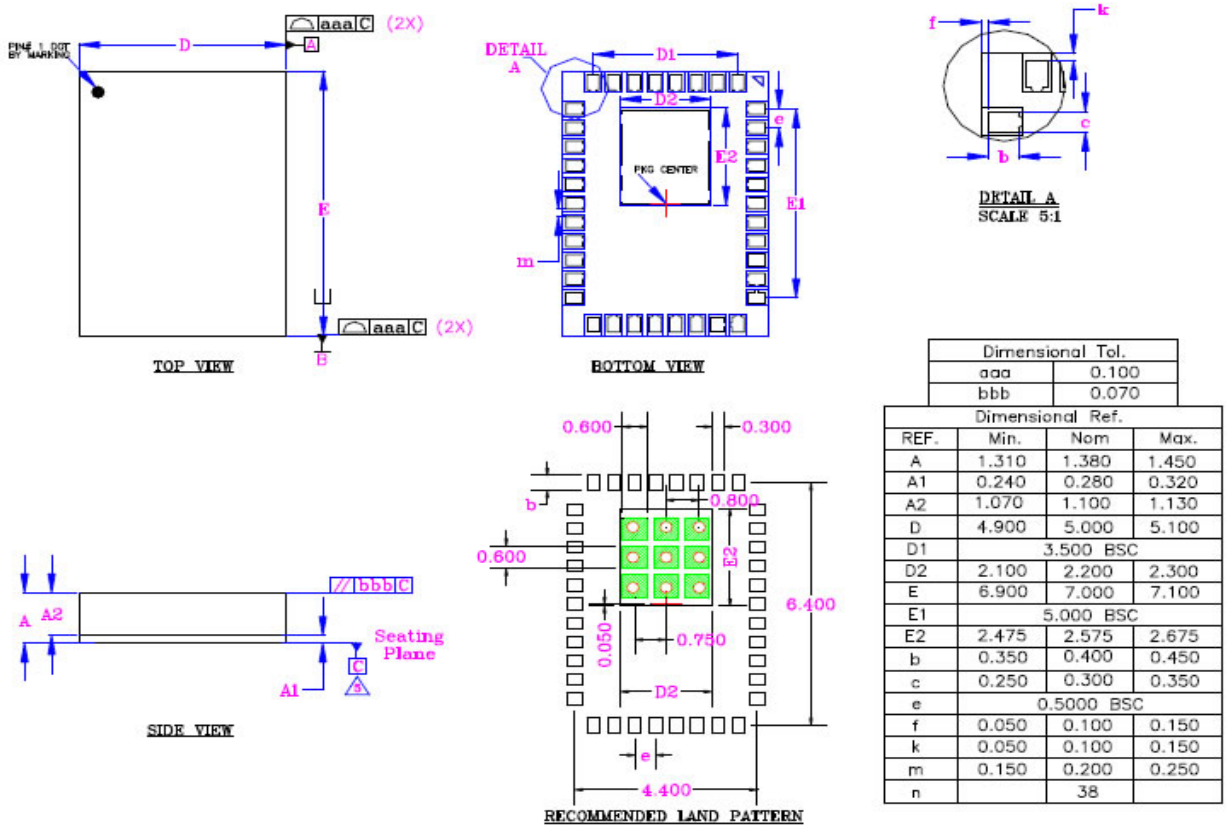


Figure 12. TIE Jitter (10K samples)

Package Information and Recommended Land Pattern for 38-Pin LGA[6]



Dimensional Tol.	
aaa	0.100
bbb	0.070

Dimensional Ref.			
REF.	Min.	Nom	Max.
A	1.310	1.380	1.450
A1	0.240	0.280	0.320
A2	1.070	1.100	1.130
D	4.900	5.000	5.100
D1		3.500 BSC	
D2	2.100	2.200	2.300
E	6.900	7.000	7.100
E1		5.000 BSC	
E2	2.475	2.575	2.675
b	0.350	0.400	0.450
c	0.250	0.300	0.350
e		0.5000 BSC	
f	0.050	0.100	0.150
k	0.050	0.100	0.150
m	0.150	0.200	0.250
n		38	

Notes:
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimensions are in millimeters.
3. 'e' represents the basic LGA pitch.
4. 'n' is the maximum no. of Land for a specified Package.
5. Package warp shall be 0.050 max.
6. Substrate base is BT Resin.
7. The Pin#1 corner must be identified on top side only.
8. Reference JEDEC Spec M0-220.
9. Red circles in land pattern indicate thermal via. Size should be 0.30mm in diameter. Pitch is 0.80mm and connected to GND for maximum thermal performance.
10. Green rectangles (SHADED AREA) indicate solder stencil opening on exposed pad area. Size is 0.60x0.60mm. Pitch is 0.75mm.
11. Land Pattern Tolerance is ±0.02mm.

38-Pin 5mm x 7mm LGA

Note:

6. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.