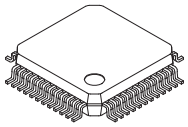
LC75890W

1/4-Duty and Static Drive General-Purpose LCD Driver

ON Semiconductor®

www.onsemi.com



SPQFP48 7x7 / SQFP48

Overview

The LC75890W is the 1/4 duty and static drive general-purpose LCD display driver that can be used for displaying segments for household appliances, home audio visual products, portable devices and other such products under the control of a microcontroller.The LC75890W can drive up to 148 segments directly. In addition the LC75890W can control up to 12 general-purpose output ports. They can control the brightness of the LED backlight of RGB, because they have the PWM output of greatest 3CH built-in. Incorporation of the oscillation circuit helps to reduce the number of external resistors and capacitors required. Incorporation of the LCD drive bias voltage stabilization circuit helps to reduce the capacitors for the LCD drive bias voltage stabilization.

Features

- Support for 1/4-duty 1/3-bias or static drive techniques under serial data control.
  When 1/4-duty drive : Capable of driving up to 148 segments
  When Static drive : Capable of driving up to 37 segments
- Support for display segment on, off, or blinking for each segment output pin under serial data control.
- Serial data control of the power-saving mode based backup function and the all segments forced off function.
- Serial data control of switching between the segment output port and general-purpose output port function.
  < Support for up to 12 general-purpose output ports >
- Support for the PWM output function of a maximum of 3 ch.
  (It can output from the general-purpose output port).
- Serial data control of the frame frequency of the common and segment output waveforms.
- Serial data control of the segment blinking frequency.
- Serial data control of switching between the internal oscillator operating mode and external clock operating mode.
- Serial data input supports CCB* format communication with the system controller.
- Independent V_{LCD} for the LCD driver block.
- Built-in LCD drive bias voltage stabilization circuit.
- The $\overline{INH}$ pin allows the display to be forced to the off state.
- Incorporation of an oscillator circuit.
  (Incorporation of resistor and capacitor for an oscillation)

* Computer Control Bus (CCB) is an ON Semiconductor's original bus format and the bus addresses are controlled by ON Semiconductor.

ORDERING INFORMATION

See detailed ordering and shipping information on page 29 of this data sheet.

July 2017 - Rev. 2
Publication Order Number :
LC75890W/D

Specifications

Absolute Maximum Ratings at Ta = 25°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	V_{DD}	−0.3 to +4.2	V
	V_{LCD} max	V_{LCD}	−0.3 to +6.5	
Input voltage	$V_{IN}1$	CE, CL, DI, $\overline{INH}$	−0.3 to +4.2	V
	$V_{IN}2$	OSCI : External clock operating mode	−0.3 to V_{DD}+0.3	
Output voltage	V_{OUT}	S1 to S37, COM1 to COM4, P1 to P12	−0.3 to V_{LCD}+0.3	V
Output current	$I_{OUT}1$	S1 to S36	300	μA
	$I_{OUT}2$	COM1 to COM4, S37	3	mA
	$I_{OUT}3$	P1 to P12 *1	5	
Allowable power dissipation	Pd max	Ta = 85°C	100	mW
Operating temperature	Topr		−40 to +85	°C
Storage temperature	Tstg		−55 to +125	°C

Note : *1 The sum of output current through P1 to P12 must be 40 mA or less.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Allowable Operating Ranges at Ta = −40 to +85°C, V_{SS} = 0 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}	V_{DD}	2.7		3.6	V
	V_{LCD}	V_{LCD}: Internal oscillator operating mode	2.7		5.5	
		V_{LCD}: External clock operating mode	V_{DD}		5.5	
Input high-level voltage	$V_{IH}1$	CE, CL, DI, $\overline{INH}$	0.7V_{DD}		3.6	V
	$V_{IH}2$	OSCI: External clock operating mode	0.7V_{DD}		V_{DD}	
Input low-level voltage	$V_{IL}1$	CE, CL, DI, $\overline{INH}$	0		0.2V_{DD}	V
	$V_{IL}2$	OSCI: External clock operating mode	0		0.2V_{DD}	
External clock operating frequency	f_{CK}	OSCI: External clock operating mode [Figure 3]	10	38	600	kHz
External clock duty cycle	D_{CK}	OSCI: External clock operating mode [Figure 3]	30	50	70	%
Data setup time	tds	CL, DI [Figure 1], [Figure 2]	160			ns
Data hold time	tdh	CL, DI [Figure 1], [Figure 2]	160			ns
CE wait time	tcp	CE, CL [Figure 1], [Figure 2]	160			ns
CE setup time	tcs	CE, CL [Figure 1], [Figure 2]	160			ns
CE hold time	tch	CE, CL [Figure 1], [Figure 2]	160			ns
High-level clock pulse width	tϕH	CL [Figure 1], [Figure 2]	160			ns
Low-level clock pulse width	tϕL	CL [Figure 1], [Figure 2]	160			ns
Rise time	tr	CE, CL, DI [Figure 1], [Figure 2]		160		ns
Fall time	tf	CE, CL, DI [Figure 1], [Figure 2]		160		ns
$\overline{INH}$ switching time	tc	$\overline{INH}$ [Figure 4], [Figure 5]	10			μs

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Electrical Characteristics for the Allowable Operating Ranges

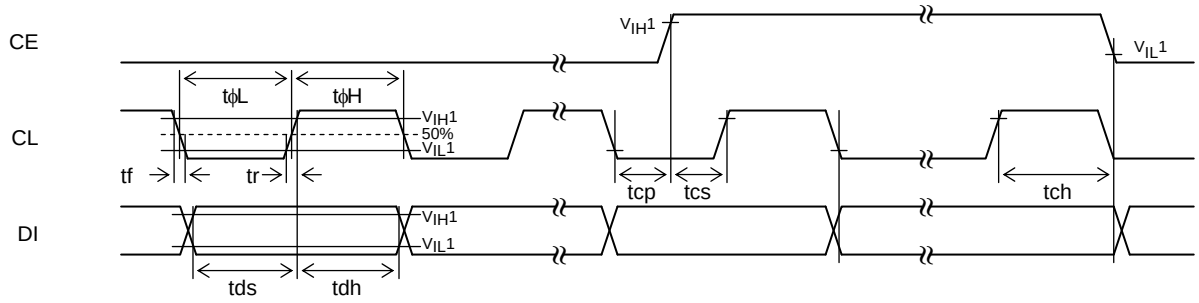
Parameter	Symbol	Pin	Conditions	Ratings			Unit
				min	typ	max	
Hysteresis	V_H	CE, CL, DI, $\overline{INH}$			$0.1V_{DD}$		V
Input high-level current	$I_{IH}1$	CE, CL, DI, $\overline{INH}$	V_I = 3.6 V			1.0	μA
	$I_{IH}2$	OSCI	$V_I = V_{DD}$: External clock operating mode			1.0	
Input low-level current	$I_{IL}1$	CE, CL, DI, $\overline{INH}$	V_I = 0 V	–1.0			μA
	$I_{IL}2$	OSCI	V_I = 0 V : External clock operating mode	–1.0			
Output high-level voltage	$V_{OH}1$	S1 to S37	I_O = –10 μA	V_{LCD}–0.9			V
	$V_{OH}2$	COM1 to COM4	I_O = –100 μA	V_{LCD}–0.9			
	$V_{OH}3$	P1 to P12	I_O = –1 mA	V_{LCD}–0.9			
Output low-level voltage	$V_{OL}1$	S1 to S37	I_O = 10 μA			0.9	V
	$V_{OL}2$	COM1 to COM4	I_O = 100 μA			0.9	
	$V_{OL}3$	P1 to P12	I_O = 1 mA			0.9	
Output middle-level voltage	$V_{MID}1$	S1 to S37	1/4 duty I_O = ±10 μA	2/3V_{LCD} –0.9		2/3V_{LCD} +0.9	V
	$V_{MID}2$	S1 to S37	1/4 duty I_O = ±10 μA	1/3V_{LCD} –0.9		1/3V_{LCD} +0.9	
	$V_{MID}3$	COM1 to COM4	1/4 duty I_O = ±100 μA	2/3V_{LCD} –0.9		2/3V_{LCD} +0.9	
	$V_{MID}4$	COM1 to COM4	1/4 duty I_O = ±100 μA	1/3V_{LCD} –0.9		1/3V_{LCD} +0.9	
Oscillator frequency	fosc	Internal oscillator circuit	Internal oscillator operating mode	240	300	360	kHz
Current drain	$I_{DD}1$	V_{DD}	Power-saving mode			2	μA
	$I_{DD}2$	V_{DD}	V_{DD} = 3.3 V, Normal mode, External clock operating mode *2		5	10	
	$I_{DD}3$	V_{DD}	V_{DD} = 3.3 V, Normal mode, External clock operating mode *2 Serial data transfer *3		90	180	
	$I_{DD}4$	V_{DD}	V_{DD} = 3.3 V, Normal mode, Internal oscilloator operating mode		50	100	
	$I_{DD}5$	V_{DD}	V_{DD} = 3.3 V, Normal mode, Internal oscilloator operating mode, Serial data transfer *3		135	270	
	$I_{LCD}1$	V_{LCD}	Power-saving mode			2	
	$I_{LCD}2$	V_{LCD}	V_{LCD} = 3.3 V, Output open, Normal mode, Static drive		8	16	
	$I_{LCD}3$	V_{LCD}	V_{LCD} = 3.3 V, Output open, Normal mode, 1/4 duty drive		70	140	
	$I_{LCD}4$	V_{LCD}	V_{LCD} = 5.0 V, Output open, Normal mode, Static drive		10	20	
	$I_{LCD}5$	V_{LCD}	V_{LCD} = 5.0 V, Output open, Normal mode, 1/4 duty drive		90	180	

Note : *2 External clock operating mode (f_{CK} = 38 kHz, $V_{IH}2 = V_{DD}$, $V_{IL}2$ = 0 V, rise/fall time = 20 ns)

*3 Serial data transfer (data transfer frequency 2 MHz, $V_{IH}1 = V_{DD}$, $V_{IL}1$ = 0 V, rise/fall time = 20 ns)

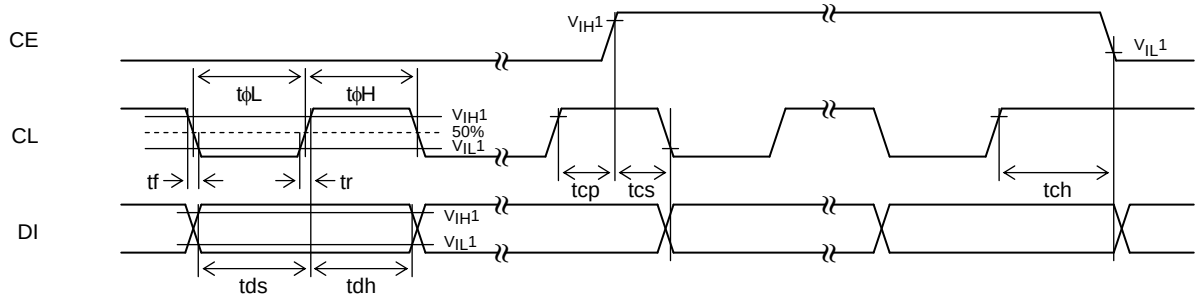
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. When CL is stopped at the low level



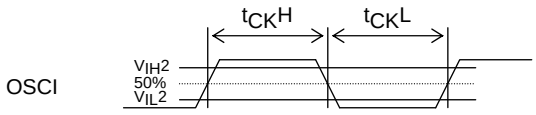
[Figure 1]

2. When CL is stopped at the high level



[Figure 2]

3. OSCI pin clock timing in external clock operating mode



$$f_{CK} = \frac{1}{t_{CK}H + t_{CK}L} \quad [kHz]$$

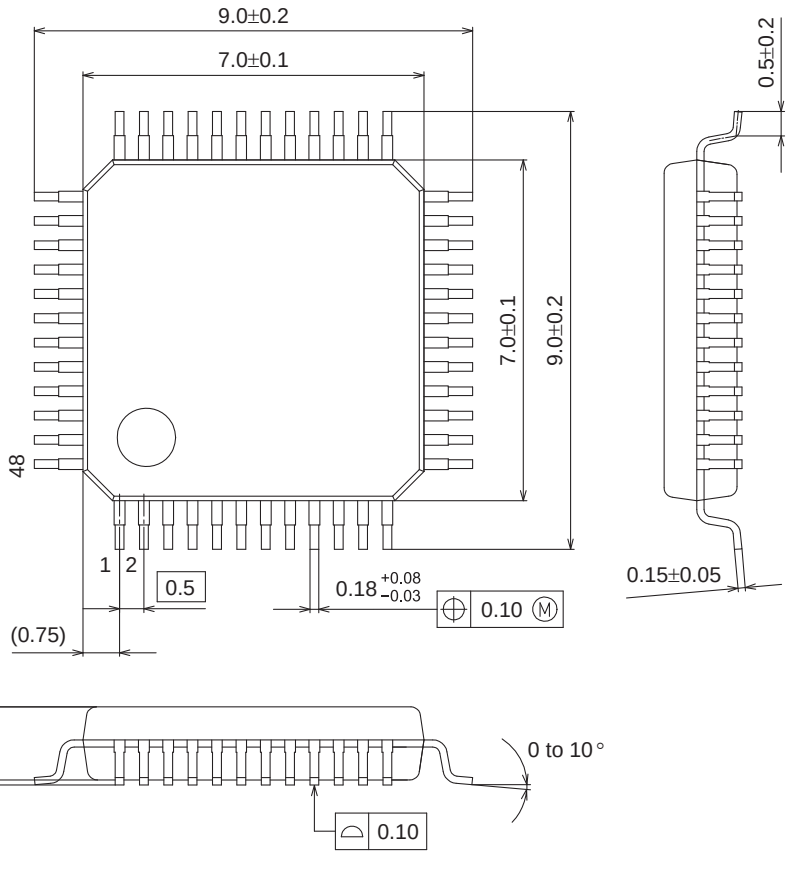
$$D_{CK} = \frac{t_{CK}H}{t_{CK}H + t_{CK}L} \times 100[\%]$$

[Figure 3]

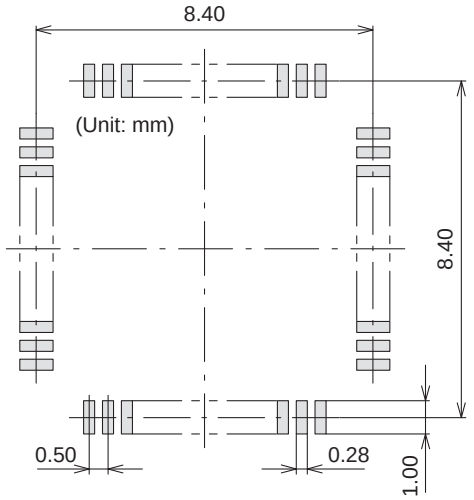
Package Dimensions

unit : mm

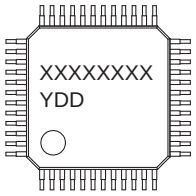
SPQFP48 7x7 / SQFP48
CASE 131AJ
ISSUE A



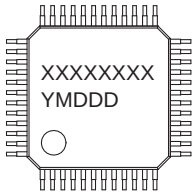
SOLDERING FOOTPRINT*



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
Y = Year
DD = Additional Traceability Data



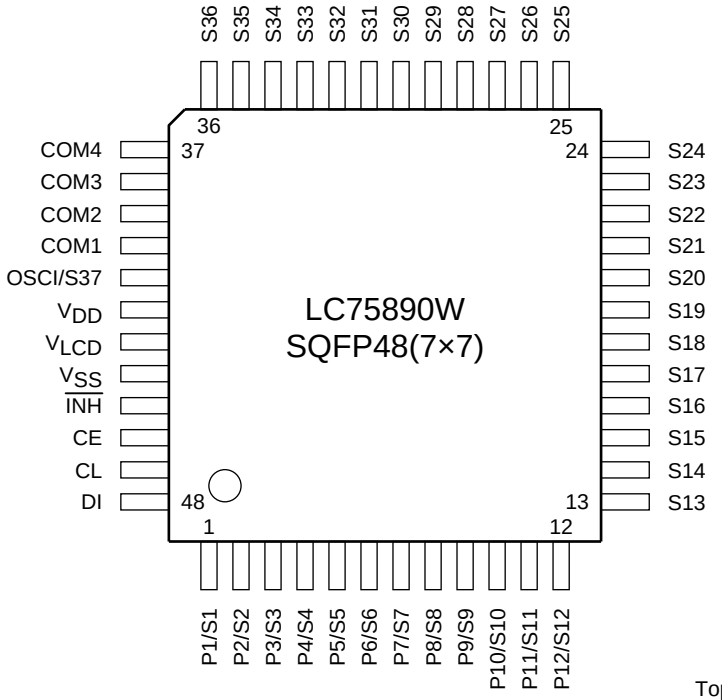
XXXXX = Specific Device Code
Y = Year
M = Month
DDD = Additional Traceability Data

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, “G” or microdot “ ▪ ”, may or may not be present.

NOTE: The measurements are not to guarantee but for reference only.

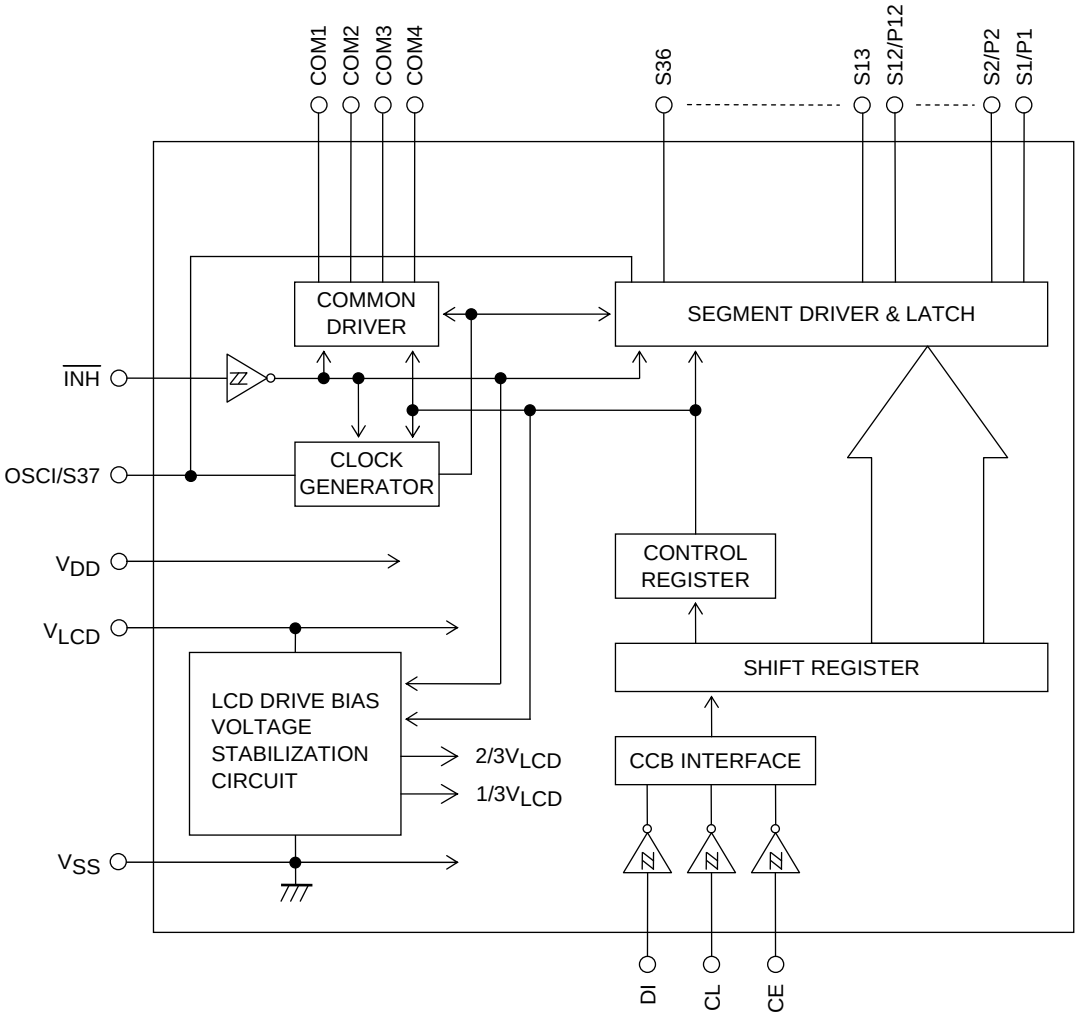
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Pin Assignment



Top view

Block Diagram



Pin Functions

Symbol	Pin No.	Function	Active	I/O	Handling when unused
S1/P1	1	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S12/P12 pins can be used as general-purpose output ports under serial data control.	-	O	OPEN
S2/P2	2				
S3/P3	3				
S4/P4	4				
S5/P5	5				
S6/P6	6				
S7/P7	7				
S8/P8	8				
S9/P9	9				
S10/P10	10				
S11/P11	11				
S12/P12	12				
S13	13				
S14	14				
S15	15				
S16	16				
S17	17				
S18	18				
S19	19				
S20	20				
S21	21				
S22	22				
S23	23				
S24	24				
S25	25				
S26	26				
S27	27				
S28	28				
S29	29				
S30	30				
S31	31				
S32	32				
S33	33				
S34	34				
S35	35				
S36	36				
COM4	37	Common driver outputs The frame frequency is fo[Hz].	-	O	OPEN
COM3	38				
COM2	39				
COM1	40				
S37/OSCI	41	Segment output. This pin can also be used as the external clock input pin when the external clock operating mode is selected by control data.	-	I/O	OPEN
CE	46	Serial data transfer inputs. Must be connected to the controller. CE : Chip enable CL : Synchronization clock DI : Transfer data	H	I	GND
CL	47		↑	I	
DI	48		-	I	

Continued on next page.

Continued from preceding page.

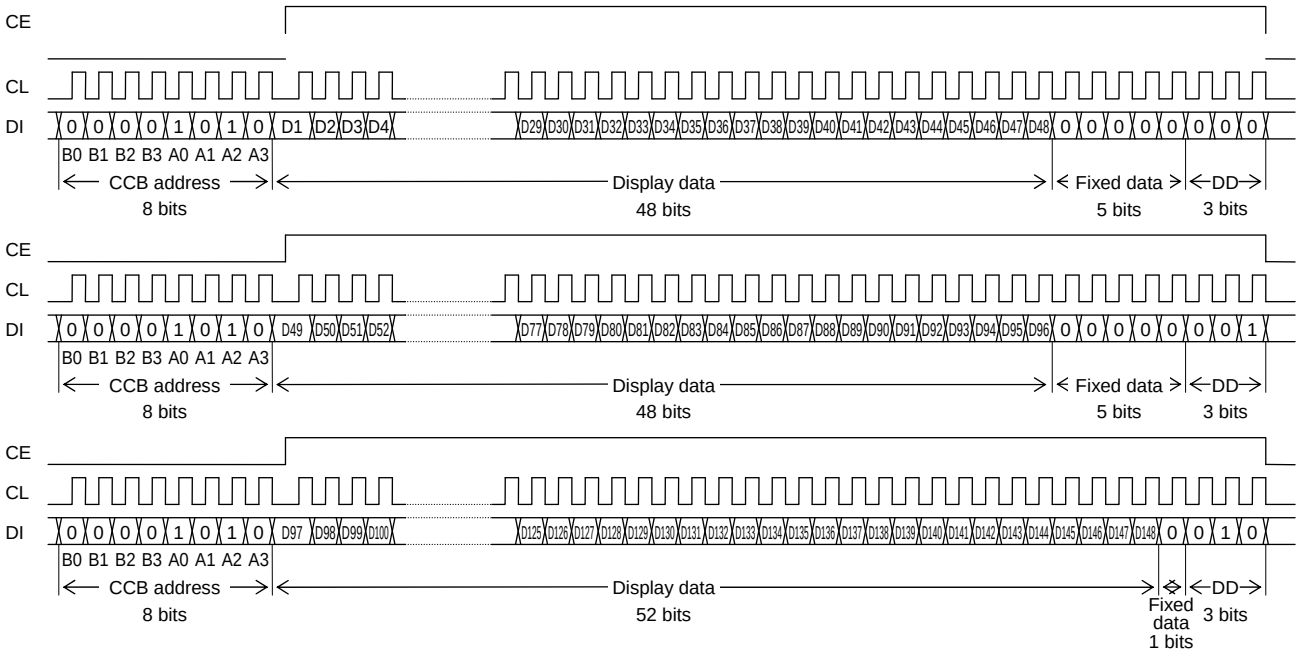
Symbol	Pin No.	Function	Active	I/O	Handling when unused
$\overline{INH}$	45	Display off control input • $\overline{INH}$ = low (V_{SS}) ...Display forced off S1/P1 to S12/P12=low (V_{SS}) (These pins are forcibly set to the general-purpose output port function and held at the V_{SS} level.) S13 to S36=low (V_{SS}) COM1 to COM4=low (V_{SS}) S37/OSCI=low (V_{SS}) (This pin is forcibly set to the segment output port function and held at the V_{SS} level.) LCD drive bias voltage stabilization circuit stopped. Stops the internal oscillator. Inhibits external clock input. • $\overline{INH}$ = high (V_{DD}) ...Display on LCD drive bias voltage stabilization circuit is enabled. Enables the internal oscillator circuit. (Internal oscillator operating mode) Enables external clock input. (External clock operating mode) However, serial data transfer is possible when the display is forced off.	L	I	GND
V_{DD}	42	Logic block power supply pin. A power voltage of 2.7 to 3.6 V must be applied to this pin.	-	-	-
V_{LCD}	43	LCD driver block power supply pin. A power voltage of 2.7 to 5.5 V must be applied to this pin.	-	-	-
V_{SS}	44	Ground pin. Must be connected to ground.	-	-	-

Serial Data Input

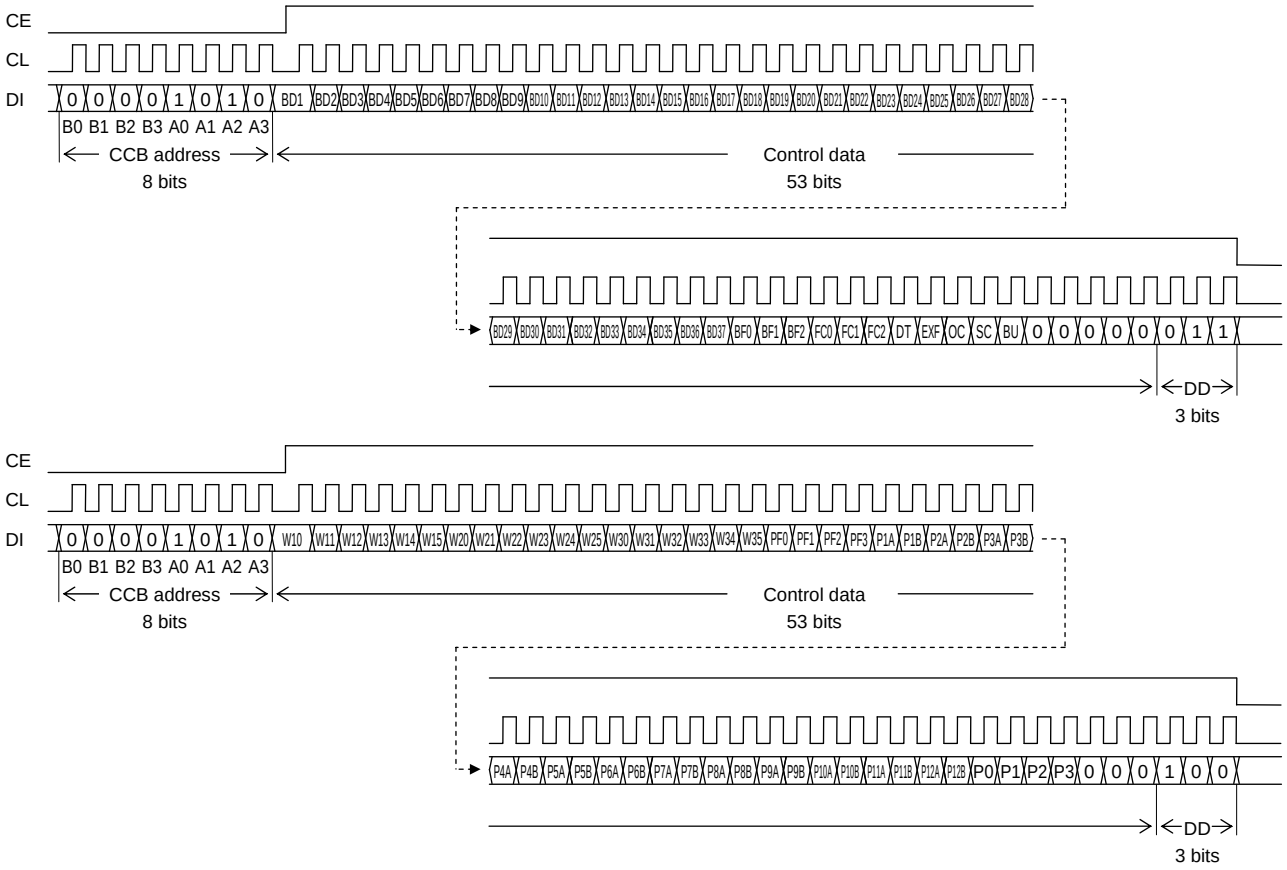
1. 1/4 duty drive

(1) When CL is stopped at the low level

• Display data Input



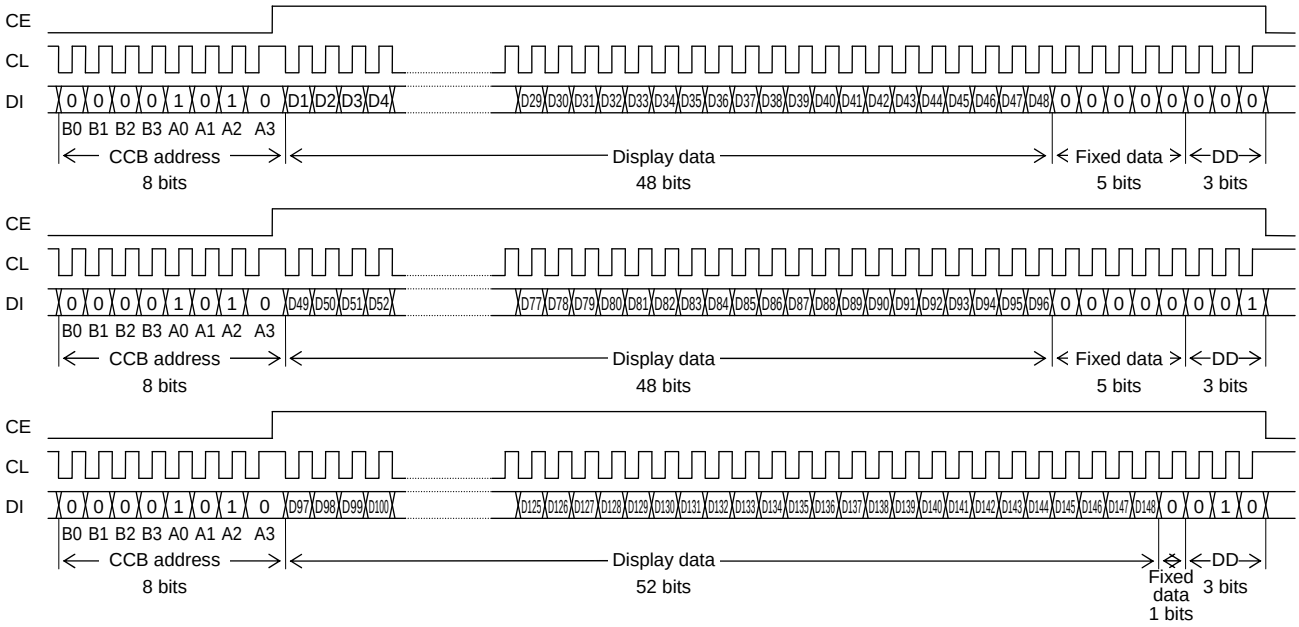
• Control data Input



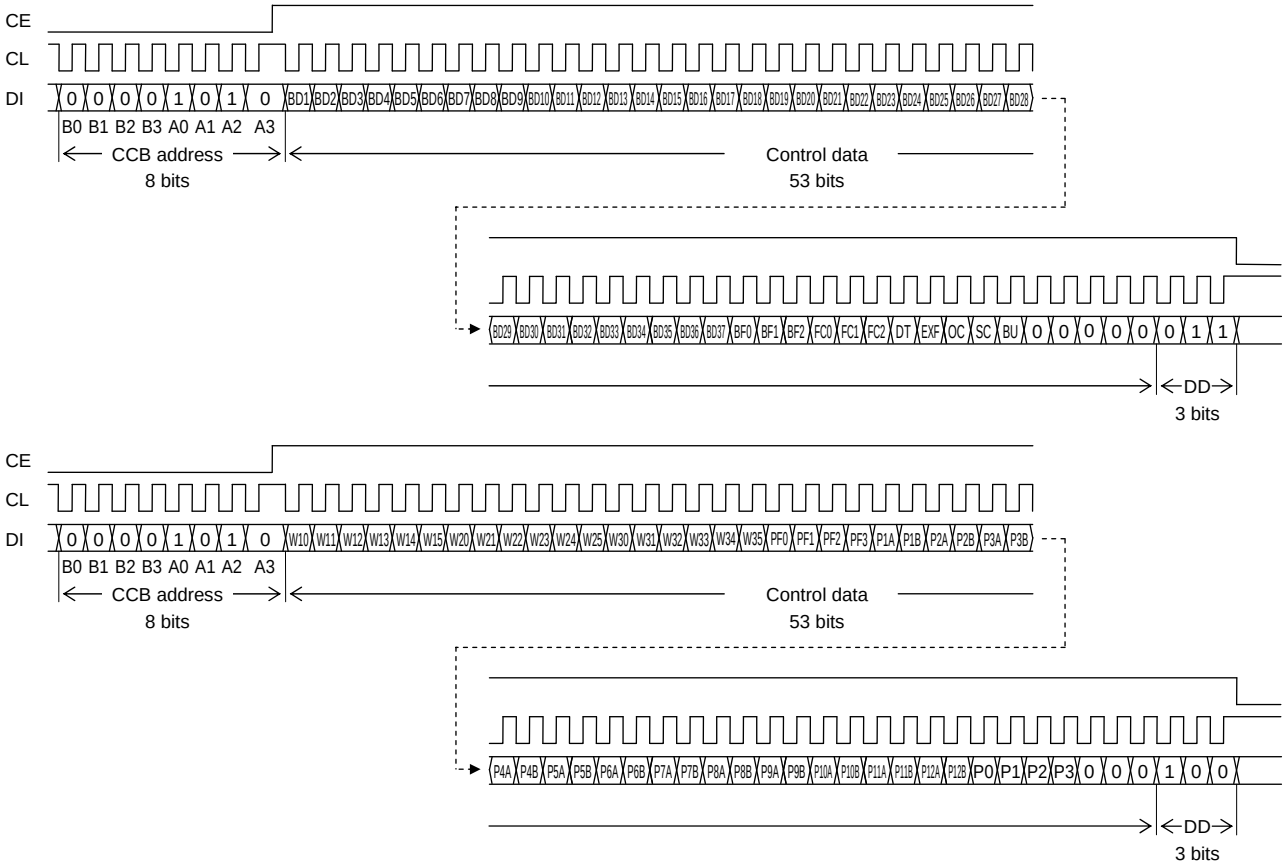
Note: DD is the direction data.

(2) When CL is stopped at the high level

• Display data Input



• Control data Input



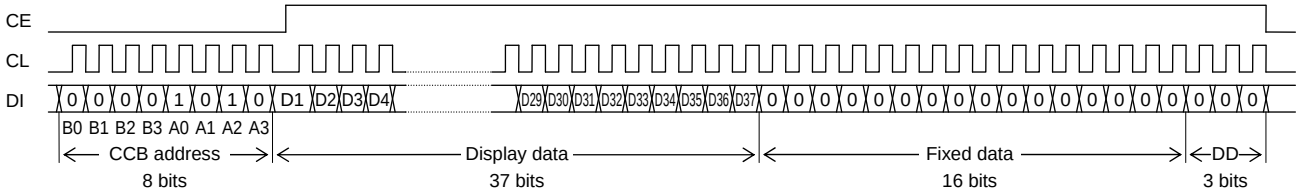
Note: DD is the direction data.

- CCB address ..... “50H”
- D1 to D148 ..... Display data
- BD1 to BD37 ..... Display blinking control data of each segment output pin
- BF0 to BF2 ..... Segment blinking frequency setting control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency setting control data
- DT ..... 1/4-duty 1/3-bias drive or static drive switching control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data
- W10 to W15, W20 to W25,... PWM data of the PWM output
  W30 to W35
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- P1A, P1B to P12A, P12B ..... General-purpose output function/PWM output function switiching control data of the general-purpose output port
- P0 to P3 ..... Segment output port/general-purpose output port switching control data

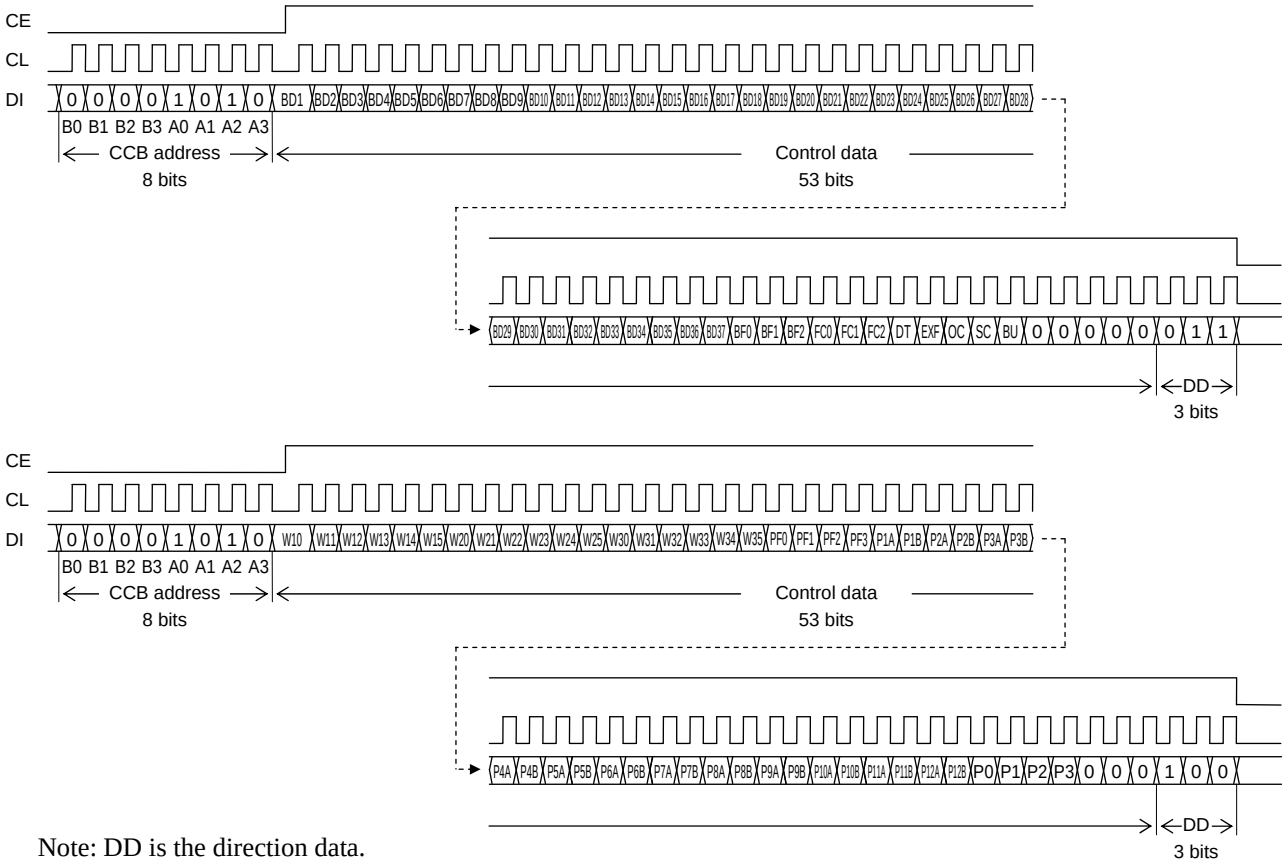
2. Static drive

(1) When CL is stopped at the low level

• Display data Input



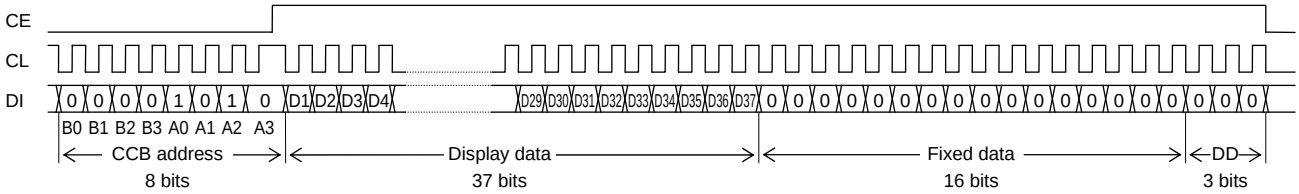
• Control data Input



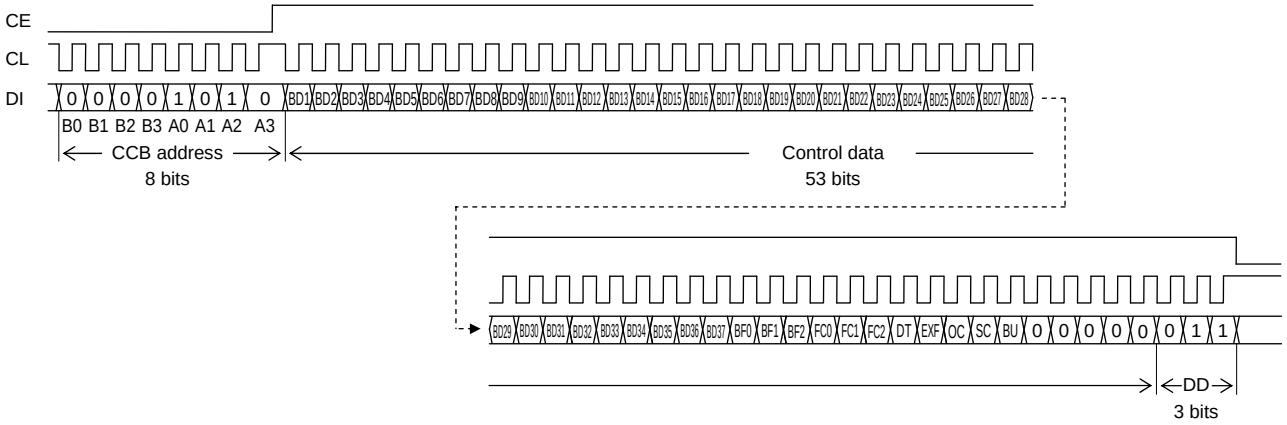
Note: DD is the direction data.

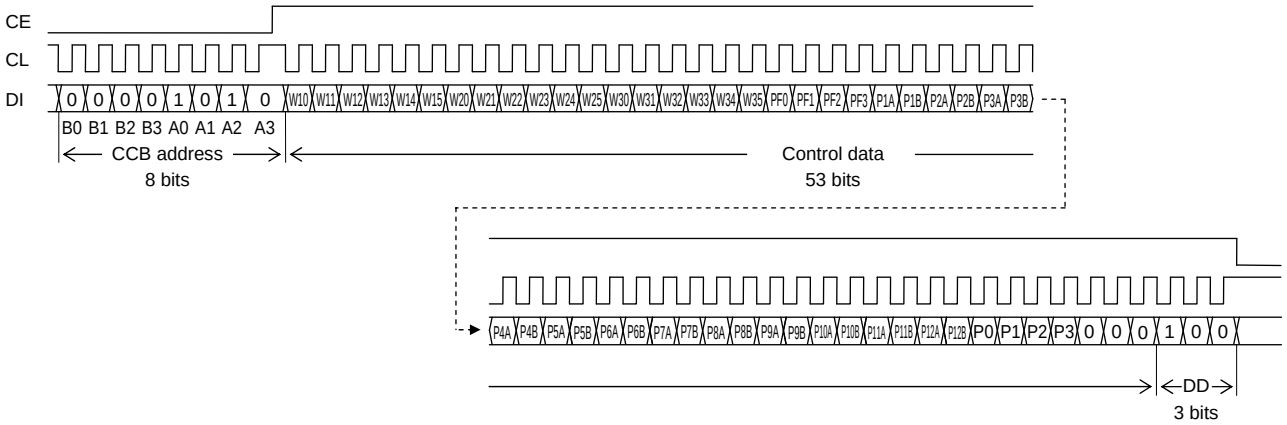
(2) When CL is stopped at the high level

• Display data Input



• Control data Input





Note: DD is the direction data.

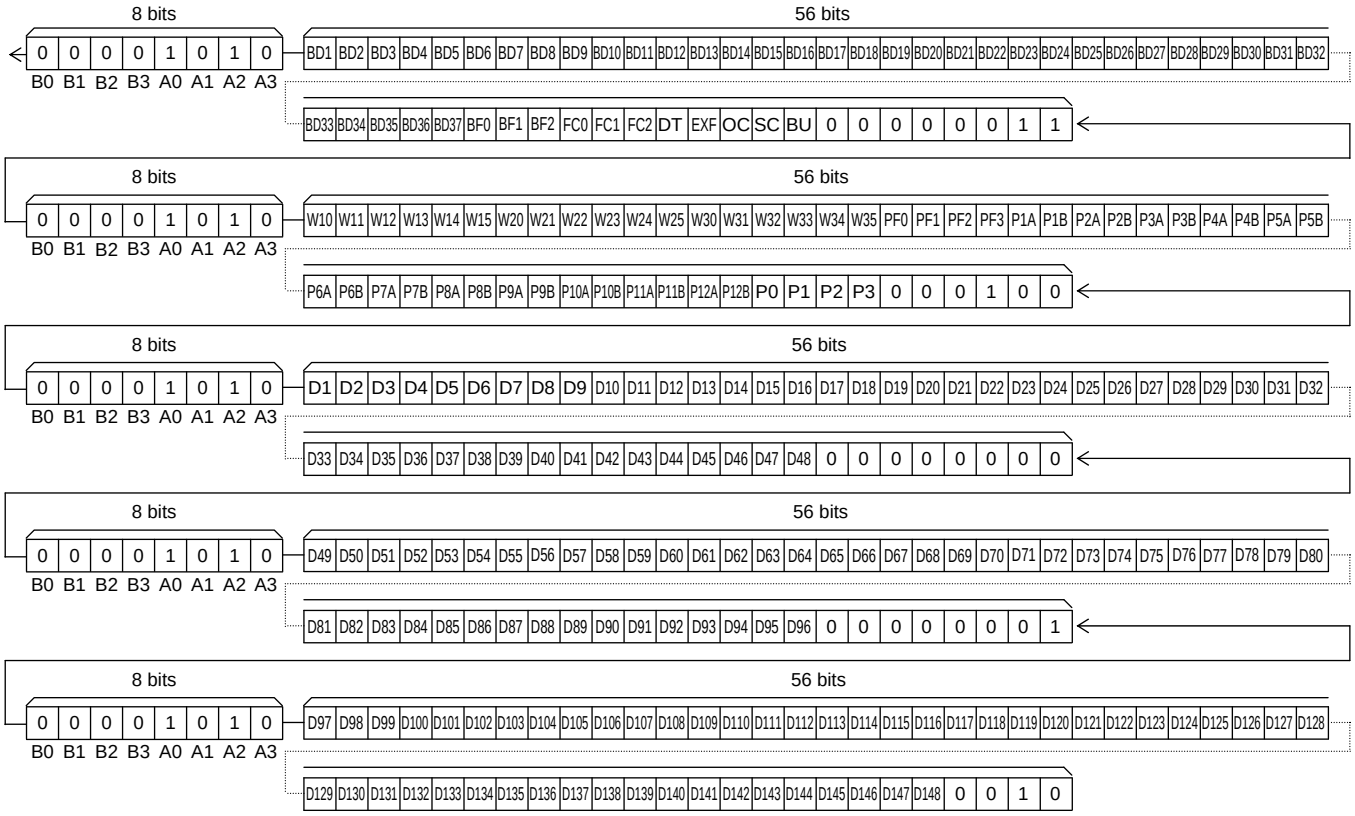
- CCB address ..... "50H"
- D1 to D37 ..... Display data
- BD1 to BD37 ..... Display blinking control data of each segment output pin
- BF0 to BF2 ..... Segment blinking frequency setting control data
- FC0 to FC2 ..... Common/segment output waveform frame frequency setting control data
- DT ..... 1/4-duty 1/3-bias drive or static drive switching control data
- EXF ..... External clock operating frequency setting control data
- OC ..... Internal oscillator operating mode/external clock operating mode switching control data
- SC ..... Segment on/off control data
- BU ..... Normal mode/power-saving mode control data
- W10 to W15, W20 to W25,... PWM data of the PWM output
  W30 to W35
- PF0 to PF3 ..... PWM output waveform frame frequency setting control data
- P1A, P1B to P12A, P12B ..... General-purpose output function/PWM output function switiching control data of the general-purpose output port
- P0 to P3 ..... Segment output port/general-purpose output port switching control data

Serial Data Transfer Example

1. 1/4 duty drive

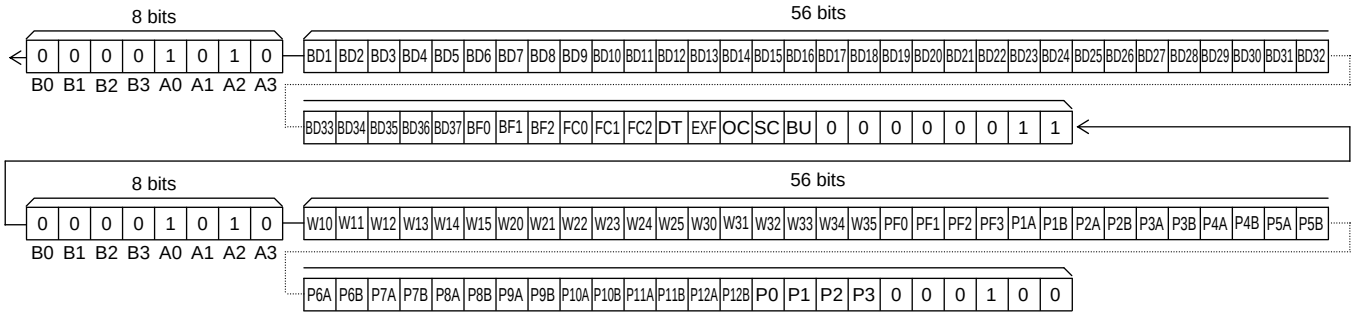
• When 97 or more segments are used

All 320 bits of serial data (including CCB address) must be sent.



• When fewer than 97 segments are used

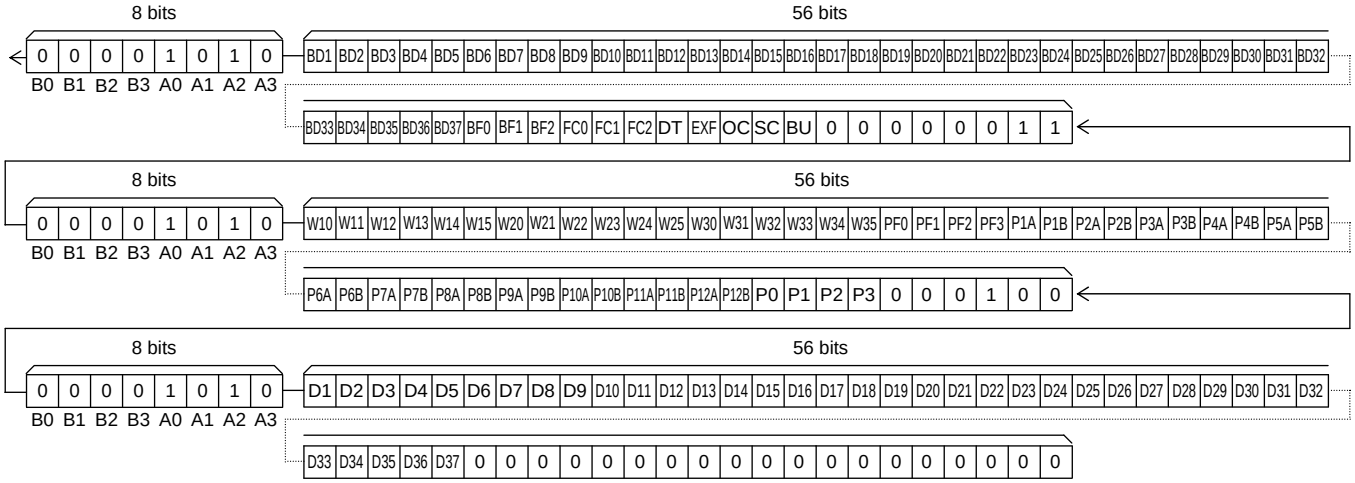
Depending on the number of segments used, 192 bits or 256 bits (including CCB address) must be sent as serial data. However, the serial data (control data) shown in the figure below must be sent without fail.



Note : After the above serial data is sent, the contents of the display data can be changed by transferring only the serial data (CCB address, display data, fixed data, and direction data) including the display data to be changed in 64-bit units.

2. Static drive

• All 192 bits of serial data (including CCB address) must be sent.



Control Data Functions

(1) BD1 to BD37 … Display blinking control data of each segment output pin

These control data bits are used to set the display segment blinking corresponding to each segment output pin.

BDn	Display segment blinking states of segment output pin Sn
0	The display segments are not blinked.
1	The display segments corresponding to the segment output pin Sn that the contents of display data are "1" are blinked.

Note: The BDn (n=1 to 37) are the control data setting the blinking state of the display segments for segment output pins Sn (n=1 to 37).

For example, the display state of segment output pin S21 becomes as follows when the contents of display data are (D81, D82, D83, D84) = (1, 0, 1, 0) in 1/4 duty drive

BD21	Display data				Display states of segment output pin S21			
	D81	D82	D83	D84	COM1	COM2	COM3	COM4
0	1	0	1	0	on	off	on	off
1	1	0	1	0	blink	off	blink	off

(2) BF0 to BF2 … Segment blinking frequency setting control data

These control data bits are used to set the display segment blinking frequency

Control data			Segment blinking frequency fb[Hz]		
BF0	BF1	BF2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz]typ)
0	0	0	fosc/600000	$f_{CK}1$/600000	$f_{CK}2$/75000
1	0	0	fosc/360000	$f_{CK}1$/360000	$f_{CK}2$/45000
0	1	0	fosc/300000	$f_{CK}1$/300000	$f_{CK}2$/37500
1	1	0	fosc/240000	$f_{CK}1$/240000	$f_{CK}2$/30000
0	0	1	fosc/180000	$f_{CK}1$/180000	$f_{CK}2$/22500
1	0	1	fosc/150000	$f_{CK}1$/150000	$f_{CK}2$/18750
0	1	1	fosc/120000	$f_{CK}1$/120000	$f_{CK}2$/15000
1	1	1	fosc/100000	$f_{CK}1$/100000	$f_{CK}2$/12500

(3) FC0 to FC2 … Common/segment output waveform frame frequency setting control data

These control data bits set the frame frequency of the common and segment output waveforms.

Control data			Common/segment output waveform frame frequency fo[Hz]		
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz]typ)
0	0	0	fosc/4608	$f_{CK}1$/4608	$f_{CK}2$/576
0	0	1	fosc/3456	$f_{CK}1$/3456	$f_{CK}2$/432
0	1	0	fosc/3072	$f_{CK}1$/3072	$f_{CK}2$/384
0	1	1	fosc/2304	$f_{CK}1$/2304	$f_{CK}2$/288
1	0	0	fosc/1536	$f_{CK}1$/1536	$f_{CK}2$/192
1	0	1	fosc/1152	$f_{CK}1$/1152	$f_{CK}2$/144
1	1	0	fosc/768	$f_{CK}1$/768	$f_{CK}2$/96

Note: When is setting (FC0, FC1, FC2)=(1, 1, 1), the frame frequency is same as frame frequency at the time of the (FC0, FC1, FC2)=(0, 1, 0) setting (fosc/3072, $f_{CK}1$/3072, $f_{CK}2$/384).

(4) DT … 1/4-duty 1/3-bias drive or static drive switching control data

This control data bit selects either 1/4-duty 1/3-bias drive or static drive.

DT	Drive scheme	Common output pins states		
		COM2	COM3	COM4
0	1/4 duty 1/3 bias drive	COM2	COM3	COM4
1	Static drive	"L" (V_{SS})	"L" (V_{SS})	"L" (V_{SS})

Note: COM2, COM3, COM4 : Common output

"L" (V_{SS}) : "L" (V_{SS}) level output

(5) EXF … External clock operating frequency setting control data

This control data bit sets the operating frequency of the external clock which input into the OSCI pin, when the external clock operating mode (OC = "1") is set. However, this control data is effective only when external clock operating mode (OC = "1") is set.

EXF	External clock operating frequency f_{CK}[kHz]
0	$f_{CK}1$=300[kHz]typ
1	$f_{CK}2$=38[kHz]typ

(6) OC … Internal oscillator operating mode/external clock operating mode switching control data

This control data bit selects either the internal oscillator operating mode or external clock operating mode.

OC	Fundamental clock operating mode	I/O pin (S37/OSCI) state
0	Internal oscillator operating mode	S37
1	External clock operating mode	OSCI

Note: S37: Segment output

OSCI: External clock input

(7) SC … Segment on/off control data

This control data bit controls the on/off state of the segments.

SC	Display state
0	On
1	Off

Note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

(8) BU … Normal mode/power-saving mode control data

This control data bit selects either normal mode or power-saving mode.

BU	Mode
0	Normal mode
1	Power saving mode In this mode, the internal oscillator circuit stops oscillation (the S37/OSCI pin is configured for segment output) if the IC is in the internal oscillator operating mode (OC=0) and the IC stops receiving external clock signals (the S37/OSCI pin is configured for external clock input) if the IC is in the external clock operating mode (OC=1). In addition, the common and segment output pins go to the V_{SS} level and the operation of LCD drive bias voltage stabilization circuit stops. However, the S1/P1 to S12/P12 output pins can be used as general-purpose output ports under the control of the data bits P0 to P3. (The general-purpose output port P1 to P12 can not be used as PWM output).

(9) W10 to W15, W20 to W25, W30 to W35 … PWM data of the PWM output

These control data bits set the pulse width of the PWM output P1 to P12. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2$ = 38[kHz]typ (EXF="1") in external clock operating mode (OC = "1"), these control data bits become invalid.

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output
0	0	0	0	0	0	(1/64)×Tp
1	0	0	0	0	0	(2/64)×Tp
0	1	0	0	0	0	(3/64)×Tp
1	1	0	0	0	0	(4/64)×Tp
0	0	1	0	0	0	(5/64)×Tp
1	0	1	0	0	0	(6/64)×Tp
0	1	1	0	0	0	(7/64)×Tp
1	1	1	0	0	0	(8/64)×Tp
0	0	0	1	0	0	(9/64)×Tp
1	0	0	1	0	0	(10/64)×Tp
0	1	0	1	0	0	(11/64)×Tp
1	1	0	1	0	0	(12/64)×Tp
0	0	1	1	0	0	(13/64)×Tp
1	0	1	1	0	0	(14/64)×Tp
0	1	1	1	0	0	(15/64)×Tp
1	1	1	1	0	0	(16/64)×Tp
0	0	0	0	1	0	(17/64)×Tp
1	0	0	0	1	0	(18/64)×Tp
0	1	0	0	1	0	(19/64)×Tp
1	1	0	0	1	0	(20/64)×Tp
0	0	1	0	1	0	(21/64)×Tp
1	0	1	0	1	0	(22/64)×Tp
0	1	1	0	1	0	(23/64)×Tp
1	1	1	0	1	0	(24/64)×Tp
0	0	0	1	1	0	(25/64)×Tp
1	0	0	1	1	0	(26/64)×Tp
0	1	0	1	1	0	(27/64)×Tp
1	1	0	1	1	0	(28/64)×Tp
0	0	1	1	1	0	(29/64)×Tp
1	0	1	1	1	0	(30/64)×Tp
0	1	1	1	1	0	(31/64)×Tp
1	1	1	1	1	0	(32/64)×Tp

Wn0	Wn1	Wn2	Wn3	Wn4	Wn5	Pulse width of PWM output
0	0	0	0	0	1	(33/64)×Tp
1	0	0	0	0	1	(34/64)×Tp
0	1	0	0	0	1	(35/64)×Tp
1	1	0	0	0	1	(36/64)×Tp
0	0	1	0	0	1	(37/64)×Tp
1	0	1	0	0	1	(38/64)×Tp
0	1	1	0	0	1	(39/64)×Tp
1	1	1	0	0	1	(40/64)×Tp
0	0	0	1	0	1	(41/64)×Tp
1	0	0	1	0	1	(42/64)×Tp
0	1	0	1	0	1	(43/64)×Tp
1	1	0	1	0	1	(44/64)×Tp
0	0	1	1	0	1	(45/64)×Tp
1	0	1	1	0	1	(46/64)×Tp
0	1	1	1	0	1	(47/64)×Tp
1	1	1	1	0	1	(48/64)×Tp
0	0	0	0	1	1	(49/64)×Tp
1	0	0	0	1	1	(50/64)×Tp
0	1	0	0	1	1	(51/64)×Tp
1	1	0	0	1	1	(52/64)×Tp
0	0	1	0	1	1	(53/64)×Tp
1	0	1	0	1	1	(54/64)×Tp
0	1	1	0	1	1	(55/64)×Tp
1	1	1	0	1	1	(56/64)×Tp
0	0	0	1	1	1	(57/64)×Tp
1	0	0	1	1	1	(58/64)×Tp
0	1	0	1	1	1	(59/64)×Tp
1	1	0	1	1	1	(60/64)×Tp
0	0	1	1	1	1	(61/64)×Tp
1	0	1	1	1	1	(62/64)×Tp
0	1	1	1	1	1	(63/64)×Tp
1	1	1	1	1	1	(64/64)×Tp

Note: W10 to W15 … PWM data of the PWM output (Ch1)
W20 to W25 … PWM data of the PWM output (Ch2)
W30 to W35 … PWM data of the PWM output (Ch3)

$$Tp = \frac{1}{fp}$$

(10) PF0 to PF3 … PWM output waveform frame frequency setting control data

These control data bits set the frame frequency of the PWM output waveforms. However, when the PWM output function isn't used, these control data bits become invalid. In addition, when the external clock operating frequency is set the $f_{CK}2$ = 38[kHz]typ (EXF="1") in external clock operating mode (OC = "1"), these control data bits become invalid.

Control data				PWM output waveform frame frequency fp[Hz]	
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz] typ)
0	0	0	0	fosc/1536	$f_{CK}1$/1536
1	0	0	0	fosc/1408	$f_{CK}1$/1408
0	1	0	0	fosc/1280	$f_{CK}1$/1280
1	1	0	0	fosc/1152	$f_{CK}1$/1152
0	0	1	0	fosc/1024	$f_{CK}1$/1024
1	0	1	0	fosc/896	$f_{CK}1$/896
0	1	1	0	fosc/768	$f_{CK}1$/768
1	1	1	0	fosc/640	$f_{CK}1$/640
0	0	0	1	fosc/512	$f_{CK}1$/512
1	0	0	1	fosc/384	$f_{CK}1$/384
0	1	0	1	fosc/256	$f_{CK}1$/256

Note: When are setting (PF0, PF1, PF2, PF3)=(1, 1, 0, 1) and (X, X, 1, 1), the frame frequency is same as frame frequency at the time of the (PF0, PF1, PF2, PF3)=(1, 0, 1, 0) setting (fosc/896, $f_{CK}1$/896).

X: don't care

(11) P1A, P1B to P12A, P12B … General-purpose output function/PWM output function switiching control data of the general-purpose output port

These control data bits set the general-purpose output function (High or low level output) or PWM output function of the general-purpose output ports P1 to P12. However, when the S1/P1 to S12/P12 output pins arn't set the general-purpose output port, these control data bits become invalid. In addition, be careful of being unable to set a PWM output function when the external clock operating frequency is set the $f_{CK}2$ = 38[kHz]typ (EXF="1") in external clock operating mode (OC = "1").

PnA	PnB	Functions of the general-purpose output port (Pn)
0	0	General-purpose output function (High or low level output)
1	0	PWM output function (Ch1)
0	1	PWM output function (Ch2)
1	1	PWM output function (Ch3)

Note: The data PnA, PnB (n=1 to 12) are the control data switching the general-purpose output function or PWM output function of the general-purpose output ports P1 to p12. For example, if the S10/P10 output pin is set the general-purpose output port, the general-purpose output port P10 pin is selected the PWM output function (Ch1) when (P10A, P10B) = (1, 0).

(12) P0 to P3 … Segment output port/general-purpose output port switching control data

These control data bits switch the segment output port/general-purpose output port functions of the S1/P1 to S12/P12 output pins.

Control data				Output pin state											
P0	P1	P2	P3	S1/P1	S2/P2	S3/P3	S4/P4	S5/P5	S6/P6	S7/P7	S8/P8	S9/P9	S10/P10	S11/P11	S12/P12
0	0	0	0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	0	1	P1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	0	P1	P2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	0	1	1	P1	P2	P3	S4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	0	P1	P2	P3	P4	S5	S6	S7	S8	S9	S10	S11	S12
0	1	0	1	P1	P2	P3	P4	P5	S6	S7	S8	S9	S10	S11	S12
0	1	1	0	P1	P2	P3	P4	P5	P6	S7	S8	S9	S10	S11	S12
0	1	1	1	P1	P2	P3	P4	P5	P6	P7	S8	S9	S10	S11	S12
1	0	0	0	P1	P2	P3	P4	P5	P6	P7	P8	S9	S10	S11	S12
1	0	0	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	S10	S11	S12
1	0	1	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	S11	S12
1	0	1	1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	S12
1	1	0	0	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12

Note1: Sn (n=1 to 12)…Segment output port Pn (n=1 to 12)…General-purpose output port

Note2: When are setting (P0, P1, P2, P3)=(1, 1, 0, 1), (1, 1, 1, 0) and (1, 1, 1, 1), the all S1/P1 to S12/P12 output pins are selected the segment output port.

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports (general-purpose output function).

Output pin	Correspondence display data	
	1/4 duty drive	Static drive
S1/P1	D1	D1
S2/P2	D5	D2
S3/P3	D9	D3
S4/P4	D13	D4
S5/P5	D17	D5
S6/P6	D21	D6
S7/P7	D25	D7
S8/P8	D29	D8
S9/P9	D33	D9
S10/P10	D37	D10
S11/P11	D41	D11
S12/P12	D45	D12

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port and is set general-purpose output function, the S4/P4 output pin will output a high (V_{LCD}) level when the display data D13 is 1, and will output a low (V_{SS}) level when D13 is 0.

Display Data and Display Blinking Control Data and Output Pin Correspondence (1/4 Duty Drive)

Output pin	COM1	COM2	COM3	COM4	Blinking control data
S1/P1	D1	D2	D3	D4	BD1
S2/P2	D5	D6	D7	D8	BD2
S3/P3	D9	D10	D11	D12	BD3
S4/P4	D13	D14	D15	D16	BD4
S5/P5	D17	D18	D19	D20	BD5
S6/P6	D21	D22	D23	D24	BD6
S7/P7	D25	D26	D27	D28	BD7
S8/P8	D29	D30	D31	D32	BD8
S9/P9	D33	D34	D35	D36	BD9
S10/P10	D37	D38	D39	D40	BD10
S11/P11	D41	D42	D43	D44	BD11
S12/P12	D45	D46	D47	D48	BD12
S13	D49	D50	D51	D52	BD13
S14	D53	D54	D55	D56	BD14
S15	D57	D58	D59	D60	BD15
S16	D61	D62	D63	D64	BD16
S17	D65	D66	D67	D68	BD17
S18	D69	D70	D71	D72	BD18

Output pin	COM1	COM2	COM3	COM4	Blinking control data
S19	D73	D74	D75	D76	BD19
S20	D77	D78	D79	D80	BD20
S21	D81	D82	D83	D84	BD21
S22	D85	D86	D87	D88	BD22
S23	D89	D90	D91	D92	BD23
S24	D93	D94	D95	D96	BD24
S25	D97	D98	D99	D100	BD25
S26	D101	D102	D103	D104	BD26
S27	D105	D106	D107	D108	BD27
S28	D109	D110	D111	D112	BD28
S29	D113	D114	D115	D116	BD29
S30	D117	D118	D119	D120	BD30
S31	D121	D122	D123	D124	BD31
S32	D125	D126	D127	D128	BD32
S33	D129	D130	D131	D132	BD33
S34	D133	D134	D135	D136	BD34
S35	D137	D138	D139	D140	BD35
S36	D141	D142	D143	D144	BD36
S37/OSCI	D145	D146	D147	D148	BD37

Note: This table assumes that pins S1/P1 to S12/P12 and S37/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

Display data				Blinking control data	Output pin (S21) state
D81	D82	D83	D84	BD21	
0	0	0	0	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	0	0	1	0	The LCD segment corresponding to COM4 is on.
0	0	1	0	0	The LCD segment corresponding to COM3 is on.
0	0	1	1	0	The LCD segments corresponding to COM3 and COM4 are on.
0	1	0	0	0	The LCD segment corresponding to COM2 is on.
0	1	0	1	0	The LCD segments corresponding to COM2 and COM4 are on.
0	1	1	0	0	The LCD segments corresponding to COM2 and COM3 are on.
0	1	1	1	0	The LCD segments corresponding to COM2, COM3, and COM4 are on.
1	0	0	0	0	The LCD segment corresponding to COM1 is on.
1	0	0	1	0	The LCD segments corresponding to COM1 and COM4 are on.
1	0	1	0	0	The LCD segments corresponding to COM1 and COM3 are on.
1	0	1	1	0	The LCD segments corresponding to COM1, COM3, and COM4 are on.
1	1	0	0	0	The LCD segments corresponding to COM1 and COM2 are on.
1	1	0	1	0	The LCD segments corresponding to COM1, COM2, and COM4 are on.
1	1	1	0	0	The LCD segments corresponding to COM1, COM2, and COM3 are on.
1	1	1	1	0	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are on.
0	0	0	0	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are off.
0	1	0	1	1	The LCD segments corresponding to COM2 and COM4 are blinking.
1	0	1	0	1	The LCD segments corresponding to COM1 and COM3 are blinking.
1	1	1	1	1	The LCD segments corresponding to COM1, COM2, COM3, and COM4 are blinking.

Display Data and Display Blinking Control Data and Output Pin Correspondence (Static Drive)

Output pin	COM1	Blinking control data
S1/P1	D1	BD1
S2/P2	D2	BD2
S3/P3	D3	BD3
S4/P4	D4	BD4
S5/P5	D5	BD5
S6/P6	D6	BD6
S7/P7	D7	BD7
S8/P8	D8	BD8
S9/P9	D9	BD9
S10/P10	D10	BD10
S11/P11	D11	BD11
S12/P12	D12	BD12
S13	D13	BD13
S14	D14	BD14
S15	D15	BD15
S16	D16	BD16
S17	D17	BD17
S18	D18	BD18

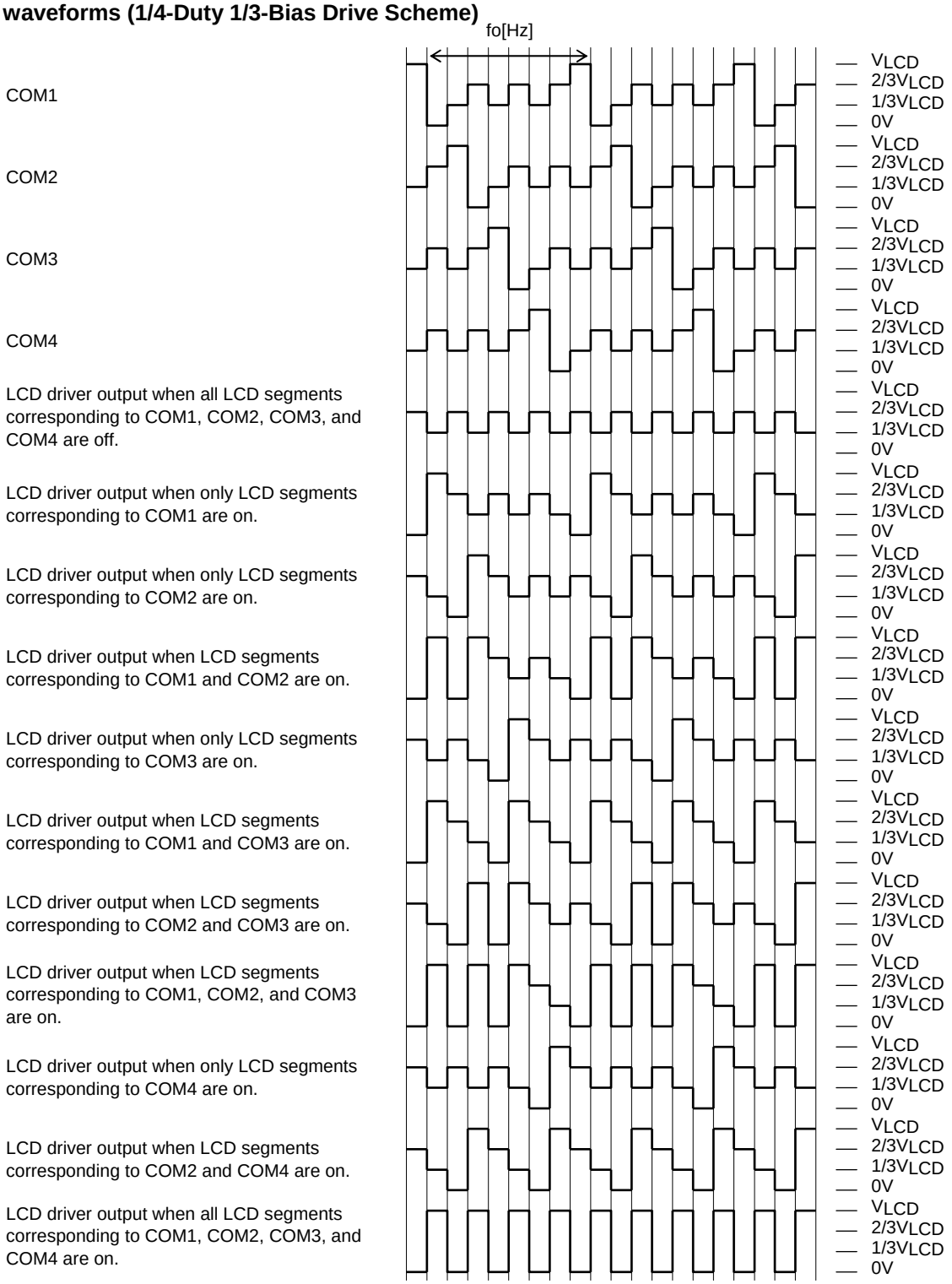
Output pin	COM1	Blinking control data
S19	D19	BD19
S20	D20	BD20
S21	D21	BD21
S22	D22	BD22
S23	D23	BD23
S24	D24	BD24
S25	D25	BD25
S26	D26	BD26
S27	D27	BD27
S28	D28	BD28
S29	D29	BD29
S30	D30	BD30
S31	D31	BD31
S32	D32	BD32
S33	D33	BD33
S34	D34	BD34
S35	D35	BD35
S36	D36	BD36
S37/OSCI	D37	BD37

Note: This table assumes that pins S1/P1 to S12/P12 and S37/OSCI are configured for segment output.

For example, the table below lists the output states for the S21 output pin.

Display data	Blinking control data	Output pin (S21) state
D21	BD21	
0	0	The LCD segment corresponding to COM1 is off.
1	0	The LCD segment corresponding to COM1 is on.
0	1	The LCD segment corresponding to COM1 is off.
1	1	The LCD segment corresponding to COM1 is blinking.

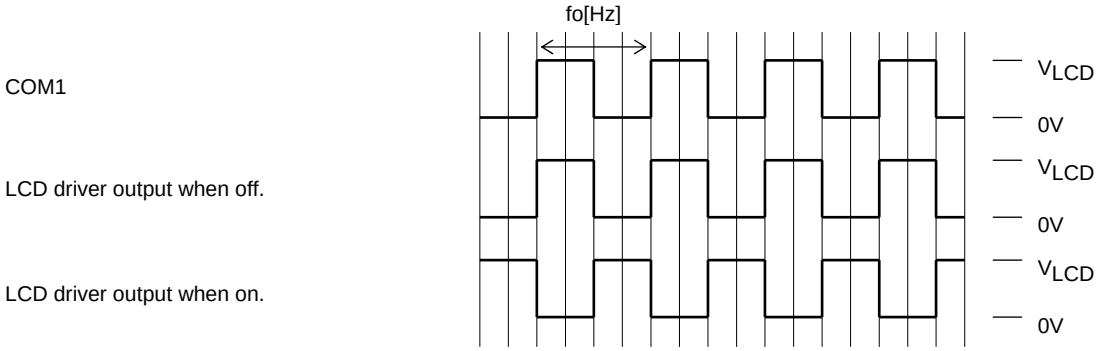
Output waveforms (1/4-Duty 1/3-Bias Drive Scheme)



Control data			Common/segment output waveform frame frequency fo[Hz]		
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz]typ)
0	0	0	fosc/4608	$f_{CK}1/4608$	$f_{CK}2/576$
0	0	1	fosc/3456	$f_{CK}1/3456$	$f_{CK}2/432$
0	1	0	fosc/3072	$f_{CK}1/3072$	$f_{CK}2/384$
0	1	1	fosc/2304	$f_{CK}1/2304$	$f_{CK}2/288$
1	0	0	fosc/1536	$f_{CK}1/1536$	$f_{CK}2/192$
1	0	1	fosc/1152	$f_{CK}1/1152$	$f_{CK}2/144$
1	1	0	fosc/768	$f_{CK}1/768$	$f_{CK}2/96$

Note: When is setting (FC0, FC1, FC2) = (1, 1, 1), the frame frequency is same as frame frequency at the time of the (FC0, FC1, FC2) = (0, 1, 0) setting (fosc/3072, $f_{CK}1/3072$, $f_{CK}2/384$).

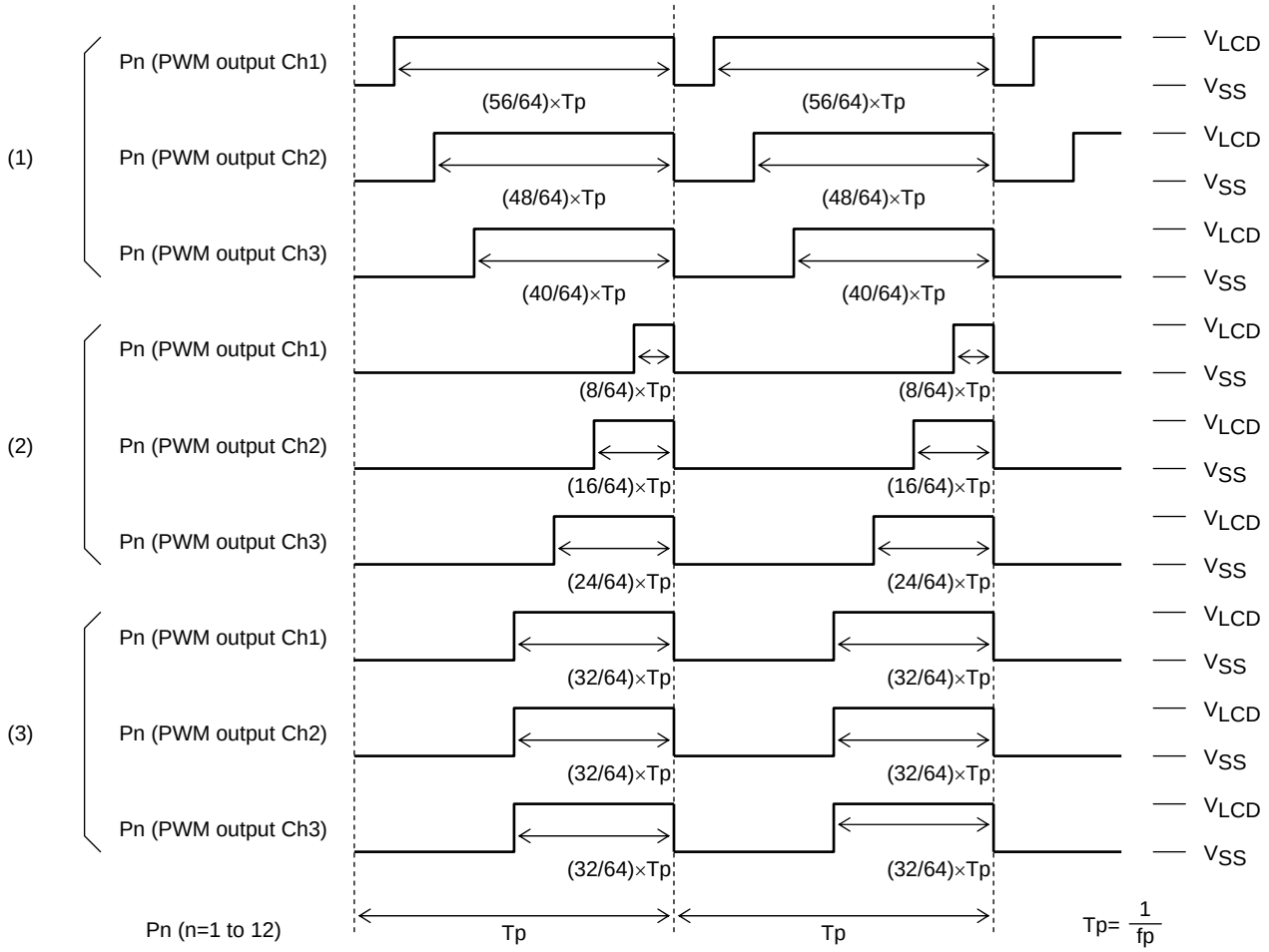
Output waveforms (Static Drive Scheme)



Control data			Common/segment output waveform frame frequency fo[Hz]		
FC0	FC1	FC2	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 0, $f_{CK}1$=300[kHz]typ)	External clock operating mode (The control data OC is 1 and EXF is 1, $f_{CK}2$=38[kHz]typ)
0	0	0	fosc/4608	$f_{CK}1/4608$	$f_{CK}2/576$
0	0	1	fosc/3456	$f_{CK}1/3456$	$f_{CK}2/432$
0	1	0	fosc/3072	$f_{CK}1/3072$	$f_{CK}2/384$
0	1	1	fosc/2304	$f_{CK}1/2304$	$f_{CK}2/288$
1	0	0	fosc/1536	$f_{CK}1/1536$	$f_{CK}2/192$
1	0	1	fosc/1152	$f_{CK}1/1152$	$f_{CK}2/144$
1	1	0	fosc/768	$f_{CK}1/768$	$f_{CK}2/96$

Note: When is setting (FC0, FC1, FC2) = (1, 1, 1), the frame frequency is same as frame frequency at the time of the (FC0, FC1, FC2) = (0, 1, 0) setting (fosc/3072, $f_{CK}1/3072$, $f_{CK}2/384$).

PWM output waveforms



Control data																		PWM output waveforms
W10	W11	W12	W13	W14	W15	W20	W21	W22	W23	W24	W25	W30	W31	W32	W33	W34	W35	
1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0	0	1	(1)
1	1	1	0	0	0	1	1	1	1	0	0	1	1	1	0	1	0	(2)
1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	(3)

Control data				PWM output waveform frame frequency fp[Hz]	
PF0	PF1	PF2	PF3	Internal oscillator operating mode (The control data OC is 0, fosc=300[kHz] typ)	External clock operating mode (The control data OC is 1 and EXF is 0, f_{CK}1=300[kHz] typ)
0	0	0	0	fosc/1536	f_{CK}1/1536
1	0	0	0	fosc/1408	f_{CK}1/1408
0	1	0	0	fosc/1280	f_{CK}1/1280
1	1	0	0	fosc/1152	f_{CK}1/1152
0	0	1	0	fosc/1024	f_{CK}1/1024
1	0	1	0	fosc/896	f_{CK}1/896
0	1	1	0	fosc/768	f_{CK}1/768
1	1	1	0	fosc/640	f_{CK}1/640
0	0	0	1	fosc/512	f_{CK}1/512
1	0	0	1	fosc/384	f_{CK}1/384
0	1	0	1	fosc/256	f_{CK}1/256

Note1: When is setting (PF0, PF1, PF2, PF3) = (1, 1, 0, 1) and (X, X, 1, 1), the frame frequency is same as frame frequency at the time of the (PF0, PF1, PF2, PF3) = (1, 0, 1, 0) setting (fosc/896, f_{CK}1/896). X: don't care

Display Control and the $\overline{INH}$ Pin

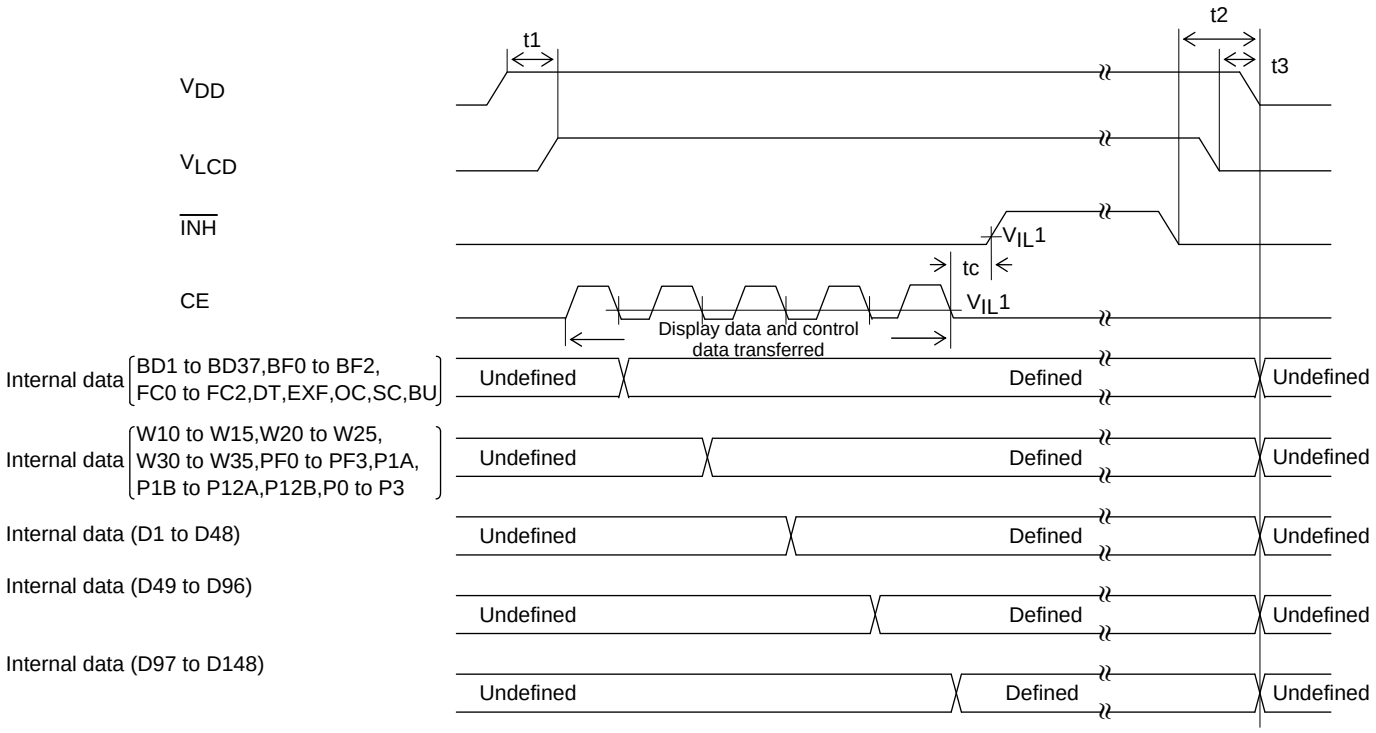
Since the LSI internal data (1/4 duty drive : the display data D1 to D148 and the control data, Static drive : the display data D1 to D37 and the control data) is undefined when power is first applied, applications should set the $\overline{INH}$ pin low at the same time as power is applied to turn off the display (This sets the S1/P1 to S12/P12, S13 to S36, COM4 to COM1, and S37/OSCI pins to the V_{SS} level.) and during this period send serial data from the controller. The controller should then set the $\overline{INH}$ pin high after the data transfer has completed. This procedure prevents meaningless display at power on.
(See Figure 4 and Figure 5.)

Notes on the Power On/Off Sequences

Applications should observe the following sequences when turning the LC75890 power on and off.
(See Figures 4 and Figure 5.)
• At power on : Logic block power supply (V_{DD}) on → LCD driver block power supply (V_{LCD}) on
• At power off : LCD driver block power supply (V_{LCD}) off → Logic block power supply (V_{DD}) off

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

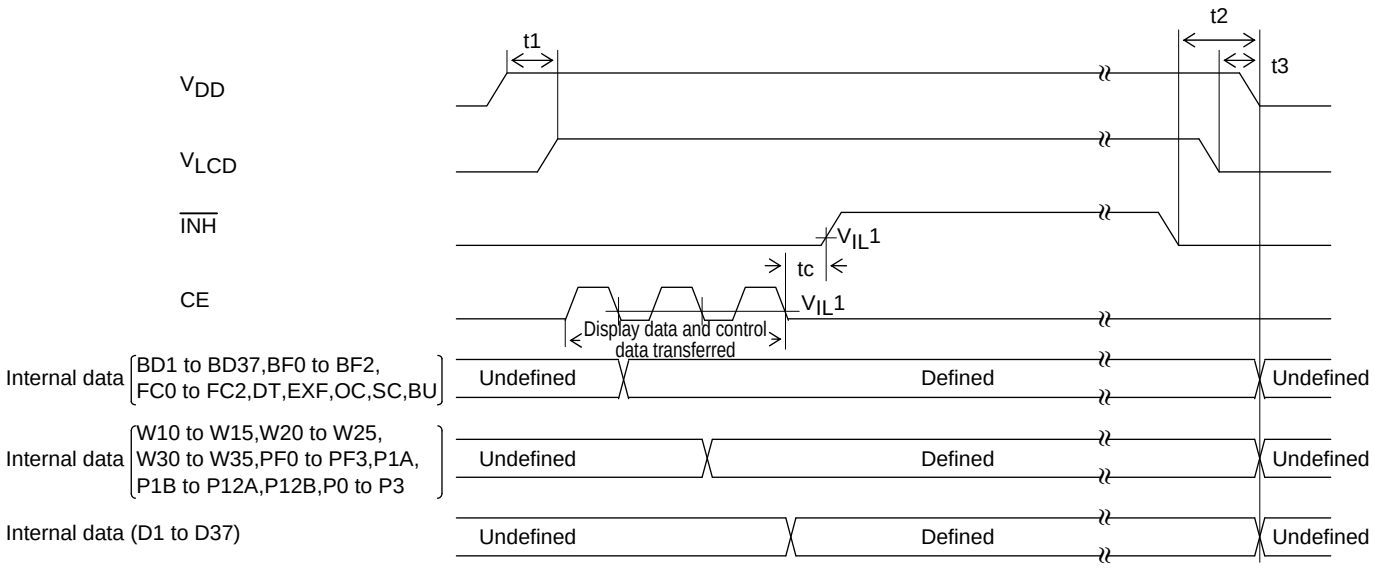
(1)1/4 duty drive



Note1 : t1≥0
t2>0
t3≥0 (t2>t3)
tc … 10 μs min

[Figure 4]

(2)Static drive



Note1 : t1≥0
t2>0
t3≥0 (t2>t3)
tc … 10 μs min

[Figure 5]

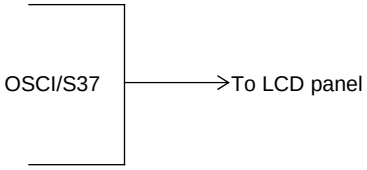
Notes on Controller Transfer of Display Data

When using the LC75890 in 1/4 duty, applications transfer the display data (D1 to D148) in three operations. In either case, applications should transfer all of the display data within 30 ms to maintain the quality of displayed image.

S37/OSCI Pin Peripheral Circuit

(1) Internal oscillator operating mode (control data OC = 0)

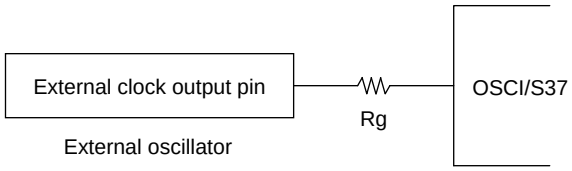
Connect the S37/OSCI pin to the LCD panel when the internal oscillator operating mode is selected.



(2) External clock operating mode (control data OC = 1)

When the external clock operating mode is selected, insert a current protection resistor Rg (2.2 to 22 kΩ) between the S37/OSCI pin and external clock output pin (external oscillator). Determine the value of the resistance according to the allowable current value at the external clock output pin. Also make sure that the waveform of the external clock is not heavily distorted.

In addition, the following conditions must be met : $V_{DD} \leq V_{LCD}$.

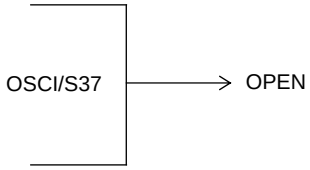


Note: Allowable current value at external clock output pin > $\frac{V_{LCD}}{Rg}$

$V_{DD} \leq V_{LCD}$

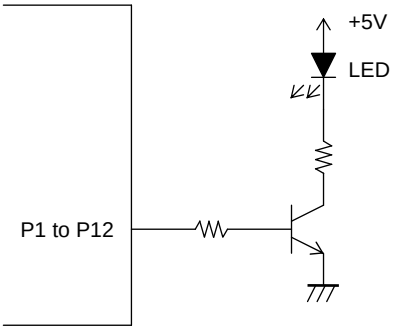
(3) Unused pin treatment

When the S37/OSCI pin is not to be used, select the internal oscillator operating mode (setting control data OC to 0) to keep the pin open.



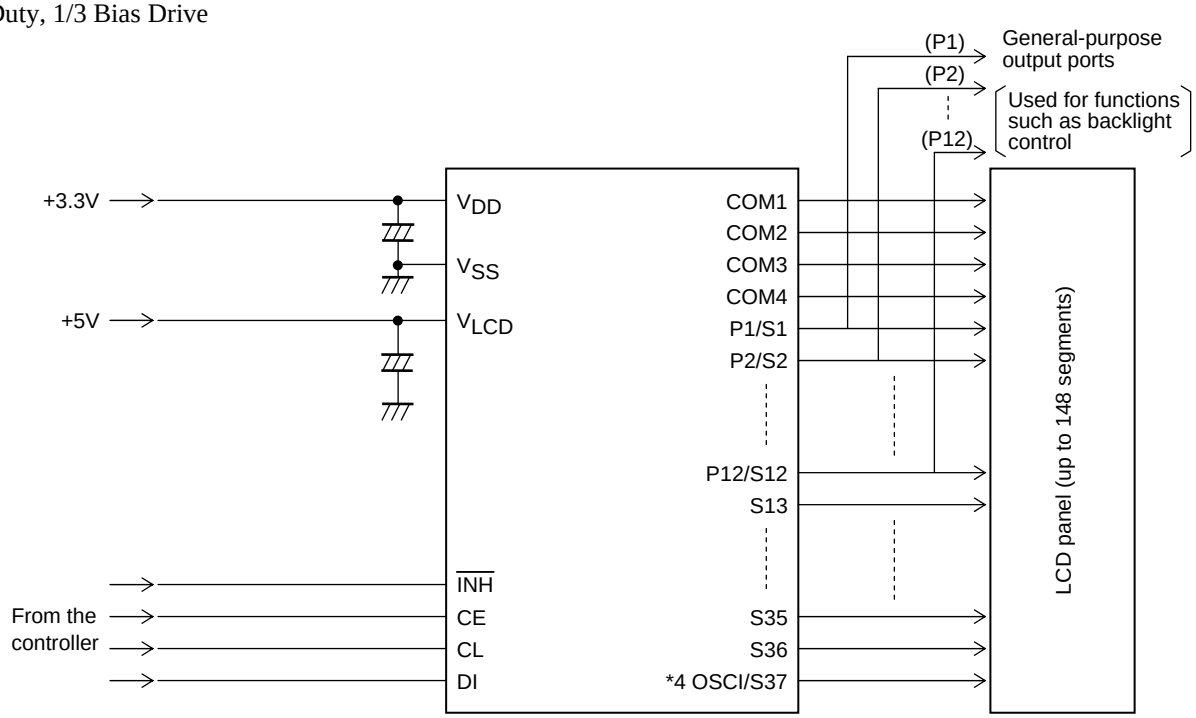
P1 to P12 pin peripheral circuit

It is recommended the circuit shown below be used to adjust the brightness of the LED backlight using the PWM output P1 to P12



Sample Applications Circuit 1

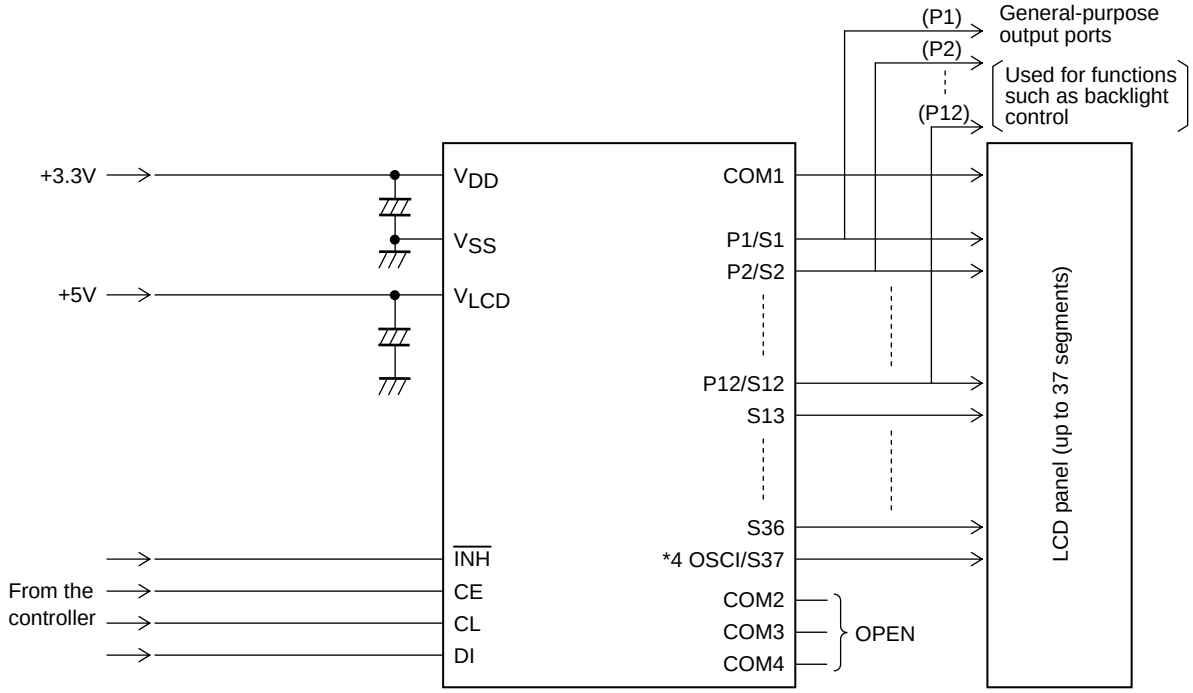
1/4 Duty, 1/3 Bias Drive



*4 Connect the S37/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg(2.2 to 22 kΩ) between the S37/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode. (See “S37/OSCI Pin Peripheral Circuit”)

Sample Applications Circuit 2

Static Drive



*4 Connect the S37/OSCI pin to the LCD panel in the internal oscillator operating mode and insert a current protection resistor Rg(2.2 to 22 kΩ) between the S37/OSCI pin and external clock output pin (external oscillator) in the external clock operating mode. (See “S37/OSCI Pin Peripheral Circuit”)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC75890W-2H	SQFP80 12x12 / SQFP80 (Pb-Free / Halogen Free)	1250 / Tray JEDEC
LC75890W-NH	SQFP80 12x12 / SQFP80 (Pb-Free / Halogen Free)	1000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D. http://www.onsemi.com/pub_link/Collateral/BRD8011-D.PDF