

# Memory FRAM

## 64 K (8 K × 8) Bit SPI

# MB85RS64

### ■ DESCRIPTION

MB85RS64 is a FRAM (Ferroelectric Random Access Memory) chip in a configuration of 8,192 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

MB85RS64 adopts the Serial Peripheral Interface (SPI).

The MB85RS64 is able to retain data without using a back-up battery, as is needed for SRAM.

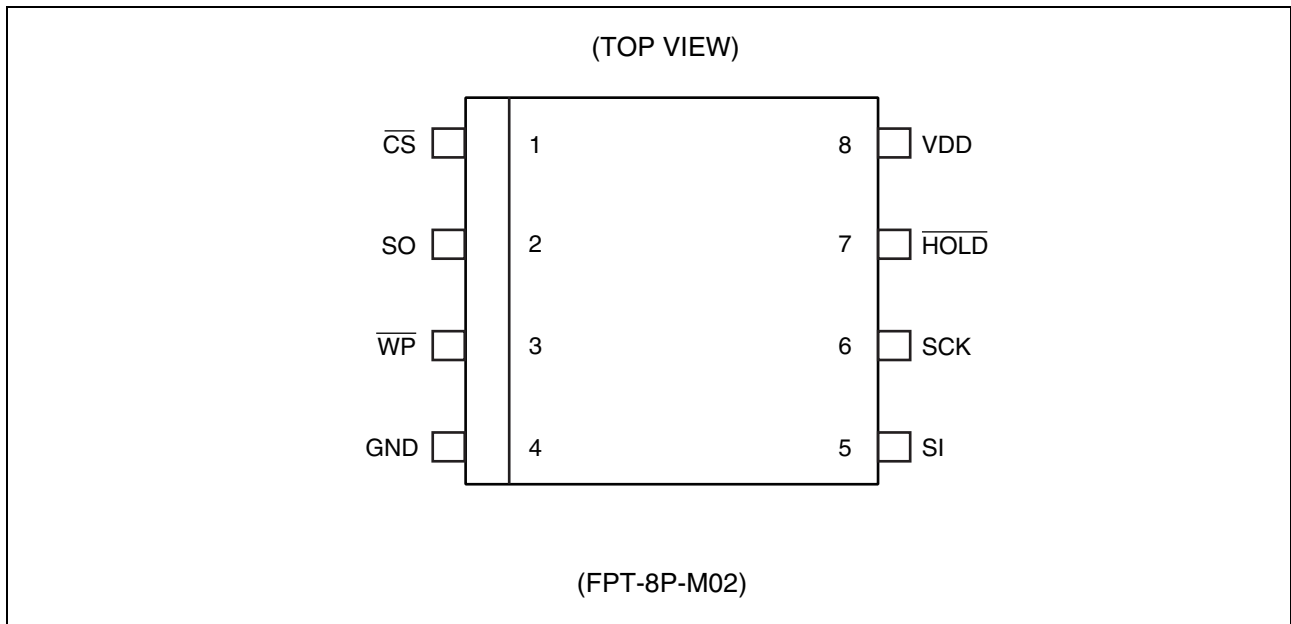
The memory cells used in the MB85RS64 can be used for  $10^{10}$  read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E<sup>2</sup>PROM.

MB85RS64 does not take long time to write data unlike Flash memories nor E<sup>2</sup>PROM, and MB85RS64 takes no wait time.

### ■ FEATURES

- Bit configuration : 8,192 words × 8 bits
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)  
Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Operating frequency : 20 MHz (Max)
- High endurance : 10 Billion Read/writes
- Data retention : 10 years (+85 °C)
- Operating power supply voltage : 2.7 V to 3.6 V
- Low power consumption : Operating power supply current 1.5(TBD)mA (Typ@20 MHz)  
Standby current 10 μA(TBD) (Typ)
- Operation ambient temperature range : - 40 °C to +85 °C
- Package : 8-pin plastic SOP (FPT-8P-M02) RoHS compliant

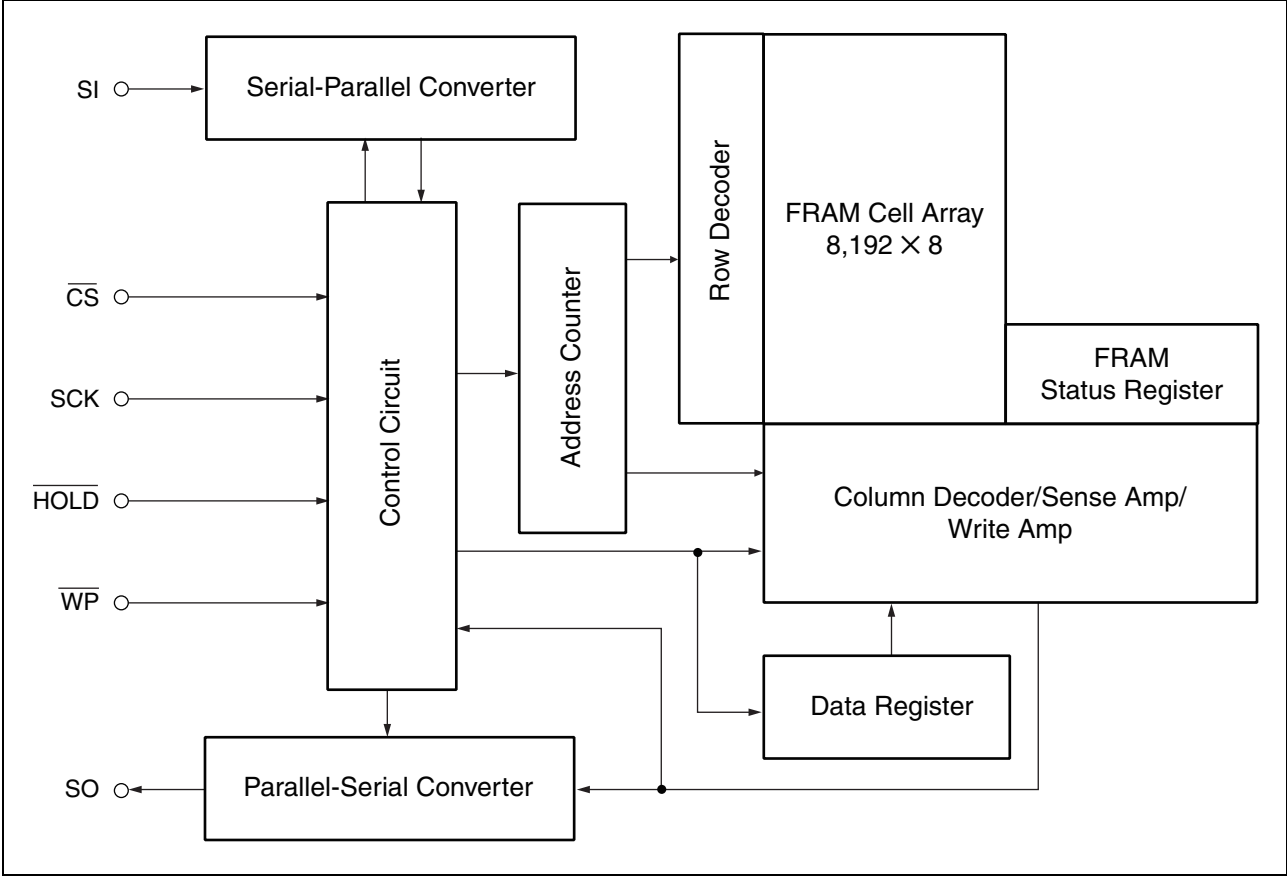
■ PIN ASSIGNMENT



■ PIN FUNCTIONAL DESCRIPTIONS

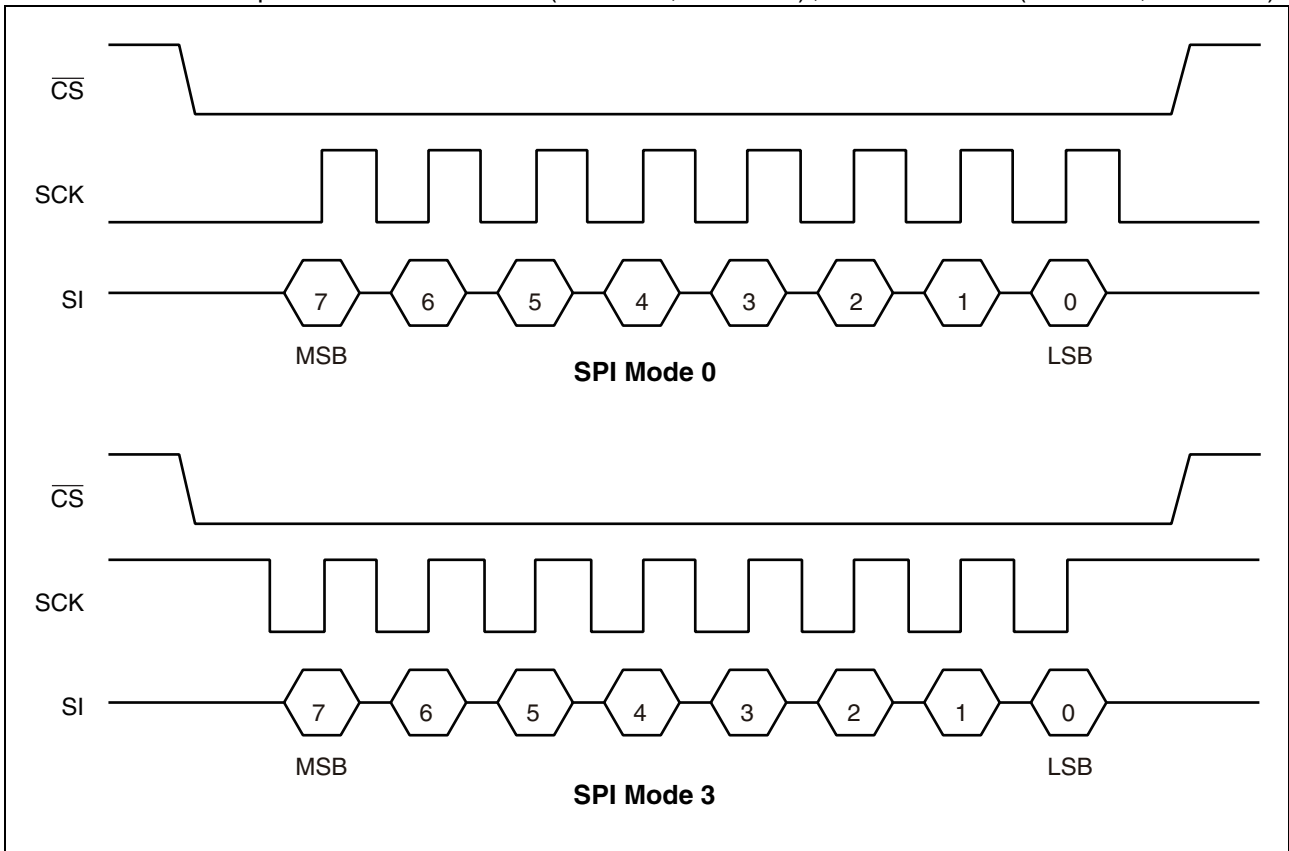
Pin No.	Pin Name	Functional description
1	$\overline{CS}$	Chip Select pin This is an input pin to make chips select. When $\overline{CS}$ is the "H" level, device is in deselect (standby) status as long as device is not write status internally, and SO becomes High-Z. Inputs from other pins are ignored at this time. When $\overline{CS}$ is the "L" level, device is in select (active) status. $\overline{CS}$ has to be the "L" level before inputting op-code. The Chip Select pin is pulled up internally to the VDD pin.
3	$\overline{WP}$	Write Protect pin This is a pin to control writing to a status register. When $\overline{WP}$ is the "L" level, writing to a status register is not operated.
7	$\overline{HOLD}$	Hold pin This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is the "L" level, hold operation is activated, SO becomes High-Z, SCK and SI become don't care. While the hold operation, $\overline{CS}$ has to be retained the "L" level.
6	SCK	Serial Clock pin This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge.
5	SI	Serial Data Input pin This is an input pin of serial data. This inputs op-code, address, and writing data.
2	SO	Serial Data Output pin This is an output pin of serial data. Reading data of FRAM memory cell array and status register data are output. This is High-Z during standby.
8	VDD	Supply Voltage pin
4	GND	Ground pin

■ BLOCK DIAGRAM



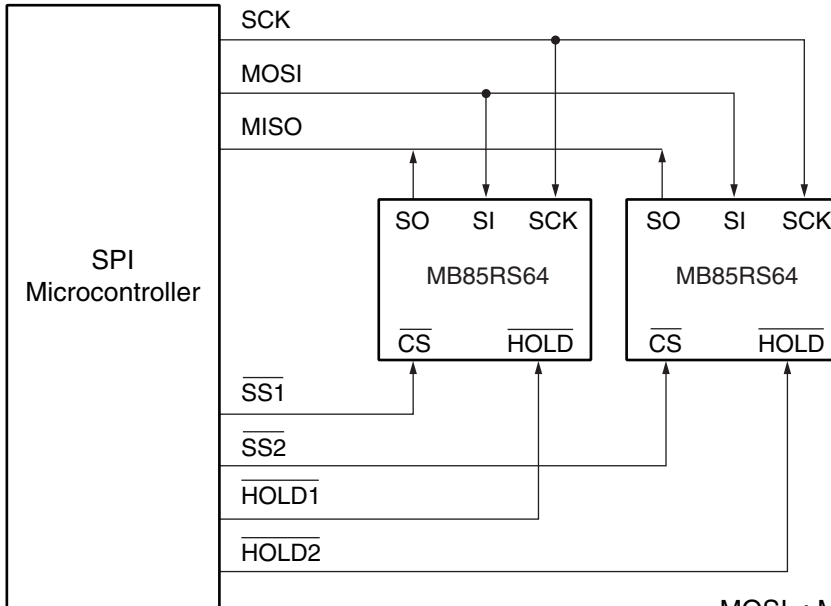
## ■ SPI MODE

MB85RS64 corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0), and SPI mode 3 (CPOL = 1, CPHA = 1).



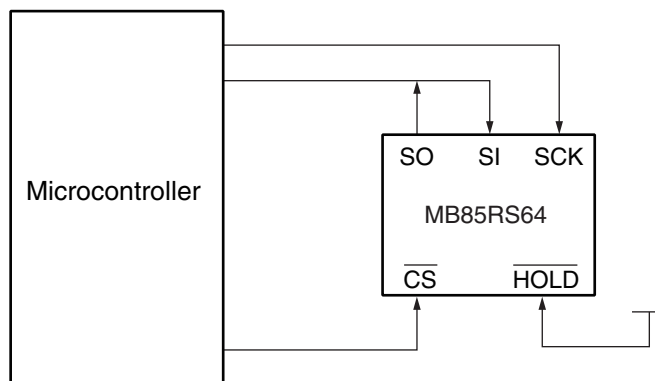
■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85RS64 works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.



MOSI : Master Out Slave In  
 MISO : Master In Slave Out  
 SS : Slave Select

System Configuration with SPI Port



System Configuration without SPI Port

■ STATUS REGISTER

Bit No.	Bit Name	Function
7	WPEN	Status Register Write Protect This is a bit composed of nonvolatile memories (FRAM). WPEN protects writing to a status register (see “■ WRITING PROTECT”) relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible.
6 to 4	—	Not Used Bits These are bits composed of nonvolatile memories, writing with the WRSR command is possible, and “000” is written before shipment. These bits are not used but they are read with the RDSR command.
3	BP1	Block Protect This is a bit composed of nonvolatile memory. This defines block size for writing protect with the WRITE command (see “■ BLOCK PROTECT”). Writing with the WRSR command and reading with the RDSR command are possible.
2	BP0	
1	WEL	Write Enable Latch This indicates FRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations. The time when power is up. The time when the WRDI command is input. The time when the WRSR command is input. The time when the WRITE command is input.
0	0	This is a bit fixed to “0”.

■ OP-CODE

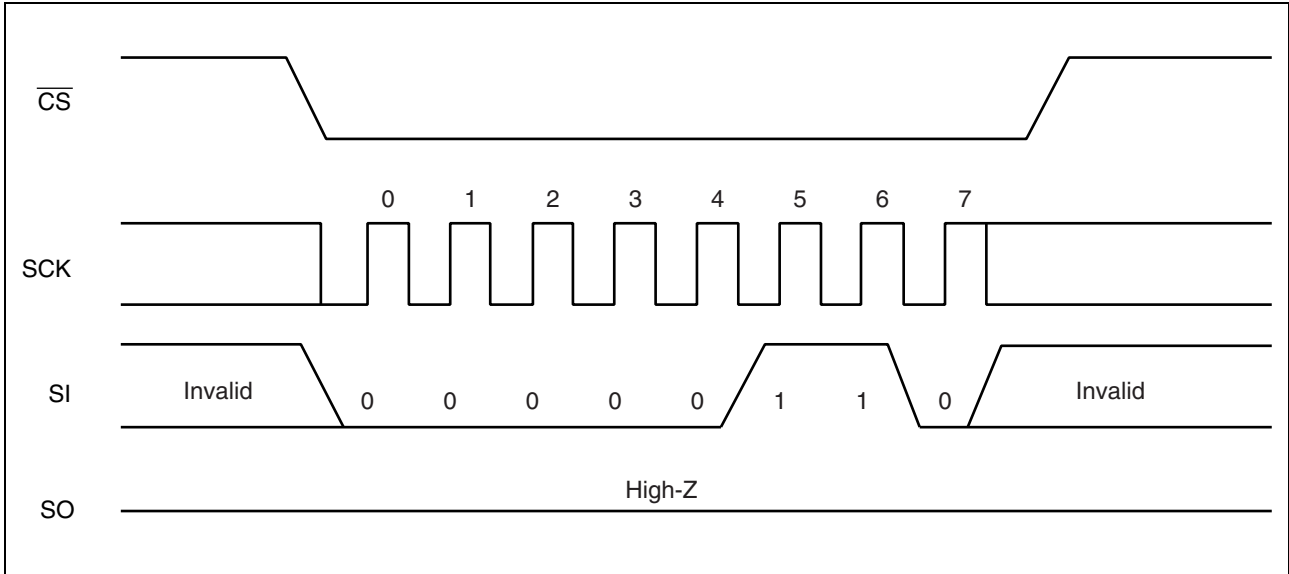
MB85RS64 accepts 6 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If  $\overline{CS}$  is risen while inputting op-code, the command are not performed.

Name	Description	Op-code
WREN	Set Write Enable Latch	0000 0110 <sub>B</sub>
WRDI	Reset Write Enable Latch	0000 0100 <sub>B</sub>
RDSR	Read Status Register	0000 0101 <sub>B</sub>
WRSR	Write Status Register	0000 0001 <sub>B</sub>
READ	Read Memory Code	0000 0011 <sub>B</sub>
WRITE	Write Memory Code	0000 0010 <sub>B</sub>

■ COMMAND

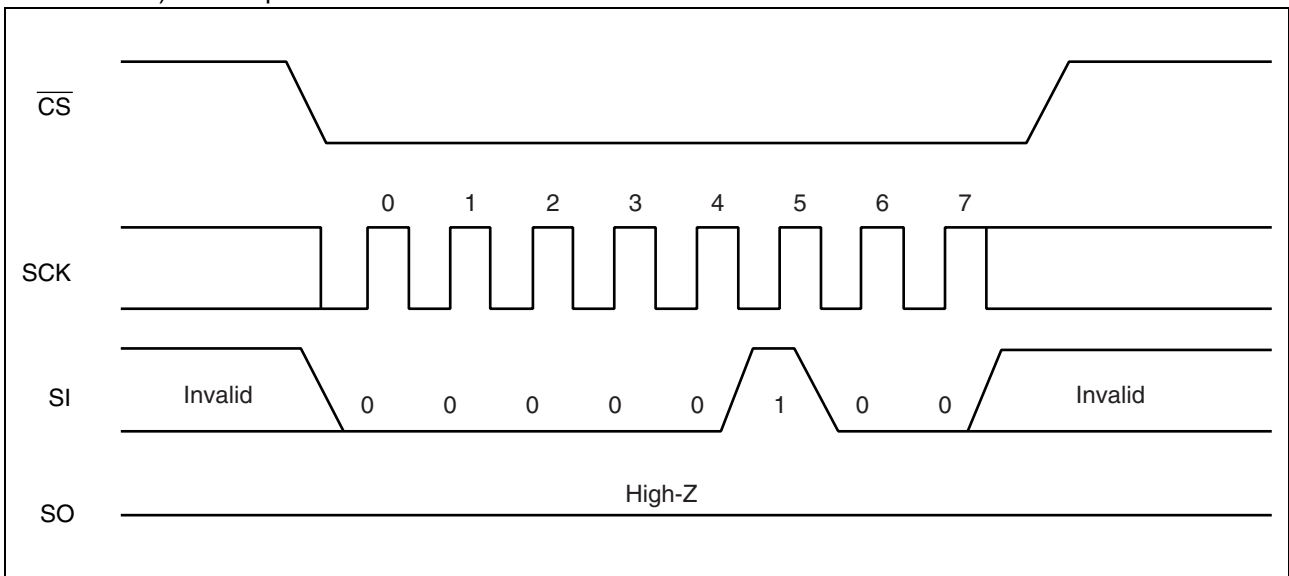
• WREN

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .



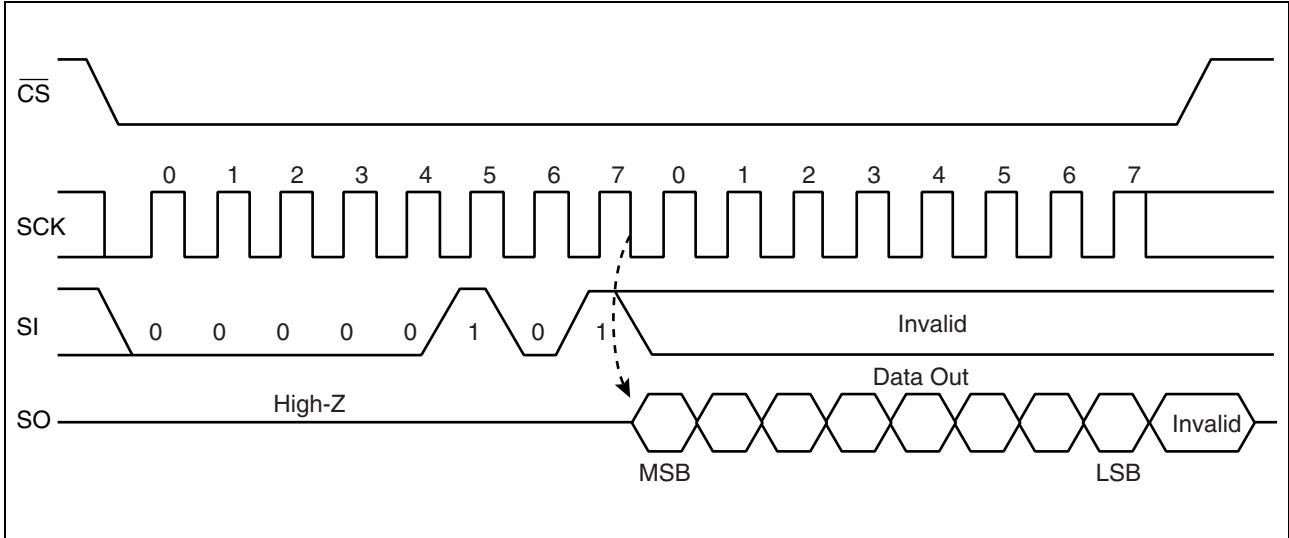
• WRDI

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRITE command and WRSR command) are not performed when WEL is reset.



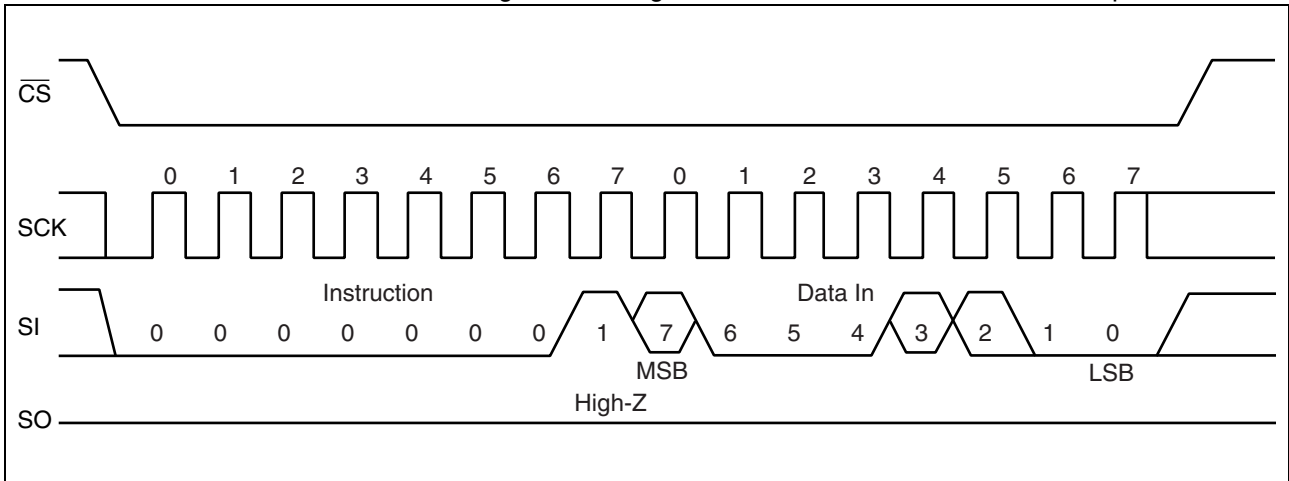
• RDSR

The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. Continuously reading status register is enabled by keep on sending SCK before rising  $\overline{CS}$  with the RDSR command.



• WRSR

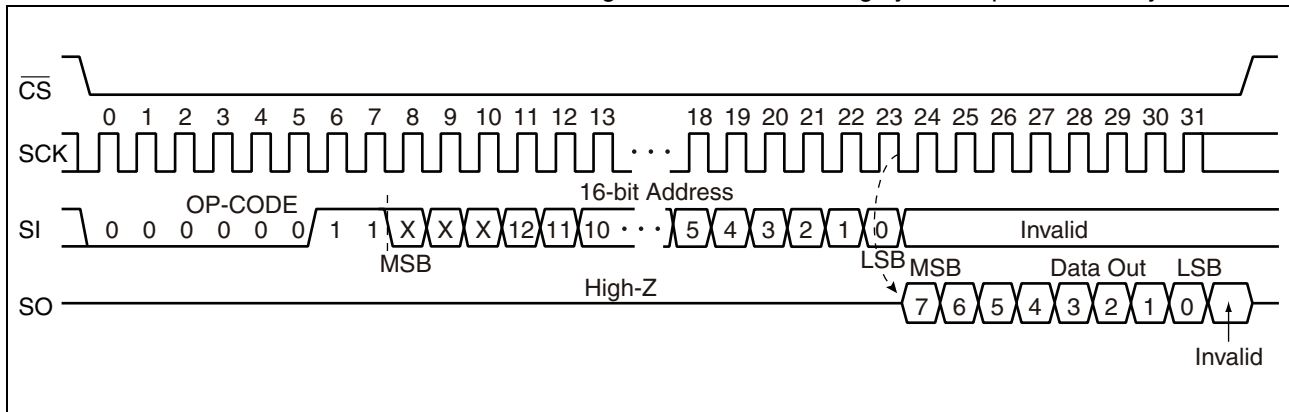
The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register is fixed to "0" and cannot be written. The SI value corresponding to bit 0 is ignored. the  $\overline{WP}$  signal level shall be fixed before performing the WRSR command, and do not change the  $\overline{WP}$  signal level until the end of command sequence.





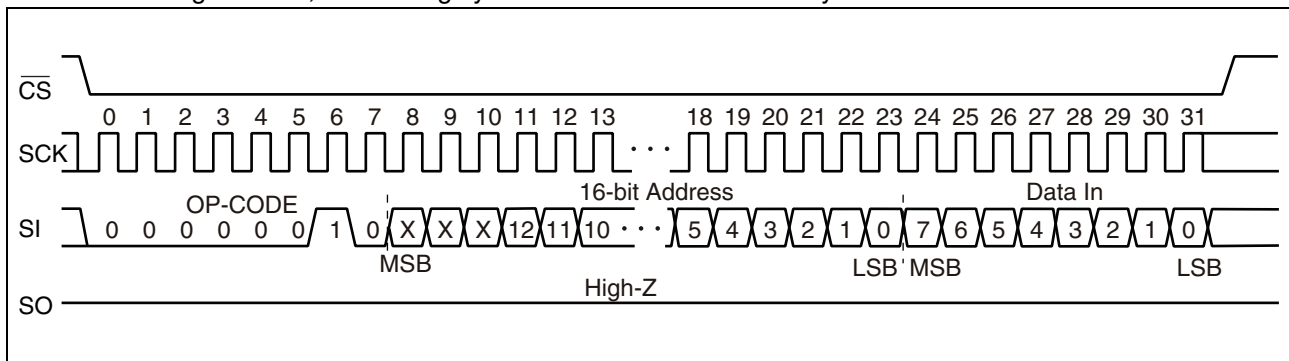
• READ

The READ command reads FRAM memory cell array data. Arbitrary 16 bits address and op-code of READ are input to SI. The 3-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When  $\overline{CS}$  is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clock for 8 cycles each to SCK before  $\overline{CS}$  is risen. When it reaches the most significant address, it rolls over to come back to the starting address, and reading cycle keeps on infinitely.



• WRITE

The WRITE command writes data to FRAM memory cell array. WRITE op-code, arbitrary 16 bits of address and 8 bits of writing data are input to SI. The most significant address bit is invalid. When 8 bits of writing data is input, data is written to FRAM memory cell array. Risen  $\overline{CS}$  will terminate the WRITE command, but if you continue sending the writing data for 8 bits each before  $\overline{CS}$  is risen, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over, comes back to the starting address, and writing cycle can be continued infinitely.



■ BLOCK PROTECT

Writing protect block is configured by the WRITE command with BP1, BP0 value of the status register.

BP1	BP0	Protected Block
0	0	None
0	1	1800 <sub>H</sub> to 1FFF <sub>H</sub> (upper 1/4)
1	0	1000 <sub>H</sub> to 1FFF <sub>H</sub> (upper 1/2)
1	1	0000 <sub>H</sub> to 1FFF <sub>H</sub> (all)

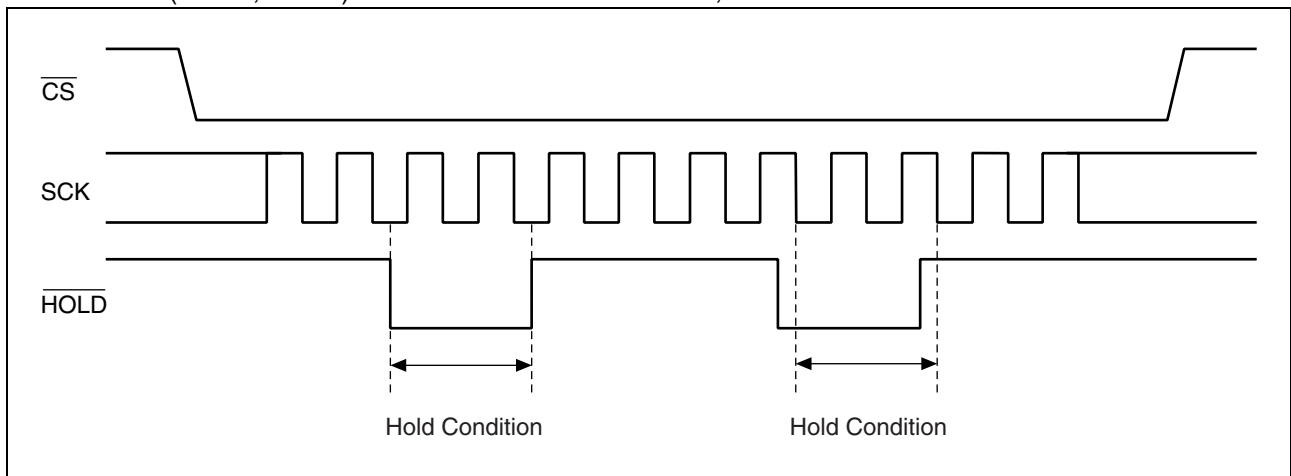
■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, WP as shown in the table.

WEL	WPEN	WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

■ HOLD OPERATION

Hold status is retained without aborting a command if  $\overline{\text{HOLD}}$  is the "L" level while  $\overline{\text{CS}}$  is the "L" level. The timing for starting and ending hold status depends on the SCK to be the "H" level or the "L" level when a HOLD pin input is transited to the hold condition as shown in the diagram below. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become don't care. And, SO becomes High-Z while reading command (RDSR, READ). If  $\overline{\text{CS}}$  is risen with hold status, a command is aborted and device is reset.



## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	$V_{DD}$	- 0.5	+ 4.0	V
Input voltage*	$V_{IN}$	- 0.5	$V_{DD} + 0.5$	V
Output voltage*	$V_{OUT}$	- 0.5	$V_{DD} + 0.5$	V
Operation ambient temperature	$T_A$	- 40	+ 85	°C
Storage temperature	$T_{stg}$	- 40	+ 125	°C

\*:These parameters are based on the condition that  $V_{SS}$  is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	$V_{DD}$	2.7	3.3	3.6	V
Input high voltage*	$V_{IH}$	$V_{DD} \times 0.8$	—	$V_{DD} + 0.3$	V
Input low voltage*	$V_{IL}$	- 0.5	—	$V_{DD} \times 0.2$	V
Operation ambient temperature	$T_A$	- 40	—	+ 85	°C

\*:These parameters are based on the condition that  $V_{SS}$  is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current	I <sub>Lil</sub>	$\overline{CS} = 0\text{ V to }V_{DD}$	—	—	200	μA
		$\overline{WP}, \overline{HOLD}, SCK, SI = 0\text{ V to }V_{DD}$	—	—	10	
Output leakage current	I <sub>Lol</sub>	$V_{OUT} = 0\text{ V to }V_{DD}$	—	—	10	μA
Operating power supply current	I <sub>DD</sub>	SCK = 20 MHz	—	1.5 (TBD)	2.0 (TBD)	mA
Standby current	I <sub>SB</sub>	SCK = SI = $\overline{CS} = V_{DD}$	—	10 (TBD)	15 (TBD)	μA
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA	$V_{DD} - 0.5$	—	$V_{DD}$	V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA	$V_{SS}$	—	0.4	V

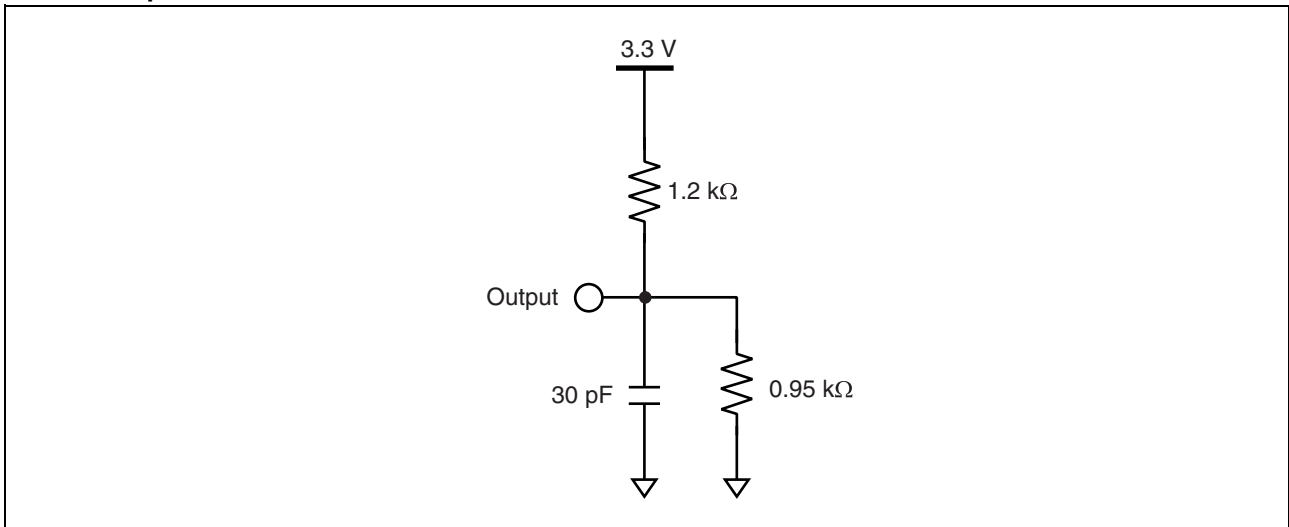
## 2. AC Characteristics

Parameter	Symbol	Value		Unit
		Min	Max	
SCK clock frequency	f <sub>CK</sub>	0	20	MHz
Clock high time	t <sub>CH</sub>	25	—	ns
Clock low time	t <sub>CL</sub>	25	—	ns
Chip select set up time	t <sub>CSU</sub>	10	—	ns
Chip select hold time	t <sub>CSH</sub>	10	—	ns
Output disable time	t <sub>OD</sub>	—	20	ns
Output data valid time	t <sub>ODV</sub>	—	18	ns
Output hold time	t <sub>OH</sub>	0	—	ns
Deselect time	t <sub>D</sub>	60	—	ns
Data in rise time	t <sub>R</sub>	—	50	ns
Data fall time	t <sub>F</sub>	—	50	ns
Data set up time	t <sub>SU</sub>	5	—	ns
Data hold time	t <sub>H</sub>	5	—	ns
$\overline{\text{HOLD}}$ set up time	t <sub>HS</sub>	10	—	ns
$\overline{\text{HOLD}}$ hold time	t <sub>HH</sub>	10	—	ns
$\overline{\text{HOLD}}$ output floating time	t <sub>HZ</sub>	—	20	ns
$\overline{\text{HOLD}}$ output active time	t <sub>LZ</sub>	—	20	ns

## AC Test Condition

Power supply voltage : 2.7 V to 3.6 V  
 Operation ambient temperature : - 40 °C to + 85 °C  
 Input voltage magnitude : 0.3 V to 2.7 V  
 Input rising time : 5 ns  
 Input falling time : 5 ns  
 Input judge level : V<sub>DD</sub>/2  
 Output judge level : V<sub>DD</sub>/2

AC Load Equivalent Circuit

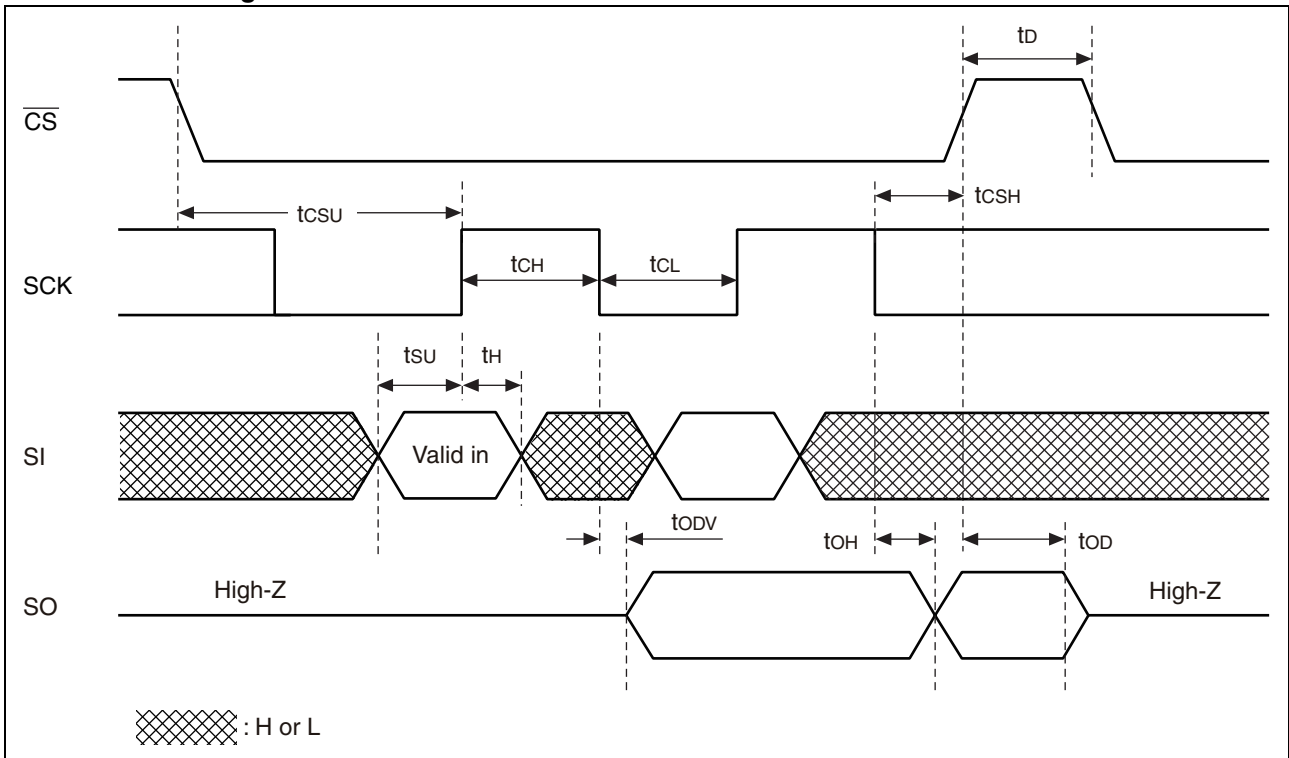


3. Pin Capacitance

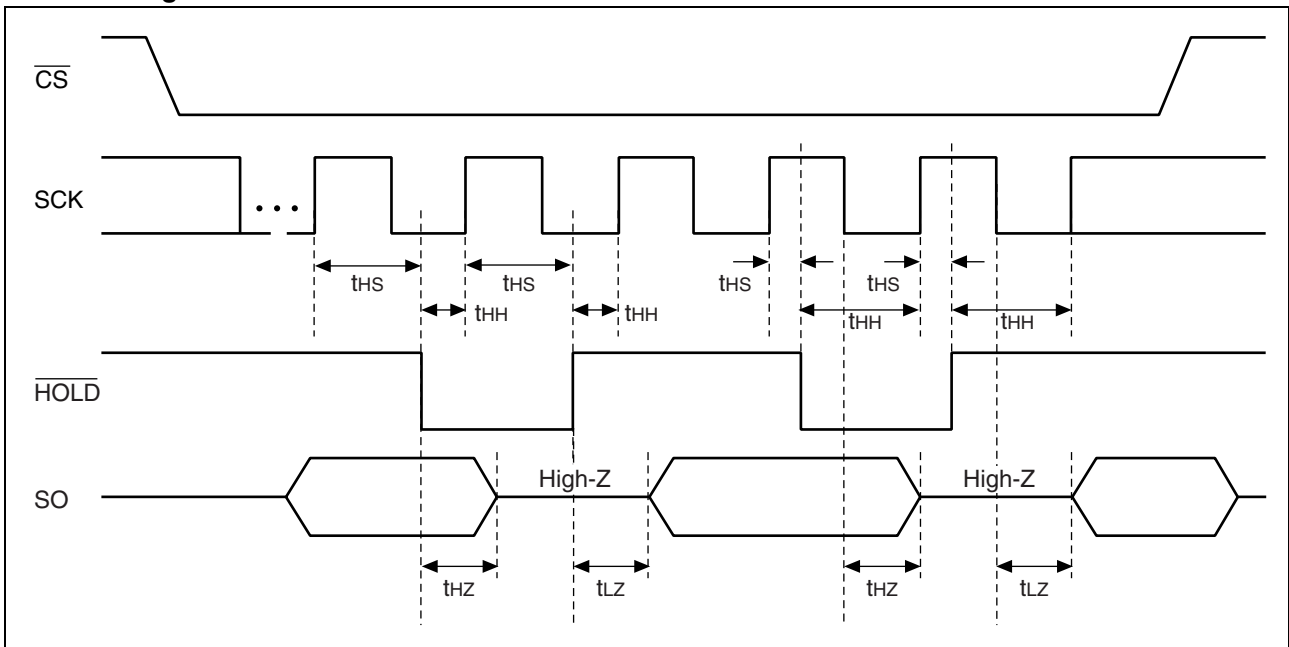
Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
Output capacitance	$C_o$	VDD = V <sub>IN</sub> = V <sub>OUT</sub> = 0 V f = 1 MHz, T <sub>A</sub> = +25 °C	—	10	pF
Input capacitance	$C_i$		—	10	pF

■ TIMING DIAGRAM

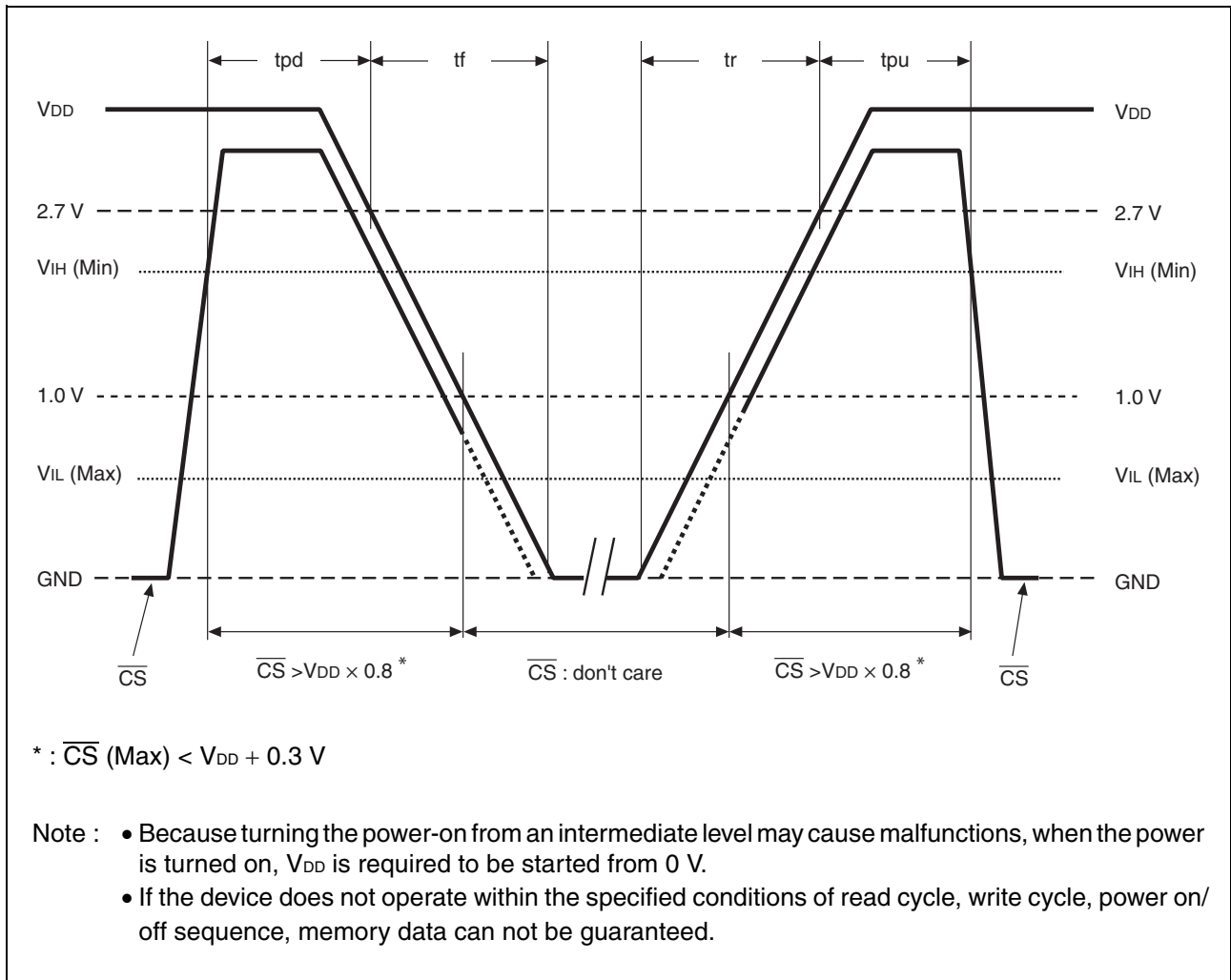
• Serial Data Timing



• Hold Timing



## ■ POWER ON/OFF SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
$\overline{CS}$ level hold time at power OFF	tpd	400	—	ns
$\overline{CS}$ level hold time at power ON	tpu	0.1	—	ms
Power supply falling time	tf	100	—	$\mu\text{s/V}$
Power supply rising time	tr	30	—	$\mu\text{s/V}$

## ■ NOTES ON USE

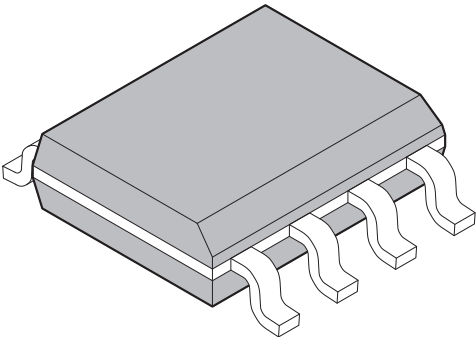
Data written before performing IR reflow is not guaranteed after IR reflow.



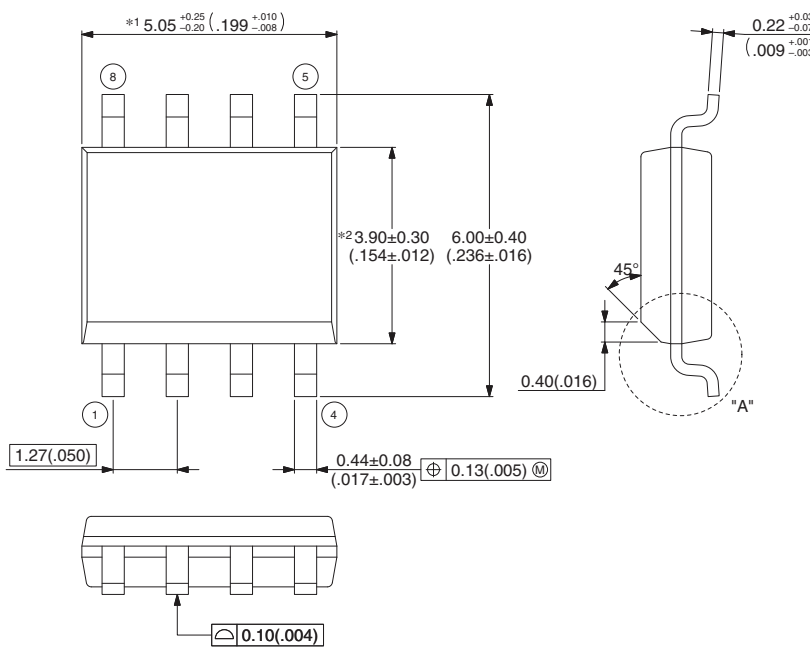
## ■ ORDERING INFORMATION

Part number	Package	Shipping form	Minimum shipping quantity
MB85RS64PNF-G-JNE1	8-pin plastic SOP (FPT-8P-M02)	Tube	1
MB85RS64PNF-G-JNERE1	8-pin plastic SOP (FPT-8P-M02)	Embossed Carrier tape	1500

## ■ PACKAGE DIMENSION

<p>8-pin plastic SOP</p>  <p>(FPT-8P-M02)</p>	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g

8-pin plastic SOP  
(FPT-8P-M02)



Top view dimensions:  
 \*1 5.05<sup>+0.25</sup>/<sub>-0.20</sub> (.199<sup>+0.010</sup>/<sub>-0.008</sub>)  
 \*2 3.90±0.30 (.154±.012) 6.00±0.40 (.236±.016)  
 Lead pitch: 1.27(.050)  
 Lead width: 0.44±0.08 (.017±.003) ⊕ 0.13(.005) ⊙  
 Lead thickness: 0.10(.004)

Lead detail dimensions:  
 Lead width: 0.22<sup>+0.03</sup>/<sub>-0.07</sub> (.009<sup>+0.001</sup>/<sub>-0.003</sub>)  
 Lead angle: 45°  
 Lead thickness: 0.40(.016)

Details of "A" part:  
 Mounting height: 1.55±0.20 (.061±.008)  
 Lead thickness: 0.25(.010)  
 Lead angle: 0~8°  
 Stand off: 0.15±0.10 (.006±.004)  
 Lead width: 0.50±0.20 (.020±.008)  
 Lead thickness: 0.60±0.15 (.024±.006)

Note 1) \*1 : These dimensions include resin protrusion.  
 Note 2) \*2 : These dimensions do not include resin protrusion.  
 Note 3) Pins width and pins thickness include plating thickness.  
 Note 4) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches).  
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.  
<http://edevice.fujitsu.com/package/en-search/>

**MEMO**

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