NTD4813NH, NVD4813NH

Power MOSFET
30 V, 40 A, Single N−Channel, DPAK/IPAK

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Low R_G
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- CPU Power Delivery
- DC−DC Converters
- High Side Switching

MARKING DIAGRAM & PIN ASSIGNMENT

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
30 V	13 mΩ @ 10 V	40 A
	25.9 mΩ @ 4.5 V	

N−Channel

DPAK
CASE 369AA
(Bent Lead)
STYLE 2

A = Assembly Location*
Y = Year
WW = Work Week
4813NH = Device Code
G = Pb−Free Package

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

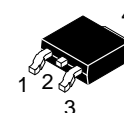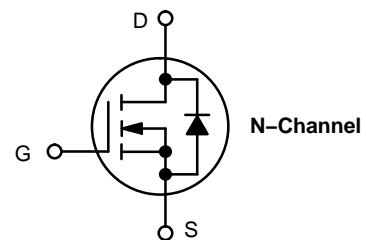| Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{θJA}$ (Note 1)	Steady State	T_A = 25°C	I_D	9.0	A
		T_A = 85°C		7.0	
Power Dissipation $R_{θJA}$ (Note 1)		T_A = 25°C	P_D	1.94	W
Continuous Drain Current $R_{θJA}$ (Note 2)		T_A = 25°C	ID	7.6	A
		T_A = 85°C		5.9	
Power Dissipation $R_{θJA}$ (Note 2)		T_A = 25°C	P_D	1.27	W
Continuous Drain Current $R_{θJC}$ (Note 1)		T_C = 25°C	I_D	40	A
		T_C = 85°C		31	
Power Dissipation $R_{θJC}$ (Note 1)		T_C = 25°C	P_D	35.3	W
Pulsed Drain Current	t_p=10μs	T_A = 25°C	I_{DM}	90	A
Current Limited by Package		T_A = 25°C	$I_{DmaxPkg}$	35	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +175	°C
Source Current (Body Diode)			I_S	29	A
Drain to Source dV/dt			dV/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 24 V, V_{GS} = 10 V, I_L = 17.2 A_{pk}, L = 0.3 mH, R_G = 25 Ω)			EAS	44.4	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
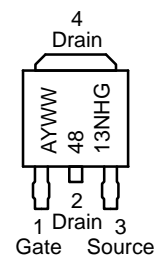
September, 2014 − Rev. 4

1

Publication Order Number:
NTD4813NH/D

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction–to–Case (Drain)	$R_{\theta JC}$	4.25	°C/W
Junction–to–TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction–to–Ambient – Steady State (Note 1)	$R_{\theta JA}$	77.5	
Junction–to–Ambient – Steady State (Note 2)	$R_{\theta JA}$	118.5	

1. Surface–mounted on FR4 board using 1 sq–in pad, 1 oz Cu.
2. Surface–mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		30			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				24.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V	T_J = 25 °C			1	μA
			T_J = 125°C			10	
Gate–to–Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				5.4		mV/°C
Drain–to–Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V to 11.5 V	I_D = 30 A		10.9	13	mΩ
			I_D = 15 A		10.7		
		V_{GS} = 4.5 V	I_D = 30 A		20.9	25.9	
			I_D = 15 A		18.5		
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 10 A			6.7		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 12 V			940		pF
Output Capacitance	C_{OSS}				201		
Reverse Transfer Capacitance	C_{RSS}				115		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 15 V; I_D = 30 A			7.1	10	nC
Threshold Gate Charge	$Q_{G(TH)}$				1.6		
Gate–to–Source Charge	Q_{GS}				3.4		
Gate–to–Drain Charge	Q_{GD}				3.0		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 11.5 V, V_{DS} = 15 V; I_D = 30 A			18.2		nC
SWITCHING CHARACTERISTICS (Note 4)							
Turn–On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			10		ns
Rise Time	t_r				19.5		
Turn–Off Delay Time	$t_{d(OFF)}$				10.3		
Fall Time	t_f				2.9		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

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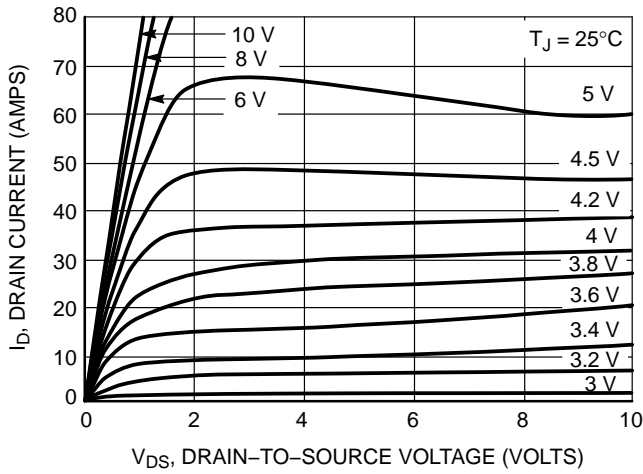**ELECTRICAL CHARACTERISTICS** (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (Note 4)							
Turn–On Delay Time	$t_{d(ON)}$	V_{GS} = 11.5 V, V_{DS} = 15 V, I_D = 15 A, R_G = 3.0 Ω			5.1		ns
Rise Time	t_r				16.1		
Turn–Off Delay Time	$t_{d(OFF)}$				17.2		
Fall Time	t_f				1.8		
DRAIN–SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 30 A	T_J = 25°C		0.95	1.2	V
			T_J = 125°C		0.9		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIs/dt = 100 A/μs, I_S = 30 A			15		ns
Charge Time	t_a				9.9		
Discharge Time	t_b				5.1		
Reverse Recovery Charge	Q_{RR}				7.0		nC
PACKAGE PARASITIC VALUES							
Source Inductance	L_S	T_A = 25°C			2.49		nH
Drain Inductance, DPAK	L_D				0.0164		
Drain Inductance, IPAK	L_D				1.88		
Gate Inductance	L_G				3.46		
Gate Resistance	R_G				0.55		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

Figure 1. On–Region Characteristics
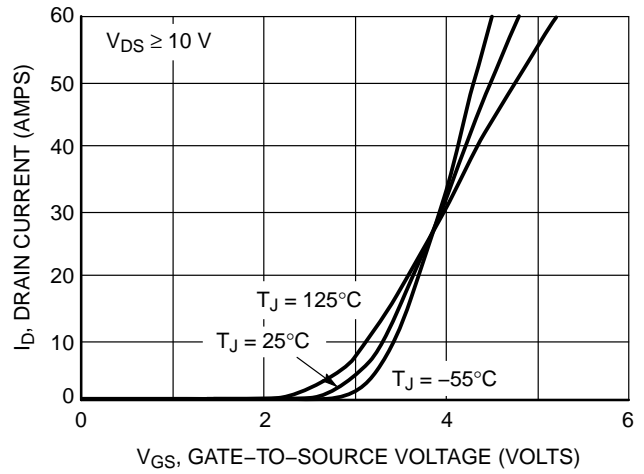
Figure 2. Transfer Characteristics
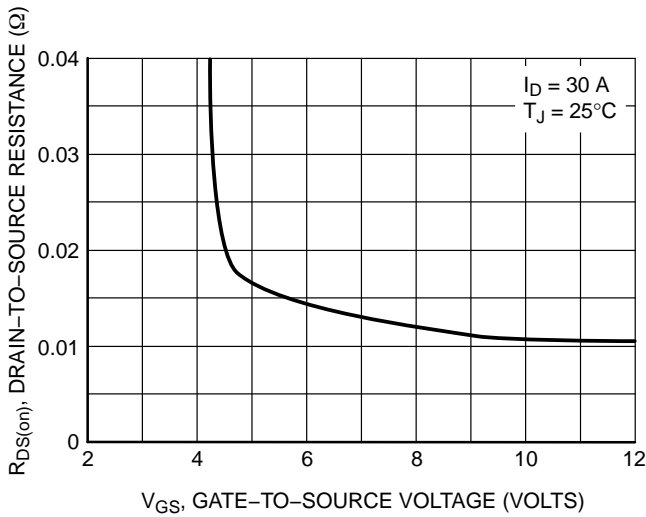
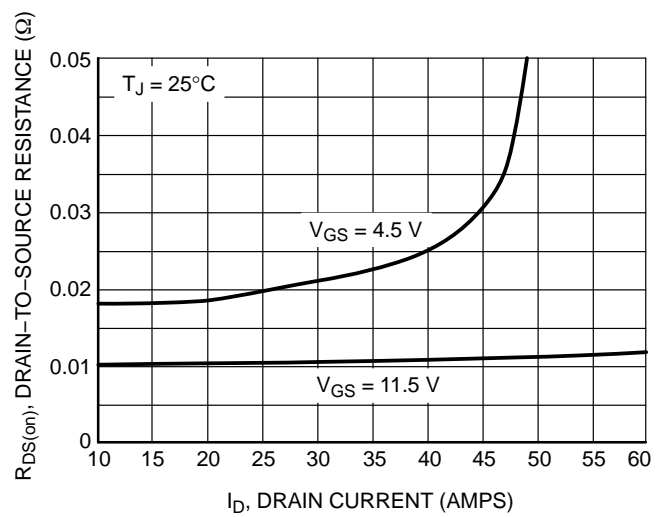**Figure 3. On–Resistance vs. Gate–to–Source Voltage**
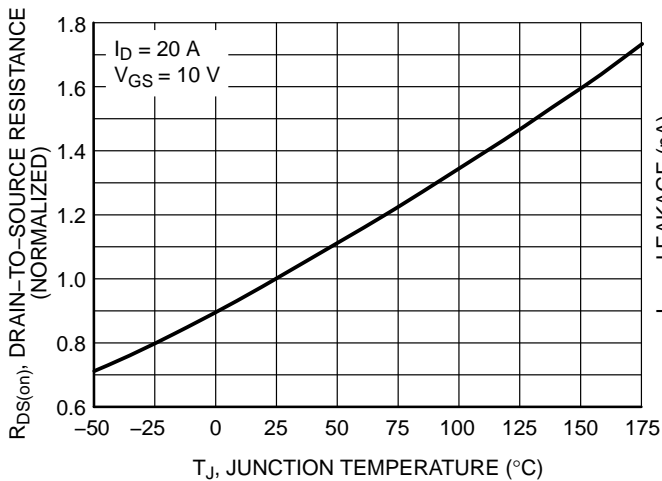
Figure 4. On–Resistance vs. Drain Current and Gate Voltage
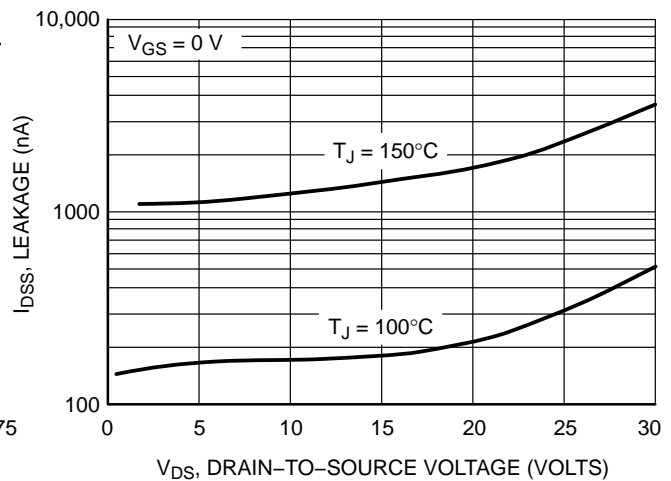
Figure 5. On–Resistance Variation with Temperature

Figure 6. Drain–to–Source Leakage Current vs. Drain Voltage
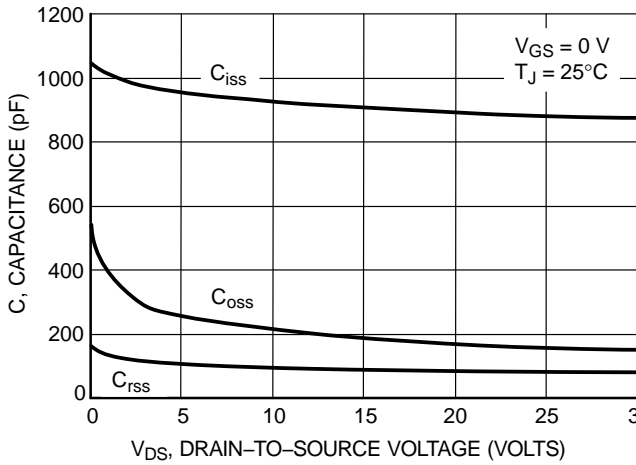
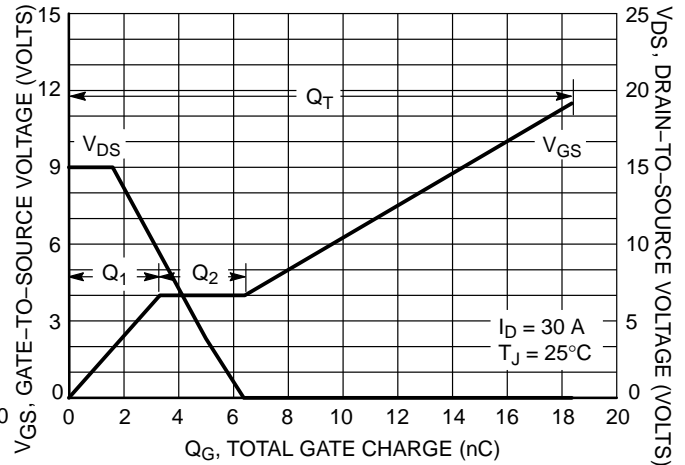## TYPICAL PERFORMANCE CURVES

Figure 7. Capacitance Variation

$V_{GS} = 0$ V
$T_J = 25°C$

C, CAPACITANCE (pF) vs V_{DS}, DRAIN–TO–SOURCE VOLTAGE (VOLTS)

C_{iss}
C_{oss}
C_{rss}

Figure 8. Gate–To–Source and Drain–To–Source Voltage vs. Total Charge

V_{GS}, GATE–TO–SOURCE VOLTAGE (VOLTS) and V_{DS}, DRAIN–TO–SOURCE VOLTAGE (VOLTS) vs Q_G, TOTAL GATE CHARGE (nC)

Q_T
V_{DS}
V_{GS}
Q_1
Q_2
$I_D = 30$ A
$T_J = 25°C$
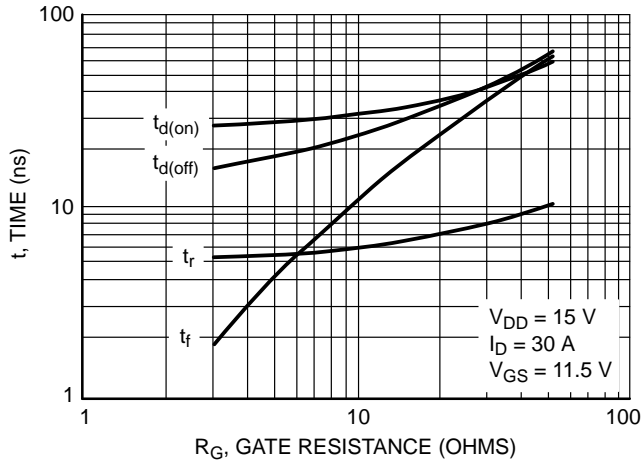
Figure 9. Resistive Switching Time Variation vs. Gate Resistance

t, TIME (ns) vs R_G, GATE RESISTANCE (OHMS)

$t_{d(on)}$
$t_{d(off)}$
t_r
t_f
$V_{DD} = 15$ V
$I_D = 30$ A
$V_{GS} = 11.5$ V
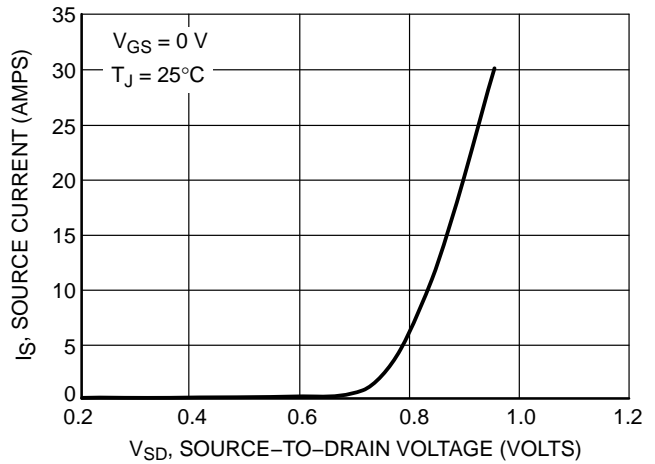
Figure 10. Diode Forward Voltage vs. Current

I_S, SOURCE CURRENT (AMPS) vs V_{SD}, SOURCE–TO–DRAIN VOLTAGE (VOLTS)

$V_{GS} = 0$ V
$T_J = 25°C$
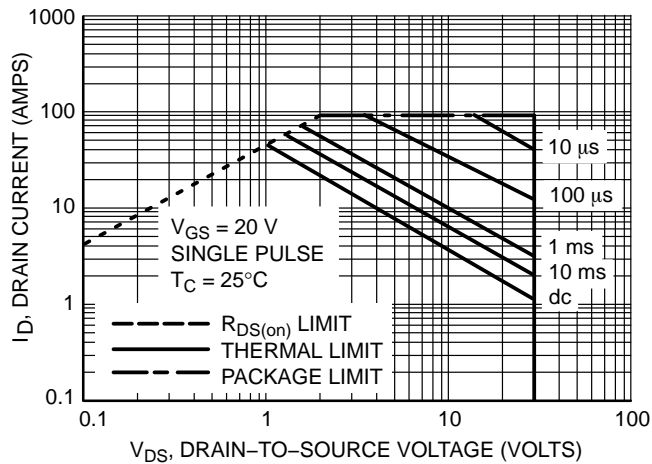
Figure 11. Maximum Rated Forward Biased Safe Operating Area

I_D, DRAIN CURRENT (AMPS) vs V_{DS}, DRAIN–TO–SOURCE VOLTAGE (VOLTS)

$V_{GS} = 20$ V
SINGLE PULSE
$T_C = 25°C$

10 µs
100 µs
1 ms
10 ms
dc

$R_{DS(on)}$ LIMIT
THERMAL LIMIT
PACKAGE LIMIT
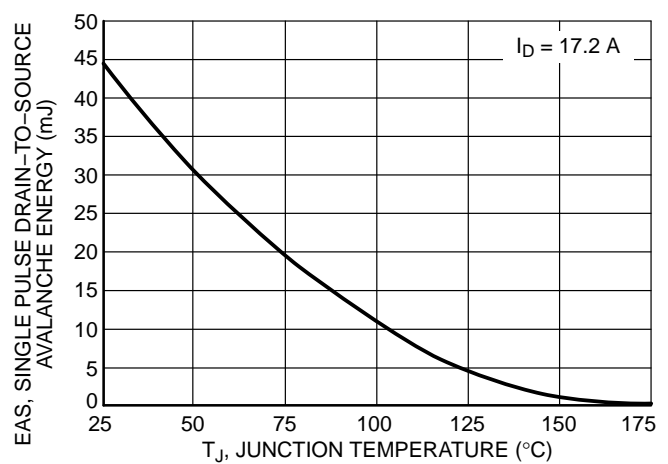
Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

EAS, SINGLE PULSE DRAIN–TO–SOURCE AVALANCHE ENERGY (mJ) vs T_J, JUNCTION TEMPERATURE (°C)

$I_D = 17.2$ A

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TYPICAL PERFORMANCE CURVES
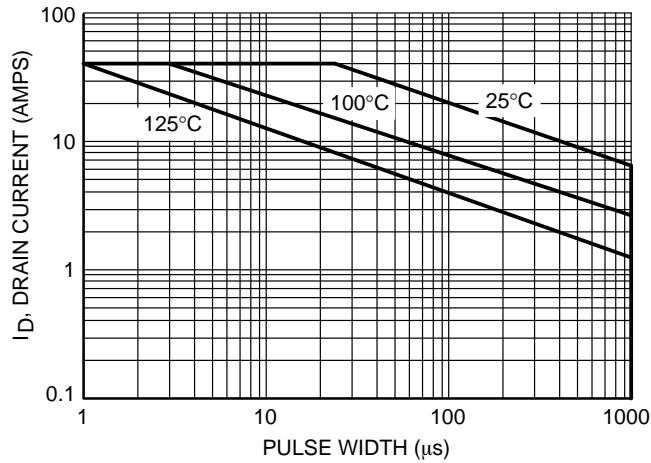
Figure 13. Avalanche Characteristics

$$R_{\theta JC}(t) = r(t)\, R_{\theta JC}$$
D CURVES APPLY FOR POWER
PULSE TRAIN SHOWN
READ TIME AT t_1
$$T_{J(pk)} - T_C = P_{(pk)}\, R_{\theta JC}(t)$$
DUTY CYCLE, $D = t_1/t_2$
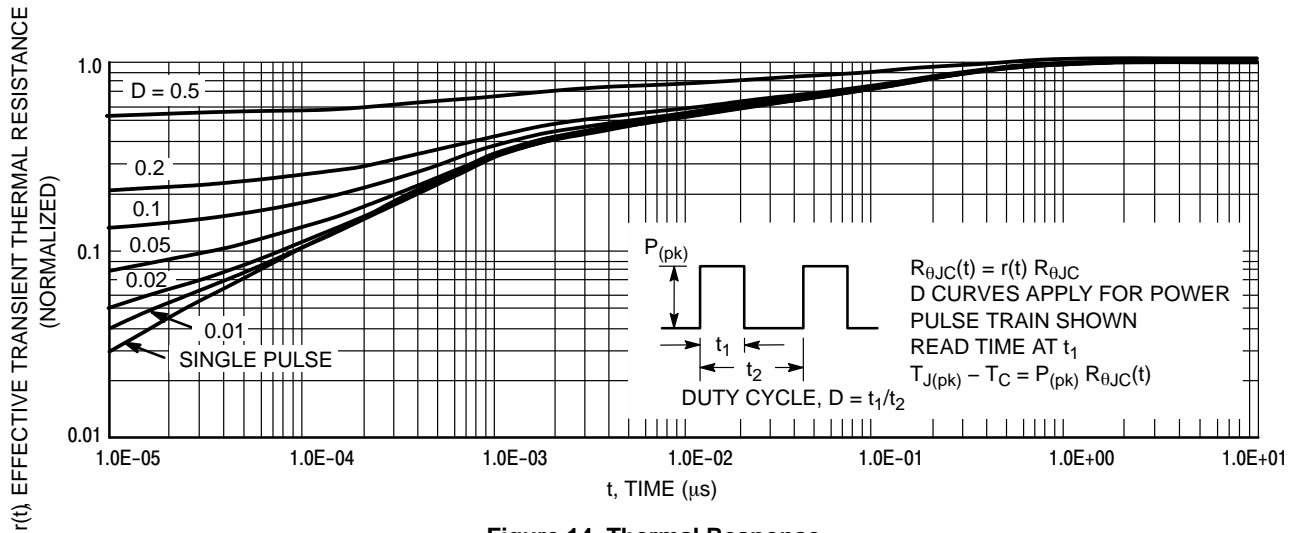
Figure 14. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping†
NTD4813NHT4G	DPAK (Pb−Free)	2500 / Tape & Reel
NVD4813NHT4G*	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE)
CASE 369AA
ISSUE B
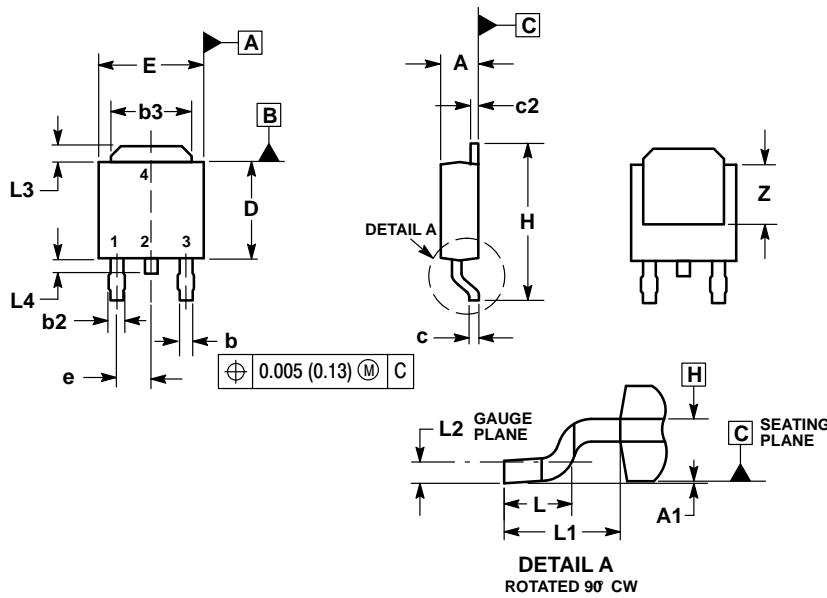
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	–––	0.040	–––	1.01
Z	0.155	–––	3.93	–––

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*
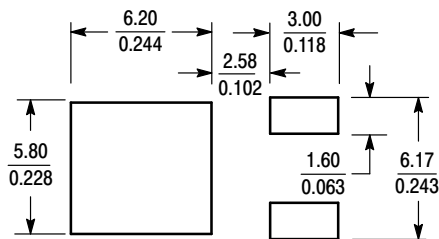
SCALE 3:1 $\left(\dfrac{mm}{inches}\right)$

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.