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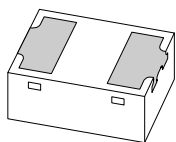
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Kind regards,

Team Nexperia



PESD5V0X1ULD

Ultra low capacitance unidirectional ESD protection diode

Rev. 1 — 15 February 2011

Product data sheet

1. Product profile

1.1 General description

Ultra low capacitance unidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients. The device is housed in a SOD882D leadless ultra small Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

The combination of extremely low capacitance and ultra low clamping voltage makes the device ideal for high-speed data line protection applications.

1.2 Features and benefits

- ESD protection of one line
- Ultra low diode capacitance
 $C_d = 0.95 \text{ pF}$
- Ultra low clamping voltage: $V_{CL} = 8 \text{ V}$
- Ultra low leakage current: $I_{RM} = 1 \text{ nA}$
- ESD protection up to 8 kV
- IEC 61000-4-2; level 4 (ESD)
- Ultra small SMD plastic package
- Solderable tin-plated side pads
- AEC-Q101 qualified

1.3 Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- 10/100/1000 Mbit/s Ethernet
- Communication systems
- Portable electronics
- Subscriber Identity Module (SIM) card protection
- USB, High-Definition Multimedia Interface (HDMI), FireWire
- High-speed data lines

1.4 Quick reference data

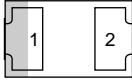
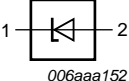
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	5.5	V
C_d	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}$	-	0.95	1.1	pF



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode ^[1]	 <p>Transparent top view</p>	 <p>006aaa152</p>
2	anode		

[1] The marking bar indicates the cathode.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0X1ULD	-	leadless ultra small plastic package; 2 terminals; body 1 × 0.6 × 0.4 mm	SOD882D

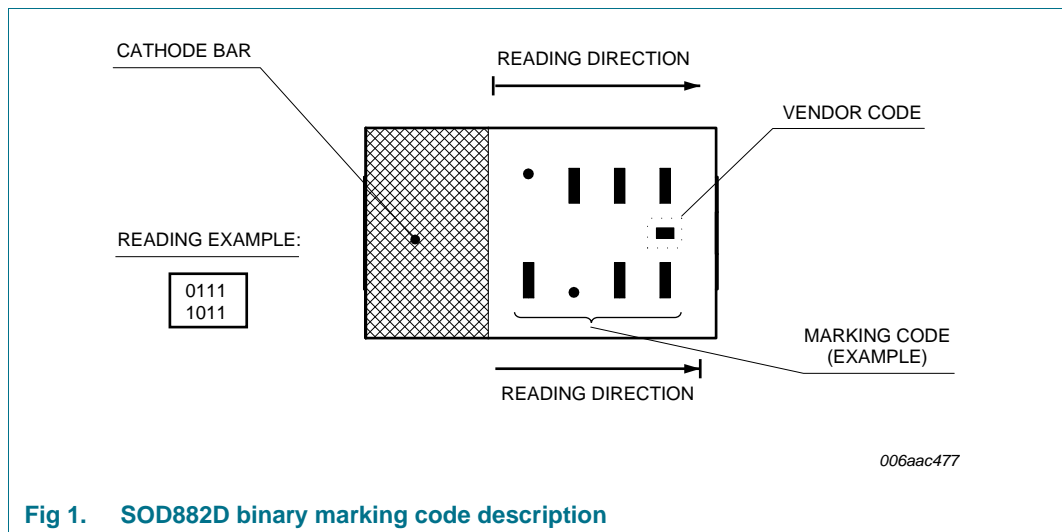
4. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PESD5V0X1ULD	1111 0000

[1] For SOD882D binary marking code description, see [Figure 1](#).

4.1 Binary marking code description



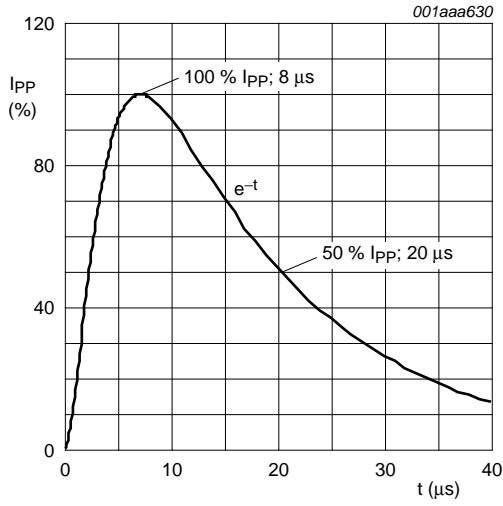


Fig 2. 8/20 μ s pulse waveform according to IEC 61000-4-5

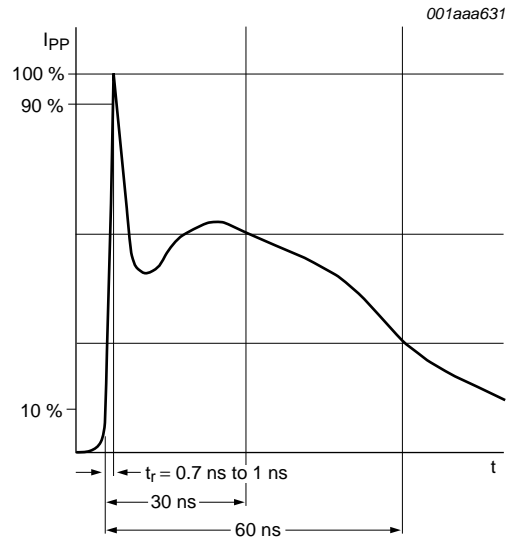


Fig 3. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

Table 8. Characteristics

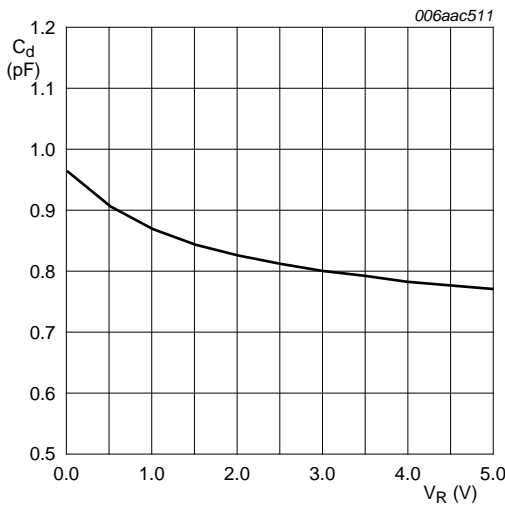
$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-	-	5.5	V
I_{RM}	reverse leakage current	$V_{RWM} = 5\text{ V}$	-	1	100	nA
V_{BR}	breakdown voltage	$I_R = 10\text{ mA}$	5.8	7.5	10	V
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}$	-	0.95	1.1	pF
V_{CL}	clamping voltage	$I_{PP} = 1.5\text{ A}$	[1][2]	8	-	V
r_{dyn}	dynamic resistance	$I_R = 10\text{ A}$	[3]	0.25	-	Ω

[1] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 to 2.

[3] Non-repetitive current pulse, Transmission Line Pulse (TLP) $t_p = 100\text{ ns}$; square pulse; ANS/IESD STM5-1-2008.



$f = 1\text{ MHz}; T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig 4. Diode capacitance as a function of reverse voltage; typical values

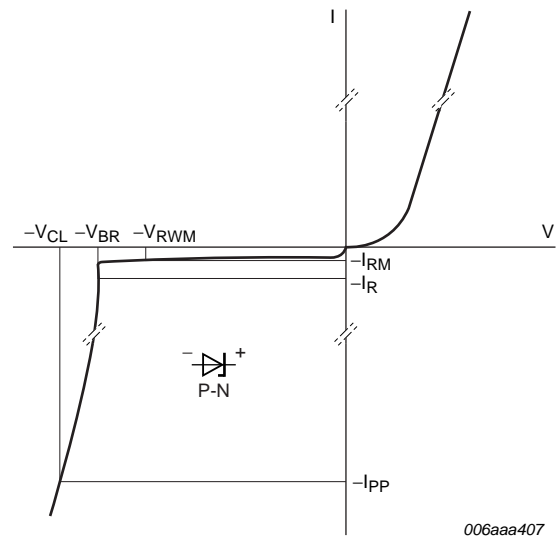


Fig 5. V-I characteristics for a unidirectional ESD protection diode

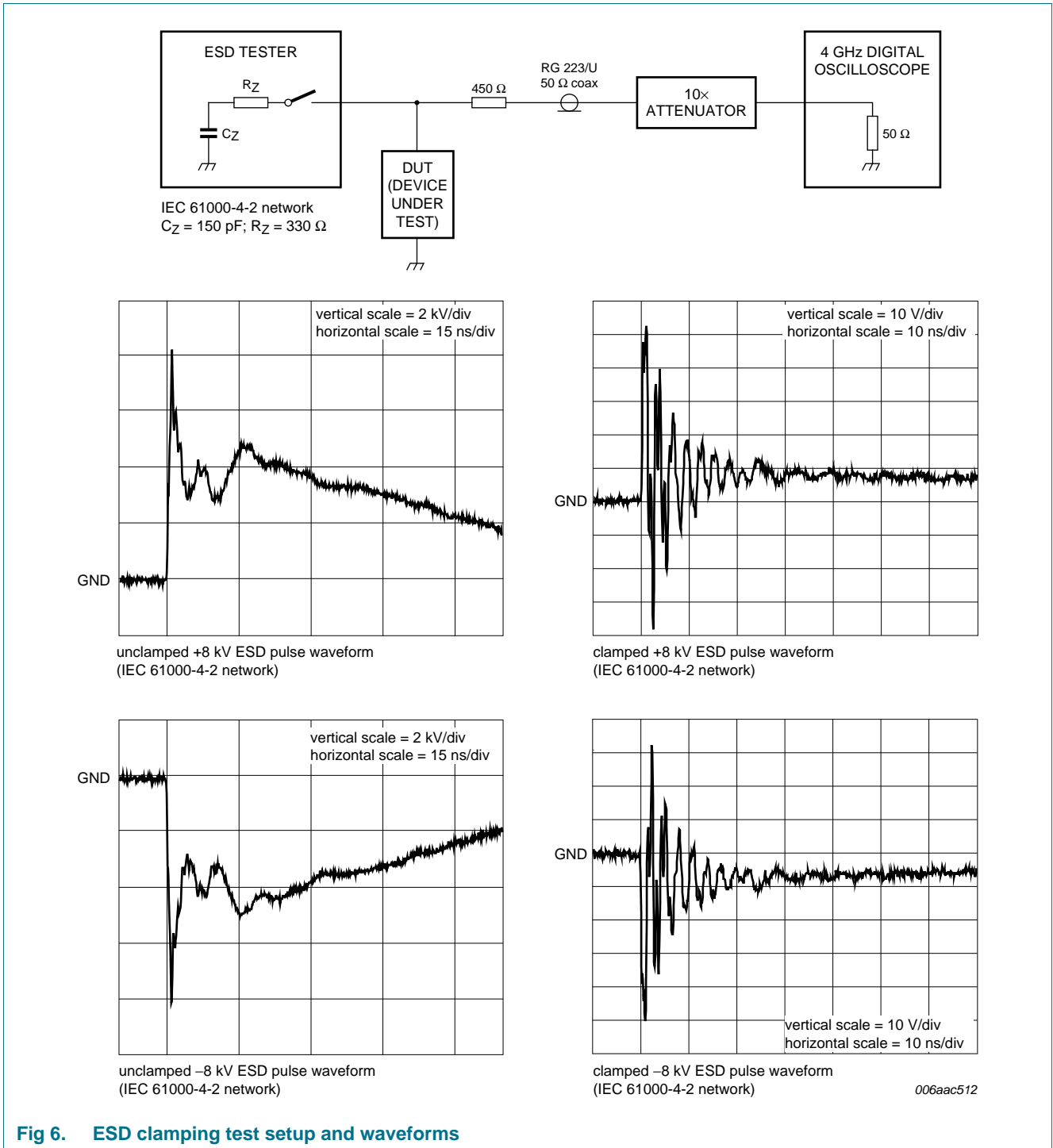


Fig 6. ESD clamping test setup and waveforms

7. Application information

The PESD5V0X1ULD is designed for the protection of one unidirectional data or signal line from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are either positive or negative with respect to ground.

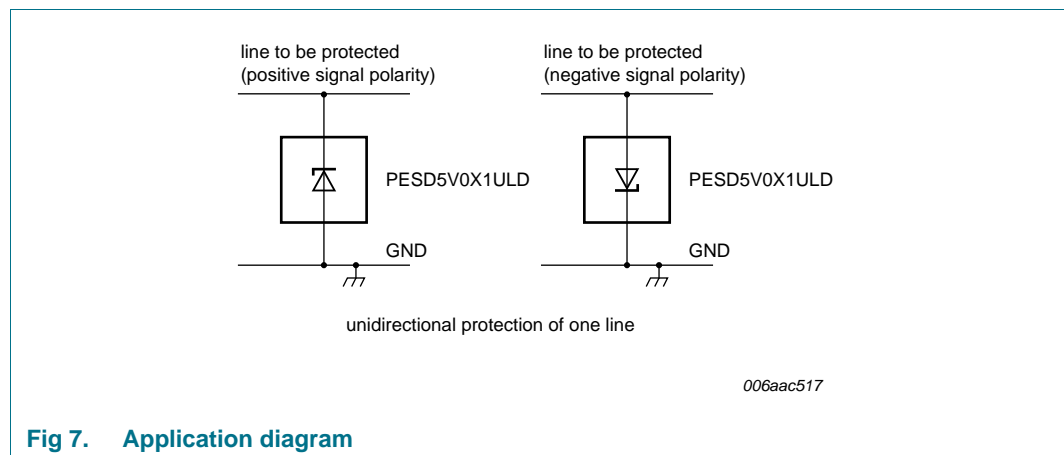


Fig 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

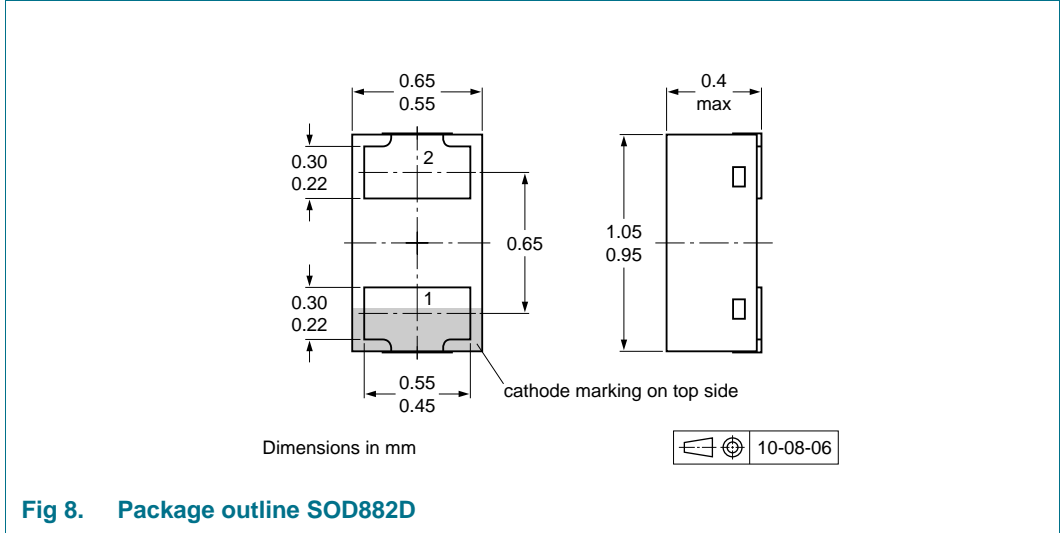
1. Place the PESD5V0X1ULD as close to the input terminal or connector as possible.
2. The path length between the PESD5V0X1ULD and the protected line should be minimized.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Ground planes should be used whenever possible. For multilayer PCBs, use ground vias.

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline



10. Packing information

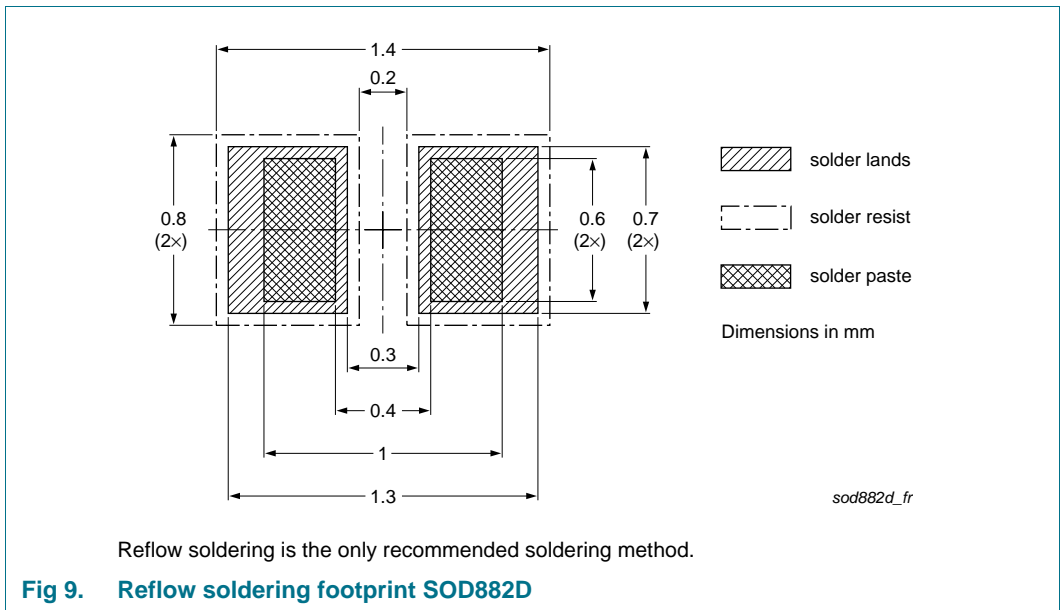
Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

Type number	Package	Description	Packing quantity
PESD5V0X1ULD	SOD882D	2 mm pitch, 8 mm tape and reel	10000 -315

[1] For further information and the availability of packing methods, see Section 14.

11. Soldering



12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0X1ULD v.1	20110215	Product data sheet	-	-

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

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