AK8771

Shipped in packet-tape reel(5000pcs/Reel)

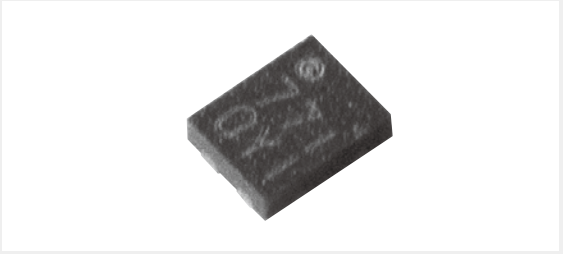
AK8771 is ultra-small Hall effect IC of a single silicon chip composed of Hall element and a signal processing IC.

Bipolar Hall Effect Latch	Supply Voltage 1.6~5.5V	Power down Function	Ultra High Sensitivity Bop:1.8mT	Output CMOS	SON

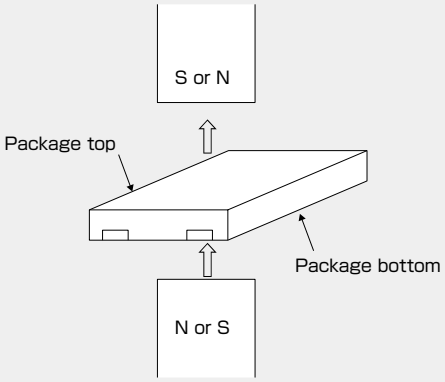
Notice:It is requested to read and accept "IMPORTANT NOTICE" written on the back of the front cover of this catalogue.

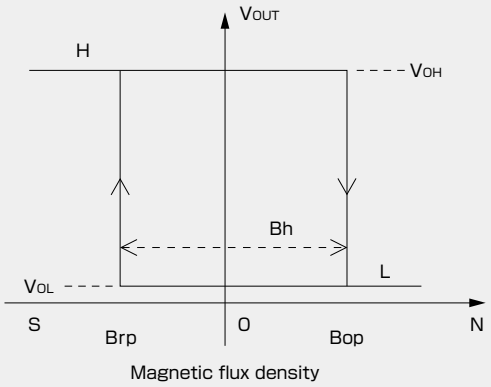
●Features

- Precision Bipolar Hall Effect Latch
- Power manageability through "PDN" pin
  Current consumption in Power down mode is less than 1μA
- Ultra small SON package : 1.1×1.4×t0.37mm, Halogen free

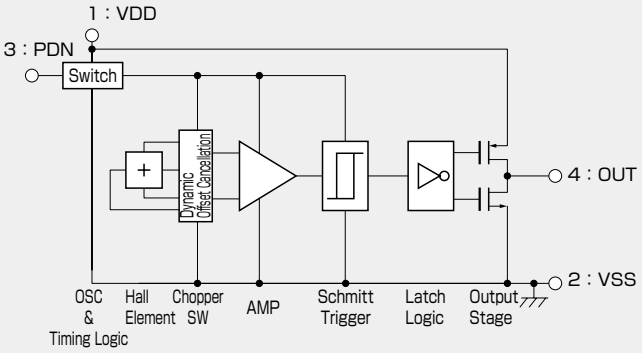


●Operational Characteristics





●Functional Block Diagram



Item	Function
OSC	Generates operating clock
Timing Logic	Generates timing signal requires for Chopper SW, AMP and other circuits
Hall Element	Hall element fabricated by CMOS process
Chopper SW	Performs chopping in order to cancel the offset voltage of Hall sensor
AMP	Reduce offset voltage and amplifies Hall output voltage
Schmitt Trigger	Hysteresis comparator
Latch Logic Output Stage	CMOS output, During the power down mode, output is latched in its previous state

●Absolute Maximum Ratings

Item	symbol	Min.	Max.	Unit	Note
Power supply voltage	V_{DD}	−0.3	+6.5	V	
Output current	I_{OUT}	−0.5	+0.5	mA	OUT
Input voltage	V_{IN}	−0.3	V_{DD}+0.3*	V	PDN
Input current	I_{IN}	−10	+10	mA	PDN
Storage temperature	T_{STG}	−55	+125	℃	

*) Less than +6.5V.
Note) Stress beyond these listed values may cause permanent damage to the device.

●Recommended Operating Conditions

Item	symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	1.6	3.0	5.5	V
Operating temperature	Ta	−30		+85	℃

●Electrical Characteristics (Ta=25℃ V_{DD}=3.0V)

Item	symbol	Min.	Typ.	Max.	Unit	Note
Current consumption 1	$I_{DD}1$			1	μA	PDN=0V
Current consumption 2	$I_{DD}2$		2.5	6	mA	PDN=3V
PDN input current	I_{IN}	−1		1	μA	
PDN input H voltage	V_{IH}	0.7V_{DD}			V	
PDN input L voltage	V_{IL}			0.3	V	
High level output voltage	V_{OH}	V_{DD}−0.4			V	I_{OUT}=−0.5mA
Low level output voltage	V_{OL}			0.4	V	I_{OUT}=+0.5mA
PDN mode transition time 1	$T_{PD}1$			100	μs	Active→PDN
PDN mode transition time 2	$T_{PD}2$			100	μs	PDN→Active

●Magnetic Characteristics① (Ta=25℃ V_{DD}=3.0V)

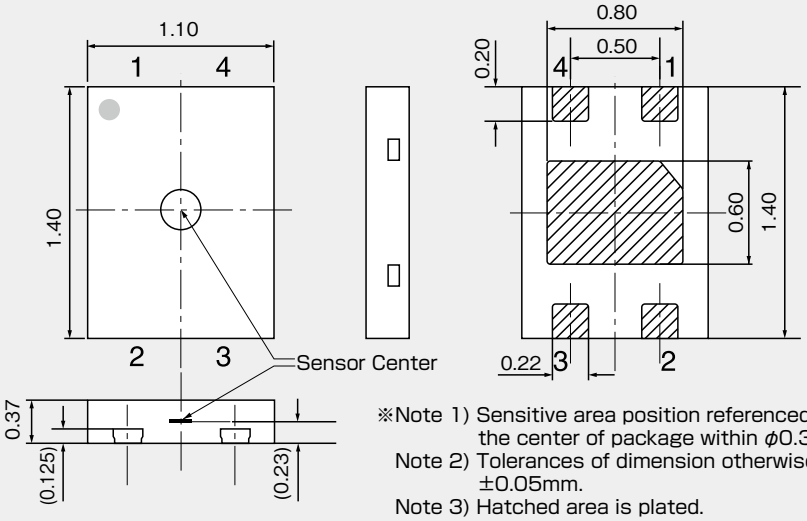
Item	symbol	Min.	Typ.	Max.	Unit
Operating point	Bop		1.8	4.0	mT
Releasing point	Brp	−4.0	−1.8		mT
Hysteresis	Bh		3.6		mT

●Magnetic Characteristics② (Ta=−30～+85℃ V_{DD}=1.6～5.5V)

Item	symbol	Min.	Typ.	Max.	Unit
Operating point	Bop		1.8	4.2	mT
Releasing point	Brp	−4.2	−1.8		mT
Hysteresis	Bh		3.6		mT

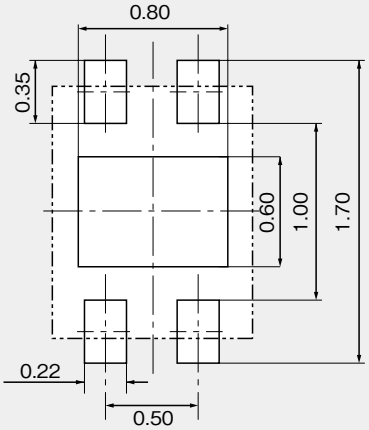
Note) The specifications in Magnetic Characteristics ② are design targets.

●Package (Unit:mm)



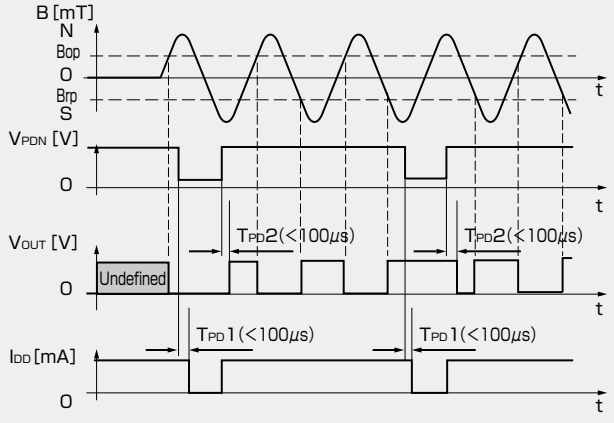
※Note 1) Sensitive area position referenced to the center of package within ϕ0.3mm circle.
Note 2) Tolerances of dimension otherwise noted is ±0.05mm.
Note 3) Hatched area is plated.
Note 4) Center pad area (TAB) should be tied to the VSS or floating

●Footprint (for reference)



No.	Pin name	Function	Note
1	VDD	Power supply	
2	VSS	Ground	
3	PDN	Power down. H:Device active L:Device power down	CMOS Input. This pin has to be tied to "H" level when external power control is not used.
4	OUT	Output	CMOS Output

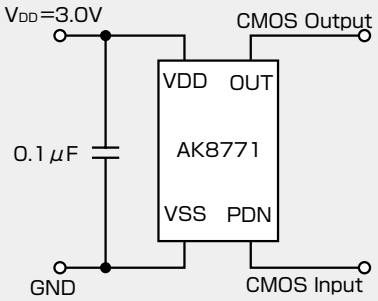
●Function Timing Chart



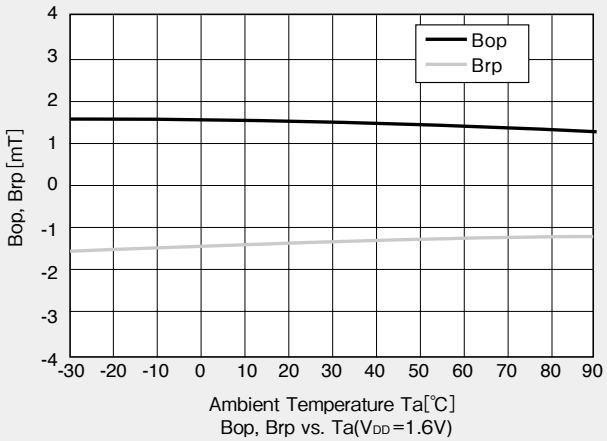
Functional Timing

Note1) During power down mode, output is latched in its previous state.
Note2) When VDD is supplied, the time from reaching V_{DD}=1.6V to the update of the output state is equal to $T_{PD}2$.

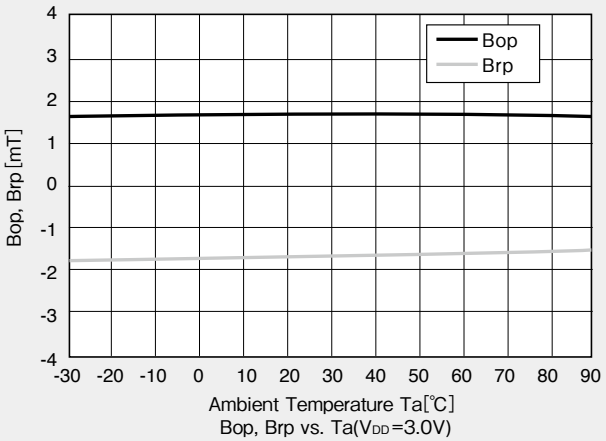
●Application Circuit



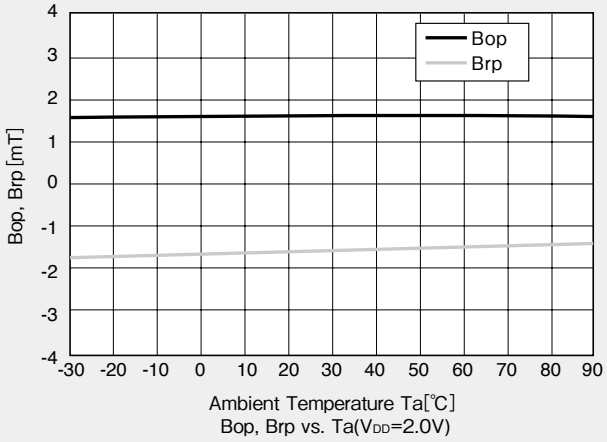
●Typical Characteristic Data (for reference)



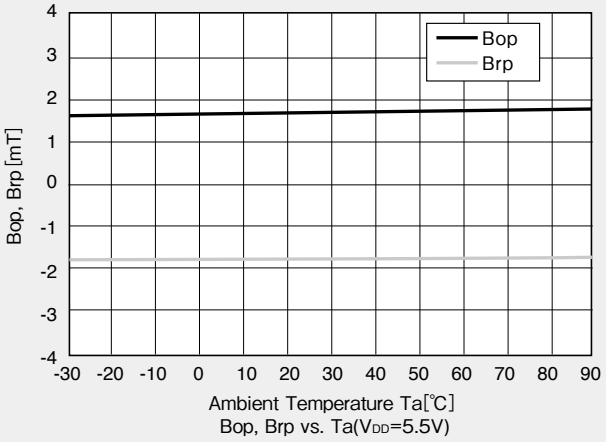
Bop, Brp vs. Ta(V_{DD}=1.6V)



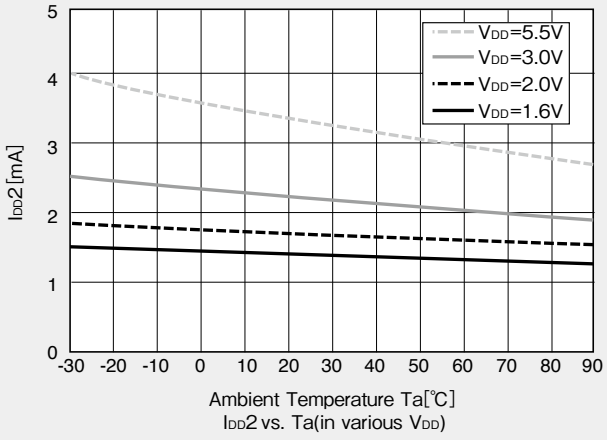
Bop, Brp vs. Ta(V_{DD}=3.0V)



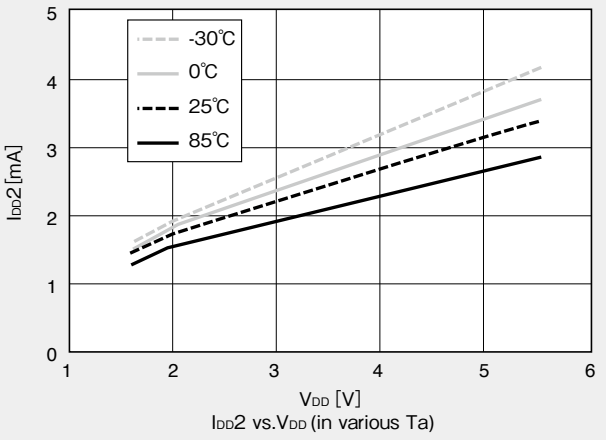
Bop, Brp vs. Ta(V_{DD}=2.0V)



Bop, Brp vs. Ta(V_{DD}=5.5V)



$I_{DD}2$ vs. Ta(in various V_{DD})



$I_{DD}2$ vs.V_{DD} (in various Ta)

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