

### FEATURES

- Highly configurable DIP switch settings: input configuration, coupling techniques, and shutdown control**
- Optional dc power supply jack (accepts 2.5 V to 5.5 V)**
- Single-ended and differential input capability**
- Multiple output interface connection terminals**

### GENERAL DESCRIPTION

The SSM2306 is a single-chip, dual-channel, Class-D stereo audio amplifier. It is a fully integrated chip, which means that the application circuit requires a minimum of external components. It comes with a differential mode input port and a high efficiency H-bridge at the output. When compared to a half-bridge output stage, a full H-bridge enables direct coupling of the audio power signal to the loudspeaker, doubling the output voltage swing and eliminating the need for a large output coupling capacitor. Another benefit of a full H-bridge is an increase in the maximum output power by 4× when compared to a half bridge under the same load impedance. These benefits are particularly useful for low voltage, battery-powered, portable electronics where energy and space are limited. The differential mode input stage allows for canceling of common-mode noise leading to a superior CMRR.

Moreover, the part features a high efficiency, low noise output modulation scheme that does not require external LC output filters when attached to an inductive load. The modulation

provides high efficiency even at low output power. Filterless operation also helps to decrease distortion due to nonlinearities of output LC filters, thereby delivering better sound quality and leading to savings in board space and overall cost.

This data sheet describes how to configure and use the SSM2306 evaluation board. It is recommended that this data sheet be read in conjunction with the [SSM2306](#) data sheet, which provides more detailed information about the specifications, internal block diagrams, and application guidance for the amplifier IC.

### EVALUATION BOARD DESCRIPTION

The SSM2306 evaluation board carries a complete application circuit for driving two stereo loudspeakers. Figure 1 shows the top view of the PCB and its layout, and Figure 2 shows the bottom view of the PCB. The silkscreen layer of the evaluation board is shown in Figure 7 with other top layers, including top copper, top solder mask, and multilayer vias. Figure 8 shows the top silkscreen layer only. There are no components on the bottom side; therefore, there is no bottom silkscreen layer. Figure 9 shows the top layers without the silkscreen layer. Figure 10 shows the bottom layers, including bottom copper, bottom solder mask, and multilayer vias. Figure 11 shows the mirrored bottom layers. The bill of materials (BOM) is provided in Table 4.

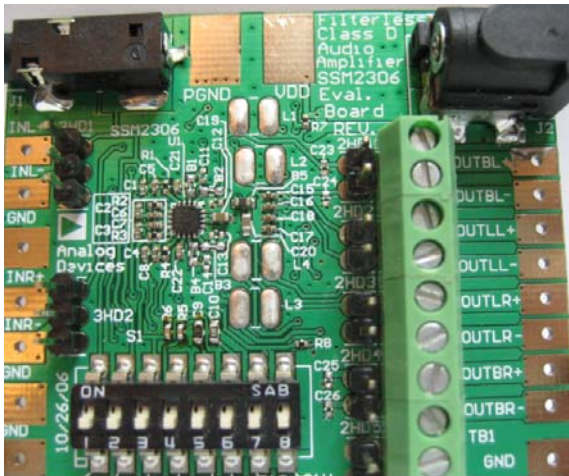


Figure 1. SSM2306 Evaluation Board

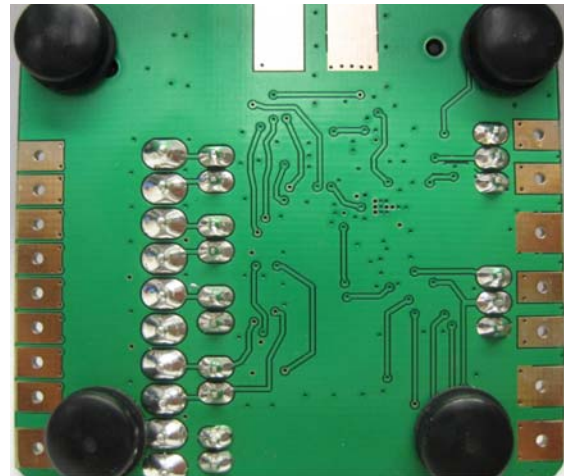


Figure 2. SSM2306 Evaluation Board, Bottom View

#### Rev. 0

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## REVISION HISTORY

8/08—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

Note that the SSM2306 evaluation board and layout guidelines were developed by Gang Liu of Analog Technologies, Inc., Sunnyvale, CA.

### SWITCHES

On the upper left corner of the evaluation board is an audio stereo jack connector (3.5 mm), J1. The evaluation board uses a conventional audio stereo signal connector/cable to receive standard stereo audio signals from common appliances such as DVD players, PCs, and TVs. Note that the two output signals from the J1 connector are combined by a resistor network, R1 and R2, into a single signal. This connector provides single-ended audio signals only. Therefore, when this input connector is used, the S1E and S1F switches must be placed in the up position to ac short-circuit the negative input ports to ground. This signal path is shown in the schematic in Figure 6. Some appliances have strong ground noise. If the audio source has strong ground noise, do not use the J1 connector as the input connection point. A single-ended input signal with strong ground noise can generate an audible hissing sound at the output. If this problem occurs, a differential mode connection is needed to cancel the ground noise interference.

When differential mode audio signals are used as the input signal source, use the headers 3HD1 and 3HD2 or use the soldering pads located on the left side of the board. The top header (3HD1) is for the left channel signals, and the lower header (3HD2) is for the right channel. For differential mode, turn the S1E and S1F switches to their off position (the down position).

There are two ground soldering pads on the lower left corner of the evaluation board. At the bottom of the board is a switch bank; the switch names and their corresponding functions are shown in Table 1.

**Table 1. Evaluation Board Switches**

Switch Name	Function
S1A	AC-couple left channel, noninverting input
S1B	AC-couple left channel, inverting input
S1C	AC-couple right channel, inverting input
S1D	AC-couple right channel, noninverting input
S1E	AC ground left channel, inverting input
S1F	AC ground right channel, inverting input
S1H	Shutdown

When the S1A, S1B, S1C, and S1D switches are placed in the up position, their corresponding coupling capacitors are shorted; when these switches are placed in the down position, the coupling capacitors are inserted in the signal paths.

The S1E and S1F switches are used to ac short-circuit the left and right channel negative input ports to ground, respectively. This function is generally recommended, but is only necessary when driving the input ports in single-ended mode. After shorting the negative input ports to ground, the noise picked up by the input port connections is conducted to ground.

The S1H switch is for the shutdown function: the up position is for shutdown, and the down position turns the amplifier on.

The upper right corner of the evaluation board has a dc power jack connector, J2. The center pin is for the positive terminal. The jack takes 2.5 V to 5.5 V voltage. With the input voltage at 5 V, the maximum peak current is approximately 1.2 A when driving a 4 Ω load, and 0.6 A when driving an 8 Ω load.

There are two solder pads at the top center edge of the evaluation board for connecting the power supply voltages by clipping or soldering.

All the output ports are located on the right side of the board and are labeled. See the legend on the evaluation board and on the schematic (Figure 6).

There are three ways to connect the output signals to the loads (the loudspeakers): using the four 2-pin headers 2HD1 to 2HD4, using the terminal block, or using the soldering pads.

### GETTING STARTED

To ensure proper operation, follow these steps carefully.

- Verify that the control switches are set as follows:
  - Shutdown control: S1H down. This activates the amplifier.
  - Audio source: S1E and S1F. For single-ended mode (audio jack), place S1E and S1F in the up position.
  - Input coupling: S1A, S1B, S1C, and S1D. For most applications, ac-couple the inputs by placing these switches in the down position.
- Connect the loads to the proper output ports, depending on the application. To connect the loads immediately after the ferrite beads, use the OUTBL+, OUTBL-, OUTBR+, and OUTBR- nodes. To connect the loads after the inductors, use the OUTLL+, OUTLL-, OUTLR+, and OUTLR- nodes.
- Connect the power supply with the correct polarity and proper voltage.

### WHAT TO TEST

When implementing the SSM2306 evaluation board, test the evaluation board for the following items:

- Electromagnetic interference (EMI). Connect wires for the speakers in the same length as for the actual application and perform the EMI test.
- Signal-to-noise ratio (SNR).
- Total harmonic distortion + noise (THD + N).
- Output noise. Use an A-weighting filter to filter the output before the measurement meter.
- Maximum output power.
- Efficiency.

## COMPONENT SELECTION

Selecting the right components is the key to achieving the performance required at the budgeted cost. The BOM for the SSM2306 evaluation board is provided in Table 4.

### Input Coupling Capacitors

The input coupling capacitors, C1, C2, C3, and C4, should be large enough to couple the low frequency signal components in the incoming signal and small enough to filter out unnecessary low frequency signals. For music signals, the selected cutoff frequency is often between 20 Hz and 30 Hz. The value of the coupling capacitor is calculated as follows:

$$C = 1/(2\pi \times R \times f_c)$$

where:

$$R = 43 \text{ k}\Omega + R_{EXT}$$

$f_c$  is the cutoff frequency.

### Input Series Resistors

The input series resistors, R1, R2, R3, and R4, are not necessary for amplifier operation and are needed only when special gain values are required. Using resistors with too high a value increases the input noise.

### Output Beads

The output beads, B1, B2, B3, and B4, are necessary components for filtering out the EMI caused at the switching output nodes when the length of the speaker wire is greater than 10 cm. The penalty for using ferrite beads for EMI filtering is slightly worse noise and distortion performance at the system level due to the nonlinearity of the beads.

Ensure that these beads have enough current conducting capability while providing sufficient EMI attenuation. The current rating needed for an 8  $\Omega$  load is approximately 600 mA, and impedance at 100 MHz must be > 220  $\Omega$ . In addition, the lower the dc resistance (DCR) of these beads, the better for minimizing their power consumption. Table 2 describes the recommended bead.

**Table 2. Recommended Output Bead**

Part Number	Manu- facturer	Z ( $\Omega$ )	I <sub>MAX</sub> (mA)	DCR ( $\Omega$ )	Size (mm)
BLM18EG221SN1D	Murata	220	2000	0.05	1.6 × 0.8 × 0.8

### Output Shunting Capacitors for the Beads

There are two groups of output shunting capacitors for the beads: C11 to C14 and C23 to C26. Capacitors C11 to C14 filter out lower frequency EMI  $\leq 250$  MHz; Capacitors C23 to C26 filter out higher frequency EMI >250 MHz. Use small size (0603 or 0402) multilayer ceramic capacitors made of X7R or C0G (NP0) materials. The higher the value of these capacitors, the lower the residual EMI level at the output, and the higher the quiescent current at the power supply. The recommended values for Capacitors C11 to C14 are 500 pF to 1 nF; the recommended values for Capacitors C23 to C26 are 100 pF to 200 pF.

## Output Inductors

Some users do not allow high frequency EMI in the system and prefer using inductors to filter out high frequency components at the output nodes. Choose inductance >2.2  $\mu$ H for these inductors. The higher the inductance, the lower the EMI at the output and the lower the quiescent current at the power supply.

However, note that higher inductance increases the power consumption of the inductors when the output power level is high. Analog Devices, Inc., recommends using 2.2  $\mu$ H to 10  $\mu$ H inductors with a current rating of >600 mA (saturation current) for an 8  $\Omega$  load. Table 3 describes the recommended inductors.

**Table 3. Recommended Output Inductors**

Part Number	Manu- facturer	L ( $\mu$ H)	I <sub>MAX</sub> (mA)	DCR ( $\Omega$ )	Size (mm)
LQH32CN4R7M53	Murata	4.7	650	0.15	3.2 × 2.5 × 1.55
LQH32CN3R3M53	Murata	3.3	710	0.12	3.2 × 2.5 × 1.55
LQH32CN2R2M53	Murata	2.2	790	0.1	3.2 × 2.5 × 1.55
SD3118-100-R	Cooper Bussmann	10	900	0.3	3.1 × 3.1 × 1.8
ELL4LM100M	Panasonic	10	690	0.18	3.8 × 3.8 × 1.8
LBC2518T2R2M	Taiyo Yuden	2.2	630	0.169	2.5 × 1.8 × 1.8
1033AS-4R7M	Toko	4.7	680	0.31	3.8 × 3.8 × 1.0

## PCB LAYOUT GUIDELINES

Correct PCB layout is critical in application designs to prevent EMI from exceeding allowable limits and to ensure that the amplifier chip operates below the temperature limit. Follow these guidelines carefully when designing the PCB layout.

- Place nine vias onto the thermal pad of the amplifier. The outer diameter of the vias should be 0.5 mm, and the inner diameter should be 0.33 mm. If internal layers are available in the PCB, allocate an area as large as possible to the ground planes and connect these vias to the ground planes (see Figure 3). If internal layers are available, allocate a specific area as a heat sink; make sure to connect the vias conducting heat to the internal layers.

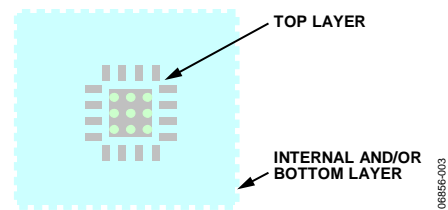


Figure 3. Heat Sink Layout

- Place the EMI filtering beads (B1, B2, B3, and B4) as close to the amplifier chip as possible. If you use output inductors (L1, L2, L3, and L4) in the application design, place them as close to the amplifier chip as possible.

3. Place the decoupling capacitors for the beads (C11 to C14 and C23 to C26) as close to the amplifier chip as possible, and connect all their ground terminals together, as shown in Figure 4. The same principle applies to the decoupling capacitors for the inductors (C15 to C18) if inductors are used in the application design. Ideally, solder their ground terminals together; do not rely on PCB tracks or ground planes to connect their ground terminals together.
4. Place the first decoupling capacitor for the power supply (C19) as close to the amplifier chip as possible, and connect its ground terminal directly to the IC GND pins (Pin 13 and Pin 16), as shown in Figure 4.
5. Place the other decoupling capacitor for the power supply (C20) as close to the amplifier chip as possible, and connect its ground terminal to the PCB ground area from which the power supply traces come.
6. Place the bead for the power supply (B5) as close to the amplifier chip as possible, and keep it on the same side of the PCB as the chip.

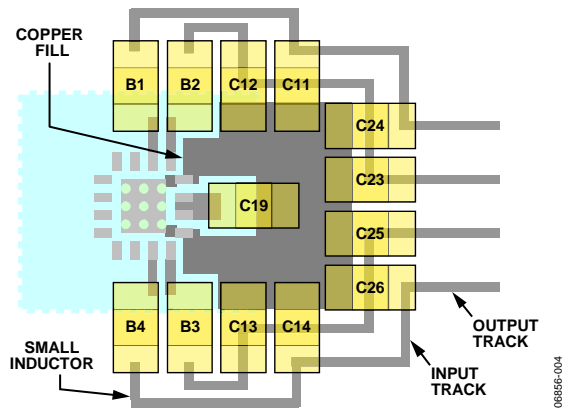


Figure 4. Placement and Routing of the Decoupling Capacitors

7. The ferrite beads and their 1 nF decoupling capacitors can block EMI up to 250 MHz. To eliminate EMI higher than 250 MHz, place a low value, small size capacitor, such as a 100 pF, 0402 size capacitor, in parallel with the decoupling capacitors, C11, C12, C13, and C14. Place these small capacitors (C23, C24, C25, and C26) at least 20 mm away from the 1 nF decoupling capacitors. Ideally, the ground terminals of these small capacitors should be connected to the ground terminals of the 1 nF decoupling capacitors or to the PCB traces, which are placed as close to the output loads (the loudspeakers) as possible. In this way, the PCB connecting

trace between these two capacitors serves as an inductor for filtering out the high frequency component, as shown in Figure 4.

8. Decouple the input port nodes and the digital pins (Pin 3, Pin 4, Pin 5, Pin 8, and Pin 9) with small capacitors, such as 100 pF. These capacitors (C5, C6, C7, and C8) are not required, but they can lower the EMI from these pins. The ground terminals of these capacitors should be connected as close to the chip ground as possible (see Figure 7).
9. Ground the unconnected pins, Pin 6 and Pin 7.
10. Connect the GND pins, Pin 13 and Pin 16, to the thermal pad and place grounding vias, as shown in Figure 7, Figure 8, and Figure 9.
11. Use a solid polygon plane on the other side of the PCB for the area of the vias that are placed on the thermal pad of the chip. See Figure 10 or Figure 11. This polygon serves as both the EMI shielding ground plane and the heat sink for the SSM2306.
12. Keep the PCB traces of high EMI nodes on the same side of the PCB and as short as possible. The high EMI nodes on the SSM2306 are Pin 1, Pin 2, Pin 11, and Pin 12.
13. The incoming and outgoing PCB track connections to the decoupling capacitors should not be connected to each other. An example of a correct layout is shown in Figure 4. An example of an incorrect layout is shown in Figure 5.

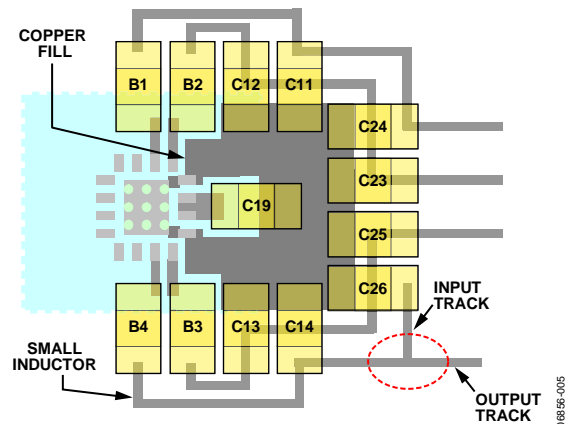


Figure 5. Incorrect Routing for the Output Decoupling Capacitors

The SSM2306 evaluation board works well only if these techniques are implemented in the PCB design to keep EMI and amplifier temperature low.

## EVALUATION BOARD SCHEMATIC AND ARTWORK

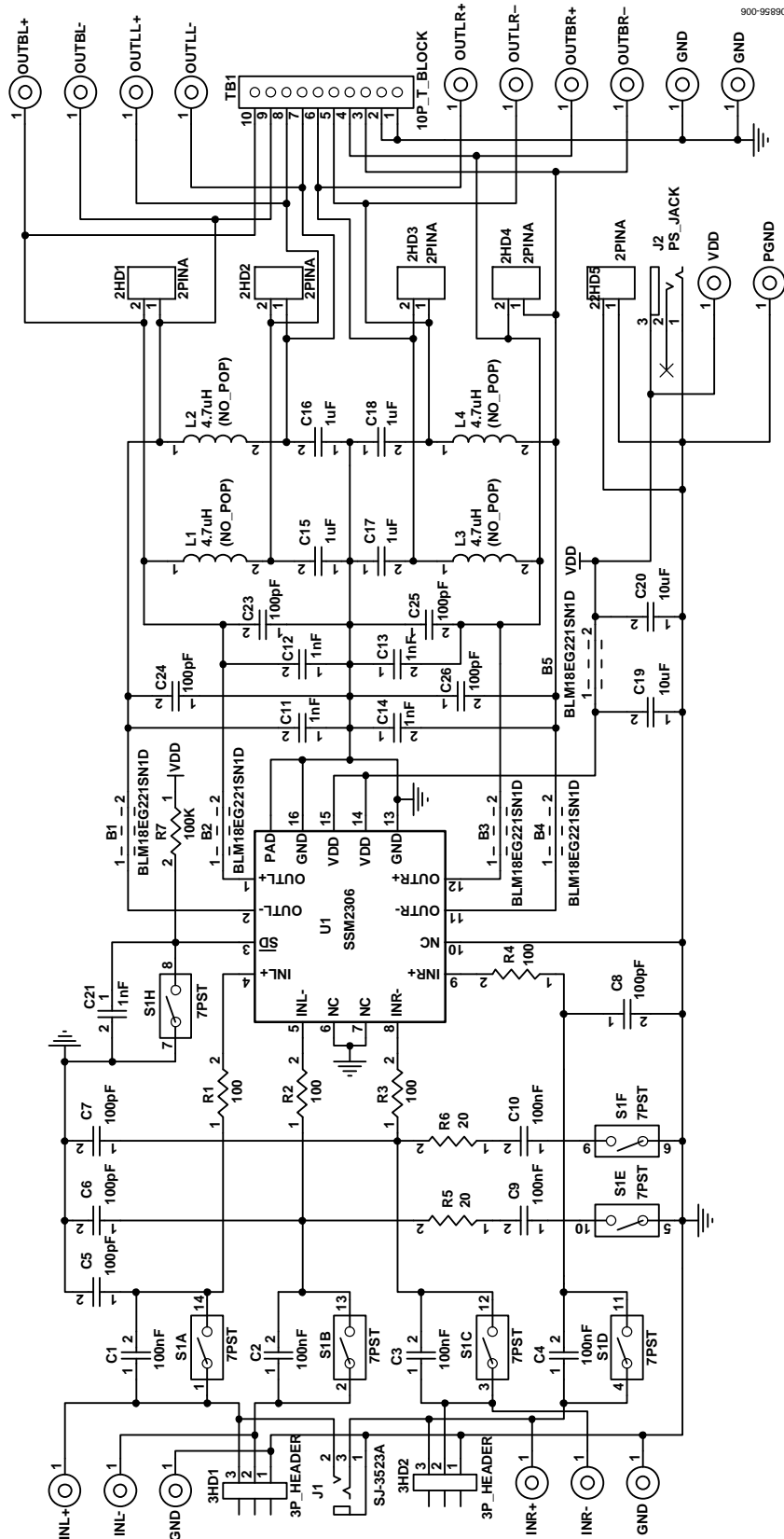


Figure 6. Schematic of the SSM2306 Evaluation Board

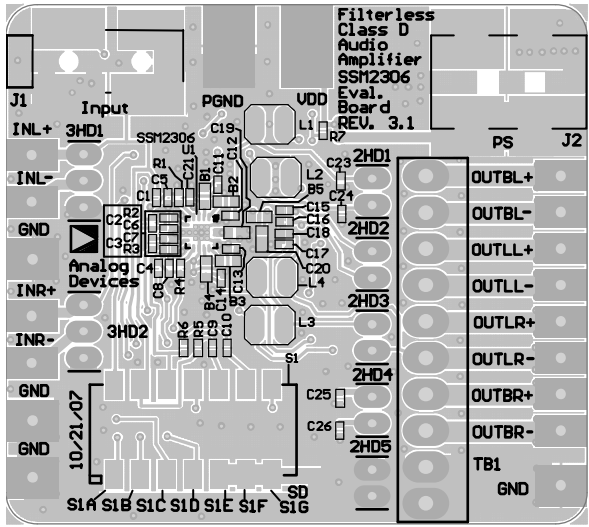


Figure 7. Top Silkscreen Layer with Other Top Layers

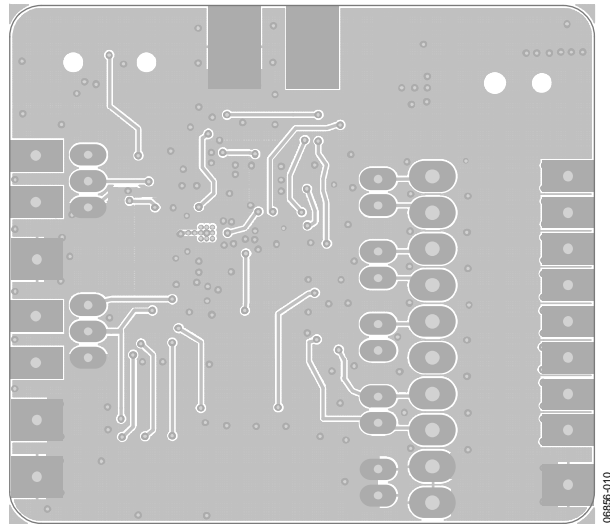


Figure 10. Bottom Layers of the Evaluation Board

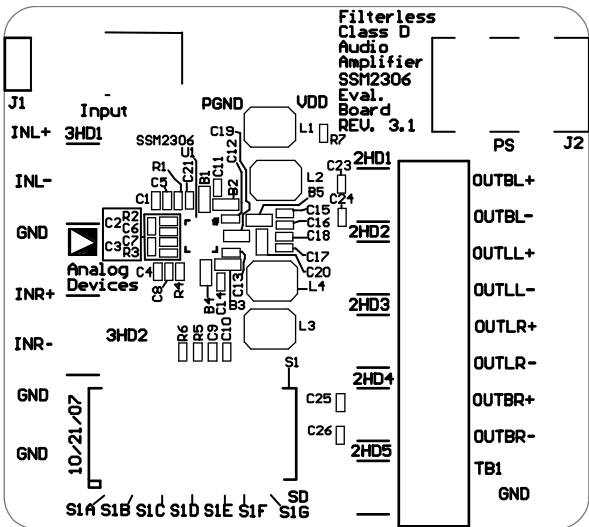


Figure 8. Top Silkscreen

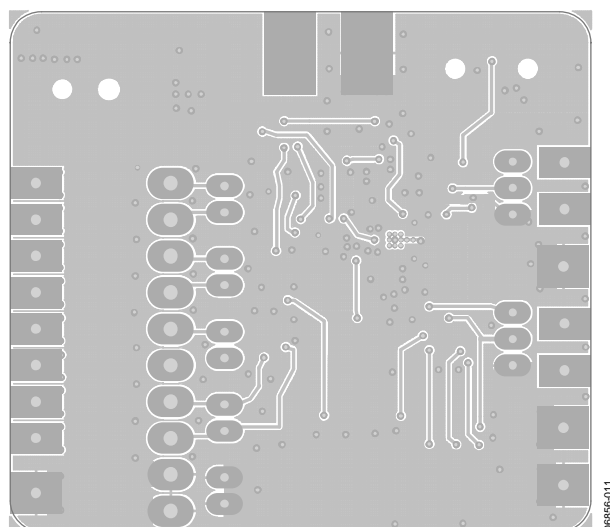


Figure 11. Mirrored Bottom Layers of the Evaluation Board

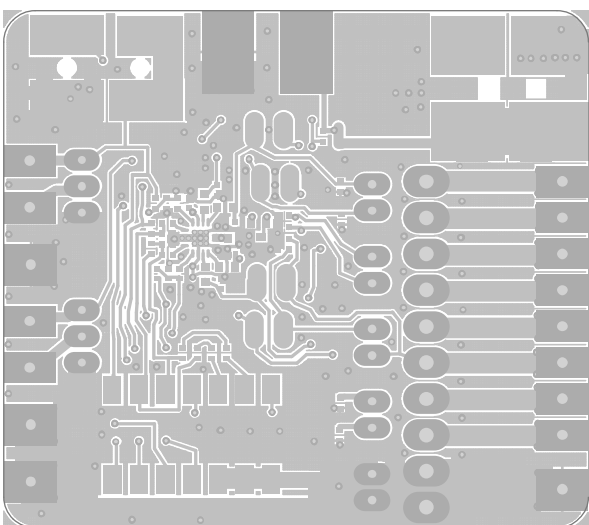


Figure 9. Top Layers Without the Top Silkscreen Layer

# EVAL-SSM2306

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 4.

Qty	Designator	Description	Supplier	Part Number
4	R1 to R4	Resistor, 100 Ω, 1/16 W, 0.5%, 0402, SMD	Digi-Key	RR05P100DTR-ND
2	R5, R6	Resistor, 20 Ω, 1/16 W, 0.5%, 0402, SMD	Digi-Key	RR05R20DTR-ND
1	R7	Resistor, 100 kΩ, 1/16 W, 0.5%, 0402, SMD	Digi-Key	RR05P100KDTR-ND
6	C1 to C4, C9, C10	Capacitor, ceramic, 100 nF, 35 V, X5R, 0402	Digi-Key	587-1994-2-ND
8	C5 to C8, C23 to C26	Capacitor, ceramic, 100 pF, 6.3 V, X7R, 0402	Digi-Key	04026C101KAT2A-ND
5	C11 to C14, C21	Capacitor, ceramic, 1 nF, 5%, 50 V, X7R, 0402	Digi-Key	478-3661-2-ND
4	C15 to C18	Capacitor, ceramic, 1 μF, 10 V, X5R, 0402	Digi-Key	490-3890-2-ND
2	C19, C20	Capacitor, ceramic, 10 μF, 6.3 V, X5R, 0603	Digi-Key	PCC2395TR-ND
4	L1 to L4	Inductor, 4.7 μH, 650 mA, 1210	Digi-Key	490-4057-2-ND
5	B1 to B5	Filter chip, 220 Ω, 2 A, 0603	Digi-Key	490-3992-2-ND
1	S1 (S1A, S1B, S1C, S1D, S1E, S1F, S1G, S1H)	Switch, DIP, top slide, 8-position, SMD	Digi-Key	CKN6092-ND
1	J1	Audio connector, 3.5 mm, SMT stereo	Mouser	806-STX-3500-3N
1	J2	DC power connector, 2 mm, SMT power jack	Mouser	806-KLDX-SMT20202A
1	U1	2 W, filterless, Class-D stereo audio amplifier	Analog Devices	SSM2306CPZ
5	2HD1, 2HD2, 2HD3, 2HD4, 2HD5	Connector header, 2-position, 0.100" SGL gold	Digi-Key	SAM1029-02-ND
2	3HD1, 3HD2	Connector header, 3-position, 0.100" SGL gold	Digi-Key	SAM1029-03-ND
1	TB1	Terminal block, 3.5 mm, 10-position PCB	Digi-Key	ED1522-ND

### ORDERING GUIDE

Model	Description
SSM2306-EVALZ <sup>1</sup>	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.