

RMLV0816BGSD - 4S2

8Mb Advanced LPSRAM (512k word × 16bit / 1024k word × 8bit)

R10DS0253EJ0200
Rev.2.00
2015.06.26

Description

The RMLV0816BGSD is a family of 8-Mbit static RAMs organized 524,288-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0816BGSD has realized higher density, higher performance and low power consumption. The RMLV0816BGSD offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 52pin μ TSOP (II).

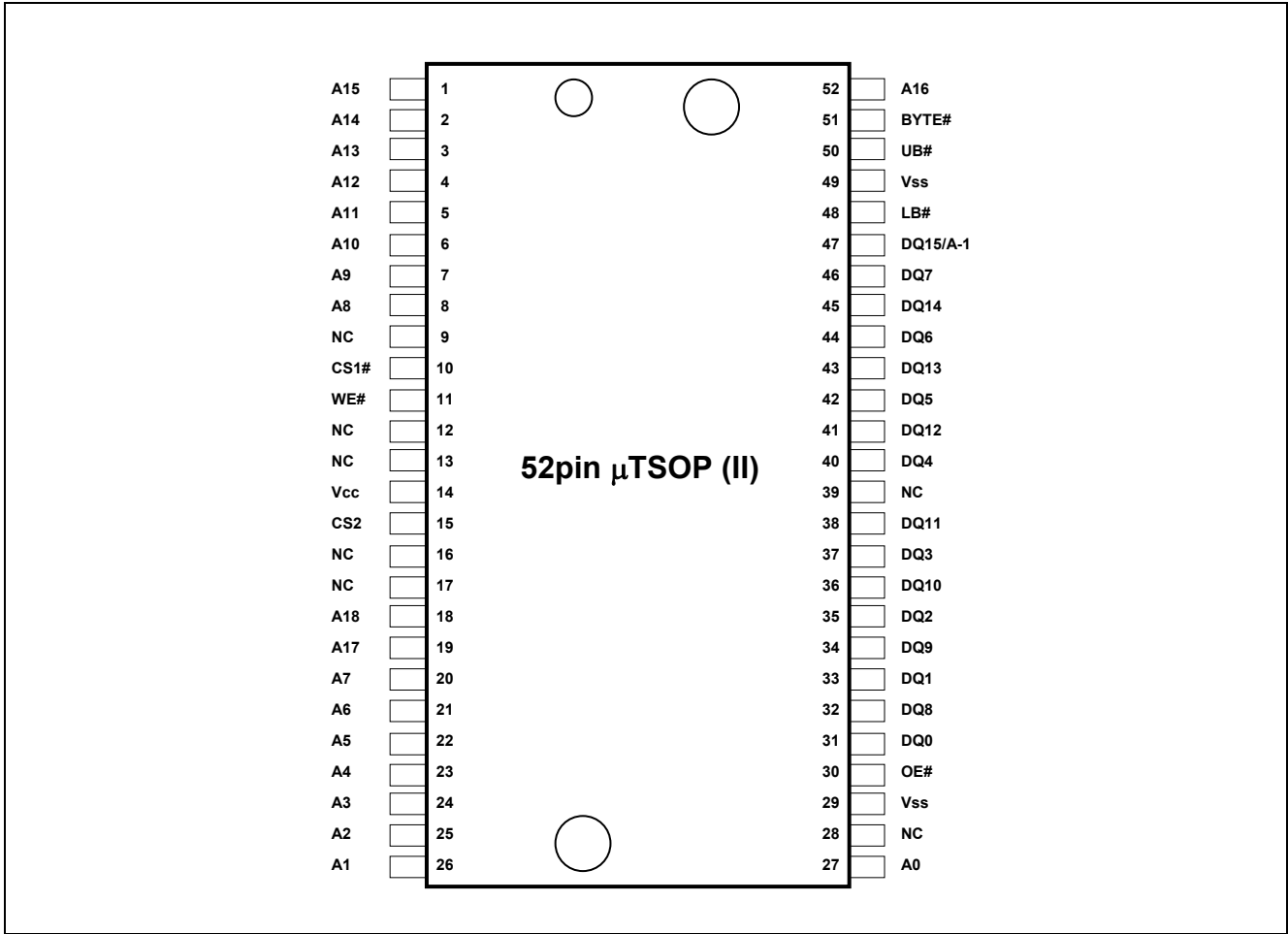
Features

- Single 3V supply: 2.4V to 3.6V
- Access time:
 - Power supply voltage from 2.7V to 3.6V: 45ns (max.)
 - Power supply voltage from 2.4V to 2.7V: 55ns (max.)
- Current consumption:
 - Standby: 0.45 μ A (typ.)
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation

Part Name Information

Part Name	Power supply	Access time	Temperature Range	Package
RMLV0816BGSD-4S2	2.7V to 3.6V	45 ns	-40 ~ +85°C	10.79mm × 10.49mm 52pin plastic μ TSOP (II)
	2.4V to 2.7V	55 ns		

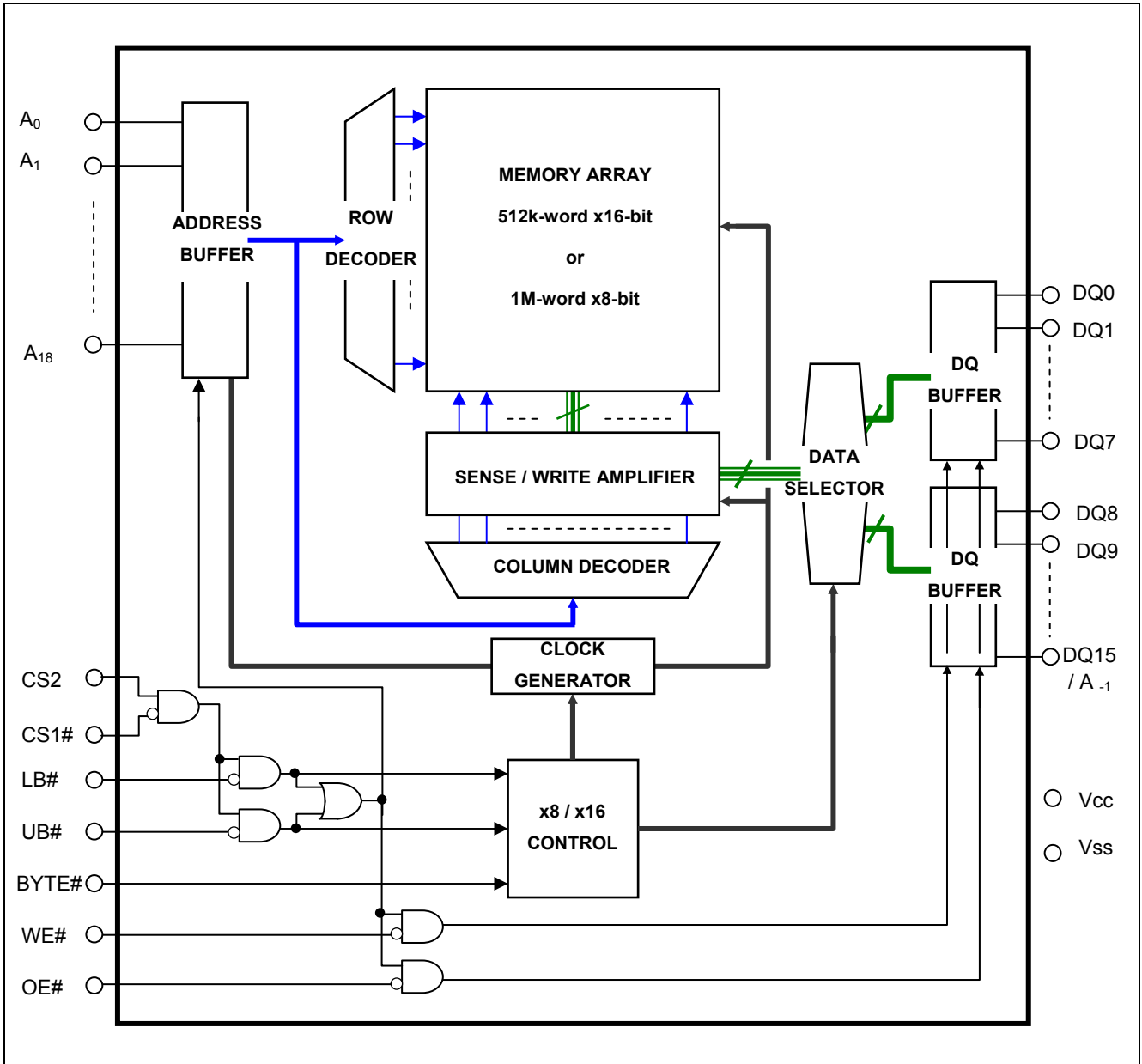
Pin Arrangement



Pin Description

Pin name	Function
V _{CC}	Power supply
V _{SS}	Ground
A0 to A18	Address input (word mode)
A-1 to A18	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
BYTE#	Byte control mode enable
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	BYTE#	UB#	LB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	H	L	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	H	L	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	H	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	L	H	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	X	X	L	X	Din	High-Z	A-1	Byte write
L	H	L	X	X	H	L	Dout	High-Z	A-1	Byte read
L	H	L	X	X	H	H	High-Z	High-Z	A-1	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5^2 to $V_{CC}+0.3^3$	V
Power dissipation	P_T	0.7	W
Operation temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to +150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Note 2. -3.0V for pulse \leq 30ns (full width at half maximum)

3. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Supply voltage	V_{CC}	2.4	3.0	3.6	V		
	V_{SS}	0	0	0	V		
Input high voltage	V_{IH}	2.0	—	$V_{CC}+0.2$	V	$V_{CC}=2.4V$ to 2.7V	
		2.2	—	$V_{CC}+0.2$	V	$V_{CC}=2.7V$ to 3.6V	
Input low voltage	V_{IL}	-0.2	—	0.4	V	$V_{CC}=2.4V$ to 2.7V	4
		-0.2	—	0.6	V	$V_{CC}=2.7V$ to 3.6V	4
Ambient temperature range	T_a	-40	—	+85	°C		

Note 4. -3.0V for pulse \leq 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	μA	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH} , $V_{I/O} = V_{SS} \text{ to } V_{CC}$
Average operating current	I_{CC1}	—	20^{*5}	25	mA	Cycle = 55ns, duty = 100%, $I_{I/O} = 0\text{mA}$, BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}
		—	25^{*5}	30	mA	Cycle = 45ns, duty = 100%, $I_{I/O} = 0\text{mA}$, BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}
	I_{CC2}	—	1.5^{*5}	3	mA	Cycle = 1 μs , duty = 100%, $I_{I/O} = 0\text{mA}$, BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# $\leq 0.2\text{V}$, CS2 $\geq V_{CC} - 0.2\text{V}$, $V_{IH} \geq V_{CC} - 0.2\text{V}$, $V_{IL} \leq 0.2\text{V}$
Standby current	I_{SB}	—	—	0.3	mA	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS2 = V_{IL} , Others = $V_{SS} \text{ to } V_{CC}$
Standby current	I_{SB1}	—	0.45^{*5}	2	μA	$\sim +25^{\circ}\text{C}$ Vin = $V_{SS} \text{ to } V_{CC}$, BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$
		—	0.6^{*6}	4	μA	$\sim +40^{\circ}\text{C}$ (1) CS2 $\leq 0.2\text{V}$ or
		—	—	7	μA	$\sim +70^{\circ}\text{C}$ (2) CS1# $\geq V_{CC} - 0.2\text{V}$, CS2 $\geq V_{CC} - 0.2\text{V}$ or
		—	—	10	μA	$\sim +85^{\circ}\text{C}$ (3) LB# = UB# $\geq V_{CC} - 0.2\text{V}$, CS1# $\leq 0.2\text{V}$, CS2 $\geq V_{CC} - 0.2\text{V}$
Output high voltage	V_{OH}	2.4	—	—	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OH} = -1\text{mA}$ $V_{CC} \geq 2.7\text{V}$
	V_{OH2}	2.0	—	—	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OH} = -0.1\text{mA}$
Output low voltage	V_{OL}	—	—	0.4	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OL} = 2\text{mA}$ $V_{CC} \geq 2.7\text{V}$
	V_{OL2}	—	—	0.4	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OL} = 0.1\text{mA}$

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 25^{\circ}\text{C}$), and not 100% tested.

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 40^{\circ}\text{C}$), and not 100% tested.

Capacitance

($T_a = 25^{\circ}\text{C}$, $f = 1\text{MHz}$)

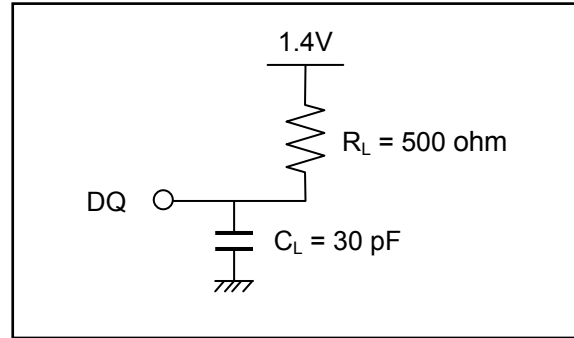
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0\text{V}$	7
Input / output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0\text{V}$	7

Note 7. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($V_{CC} = 2.4V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels:
 $V_{IL} = 0.4V$, $V_{IH} = 2.4V$ ($V_{CC}=2.7V$ to $3.6V$)
 $V_{IL} = 0.4V$, $V_{IH} = 2.2V$ ($V_{CC}=2.4V$ to $2.7V$)
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	$V_{CC}=2.7V$ to $3.6V$		$V_{CC}=2.4V$ to $2.7V$		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	45	—	55	—	ns	
Address access time	t_{AA}	—	45	—	55	ns	
Chip select access time	t_{ACS1}	—	45	—	55	ns	
	t_{ACS2}	—	45	—	55	ns	
Output enable to output valid	t_{OE}	—	22	—	30	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	—	55	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	8,9
	t_{CLZ2}	10	—	10	—	ns	8,9
LB#, UB# enable to low-Z	t_{BLZ}	5	—	5	—	ns	8,9
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	8,9
Chip deselect to output in high-Z	t_{CHZ1}	0	18	0	20	ns	8,9,10
	t_{CHZ2}	0	18	0	20	ns	8,9,10
LB#, UB# disable to high-Z	t_{BHZ}	0	18	0	20	ns	8,9,10
Output disable to output in high-Z	t_{OHZ}	0	18	0	20	ns	8,9,10

Note 8. This parameter is sampled and not 100% tested.

9. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

10. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	45	—	55	—	ns	
Address valid to write end	t_{AW}	35	—	50	—	ns	
Chip select to write end	t_{CW}	35	—	50	—	ns	
Write pulse width	t_{WP}	35	—	40	—	ns	11
LB#,UB# valid to write end	t_{BW}	35	—	50	—	ns	
Address setup time to write start	t_{AS}	0	—	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	0	—	ns	
Data to write time overlap	t_{DW}	25	—	25	—	ns	
Data hold from write end	t_{DH}	0	—	0	—	ns	
Output enable from write end	t_{OW}	5	—	5	—	ns	12
Output disable to output in high-Z	t_{OHZ}	0	18	0	20	ns	12,13
Write to output in high-Z	t_{WHZ}	0	18	0	20	ns	12,13

Note 11. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

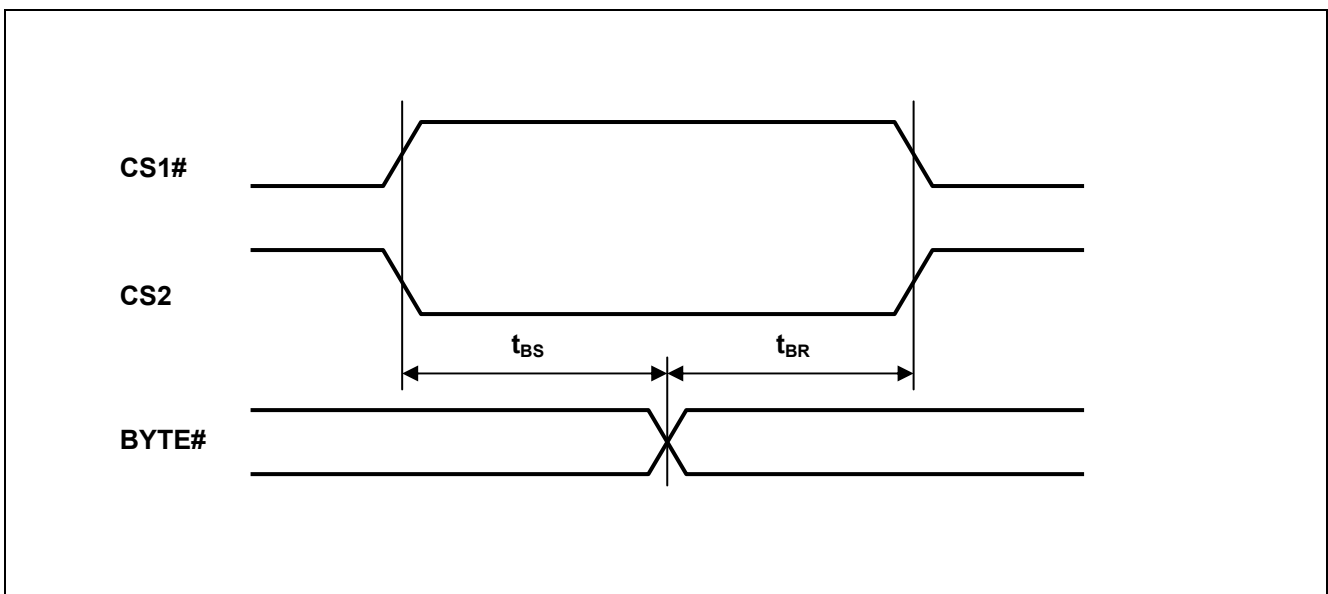
12. This parameter is sampled and not 100% tested.

13. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

BYTE# Timing Conditions

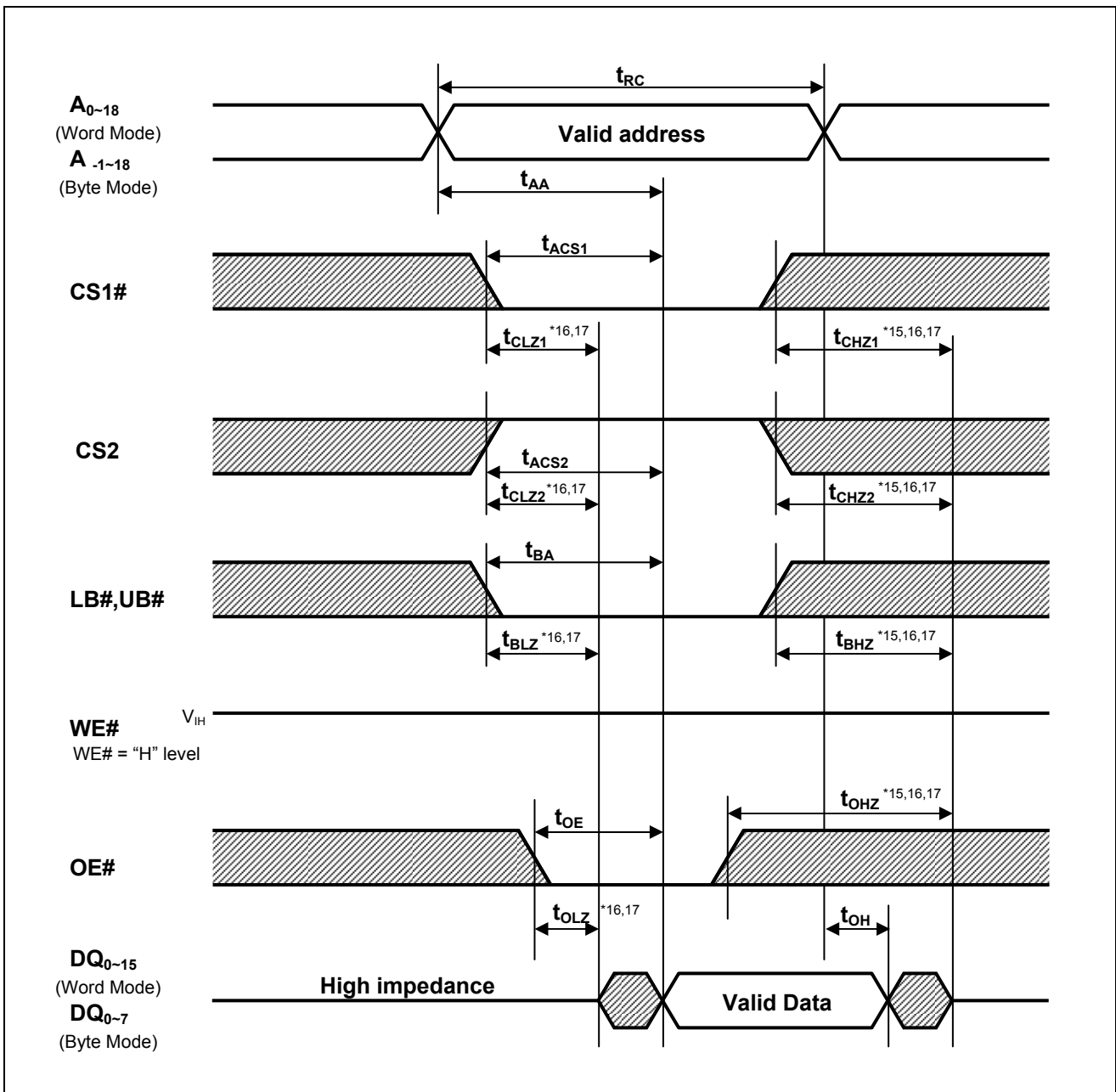
Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Byte setup time	t_{BS}	5	—	5	—	ms	
Byte recovery time	t_{BR}	5	—	5	—	ms	

BYTE# Timing Waveforms



Timing Waveforms

Read Cycle^{*14}



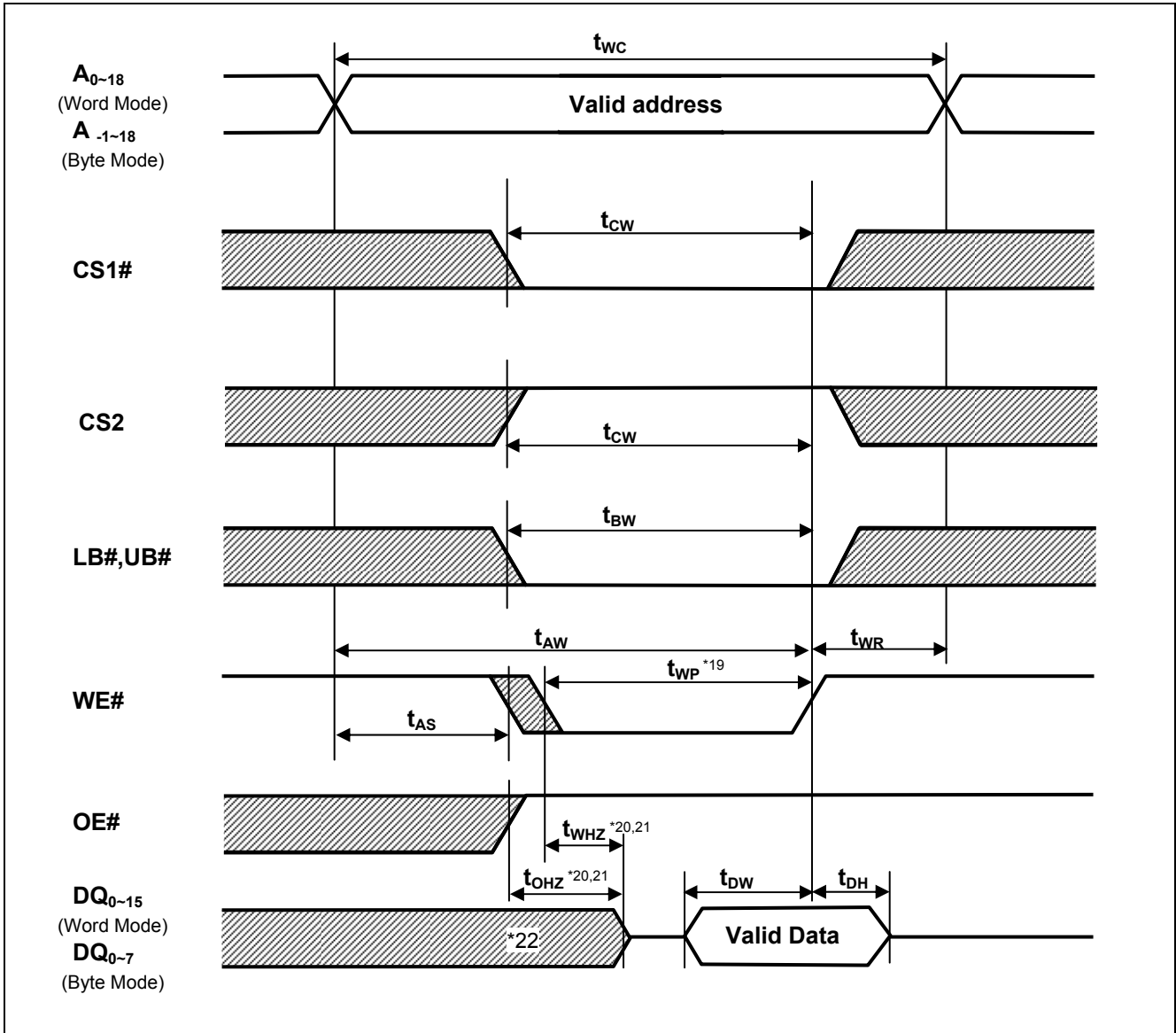
Note 14. BYTE# $\geq V_{CC} - 0.2V$ or BYTE# $\leq 0.2V$

15. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

16. This parameter is sampled and not 100% tested

17. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1)^{*18} (WE# CLOCK, OE#="H" while writing)



Note 18. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

19. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

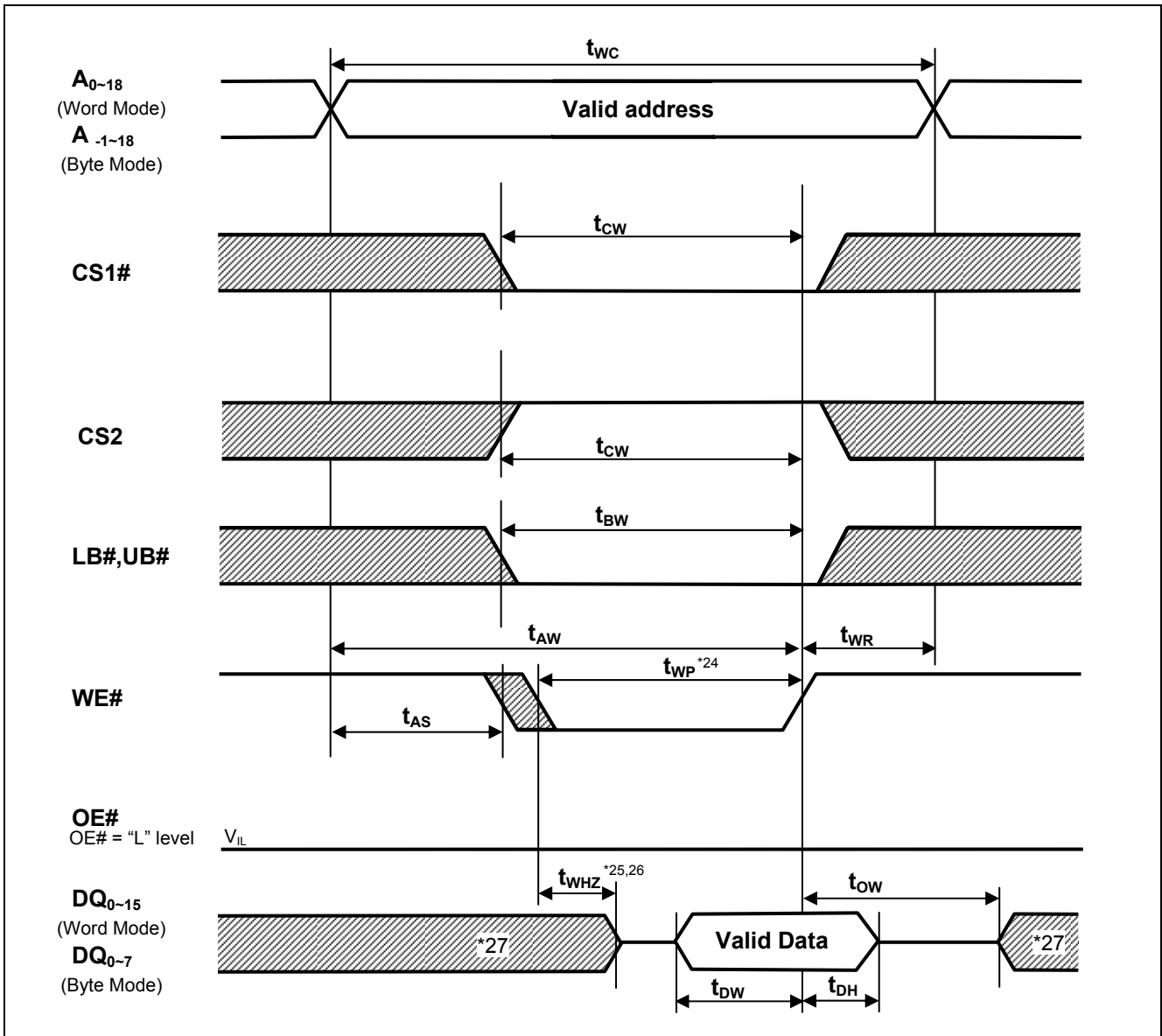
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

20. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

21. This parameter is sampled and not 100% tested

22. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2)^{*23} (WE# CLOCK, OE# Low Fixed)



Note 23. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

24. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

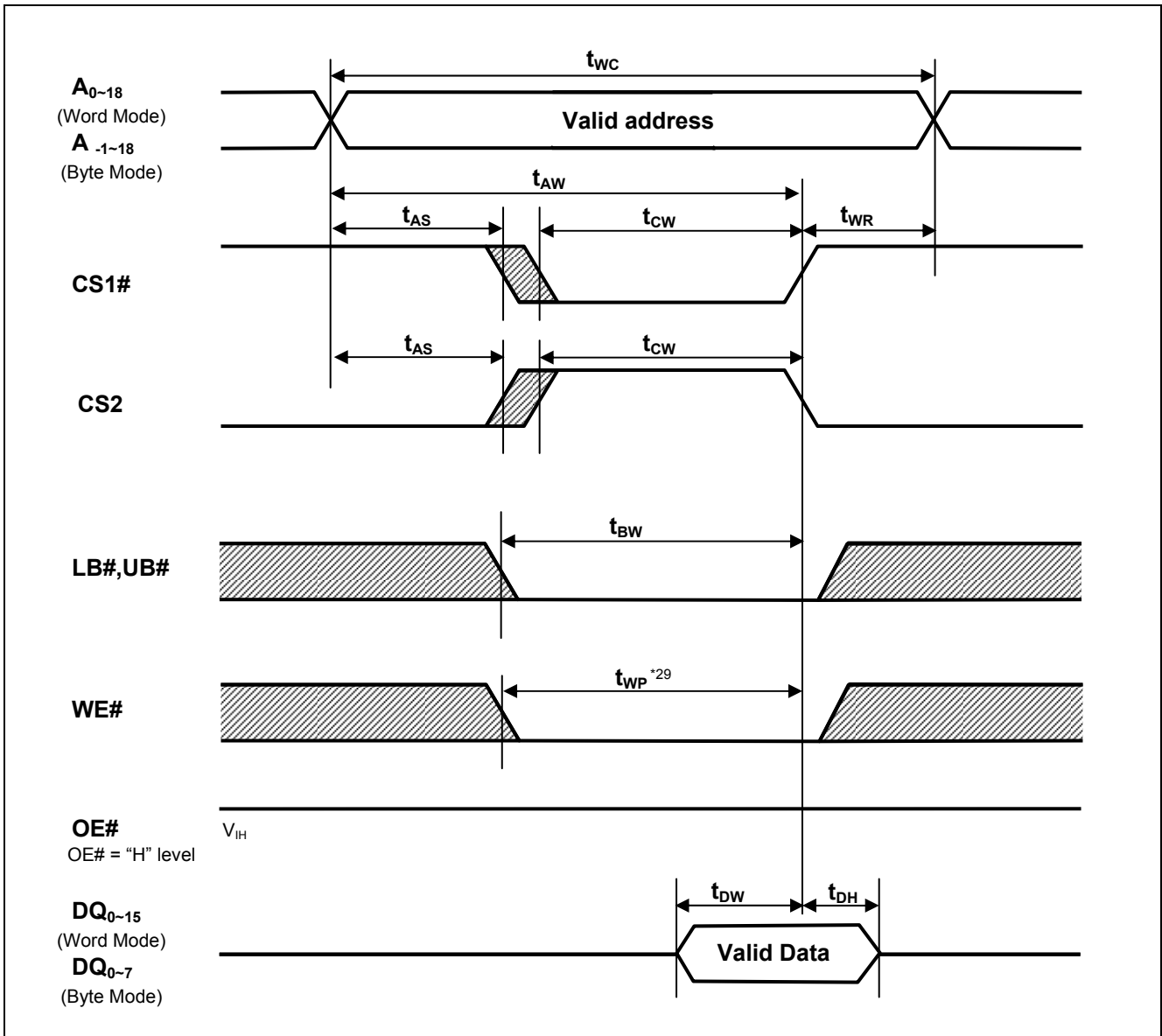
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

25. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

26. This parameter is sampled and not 100% tested.

27. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3)^{*28} (CS1#, CS2 CLOCK)



Note 28. BYTE# ≥ V_{CC} - 0.2V or BYTE# ≤ 0.2V

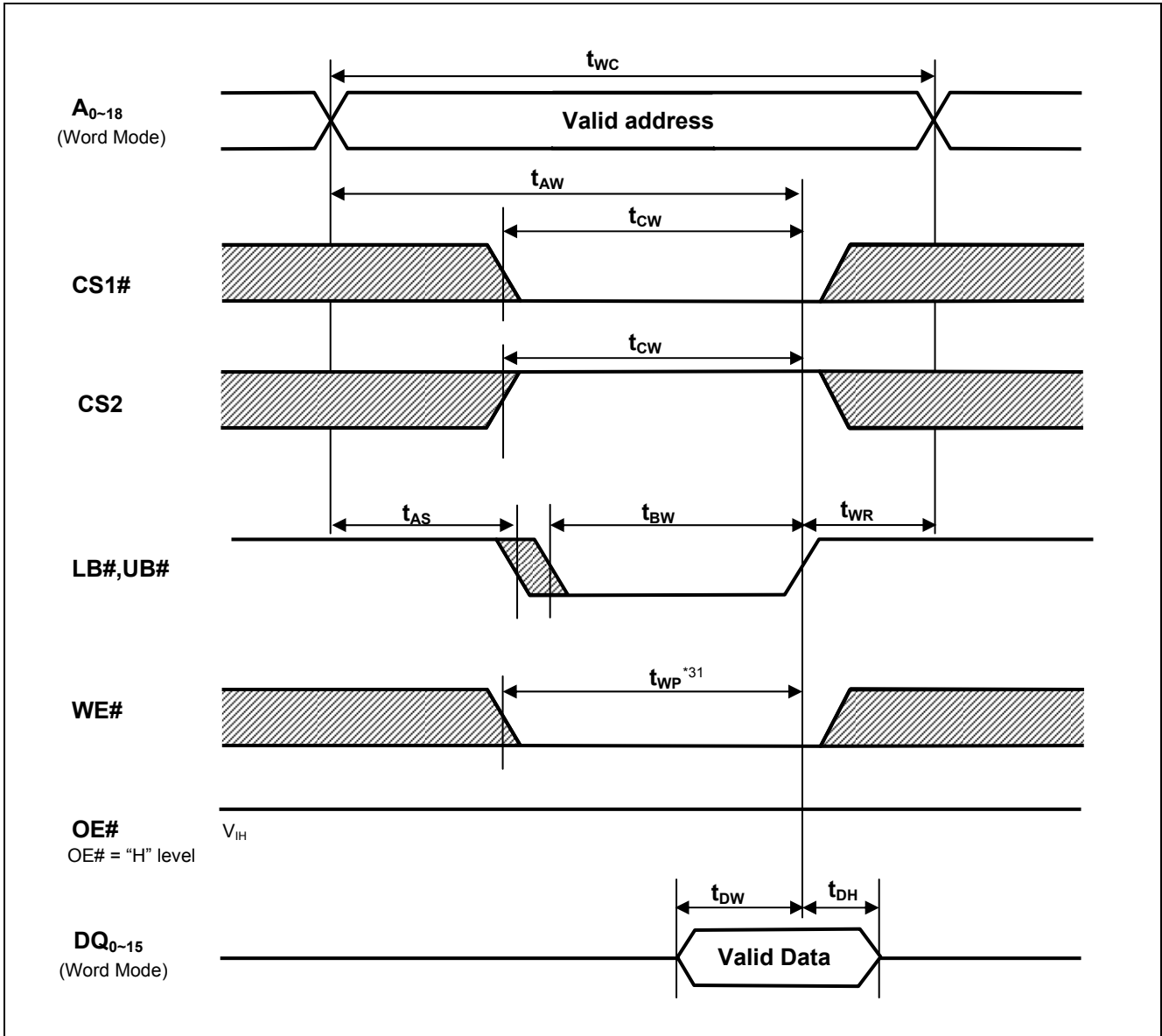
29. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4)^{*30} (LB#, UB# CLOCK, Word Mode)



Note 30. BYTE# $\geq V_{CC} - 0.2V$

31. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V_{CC} Data Retention Characteristics

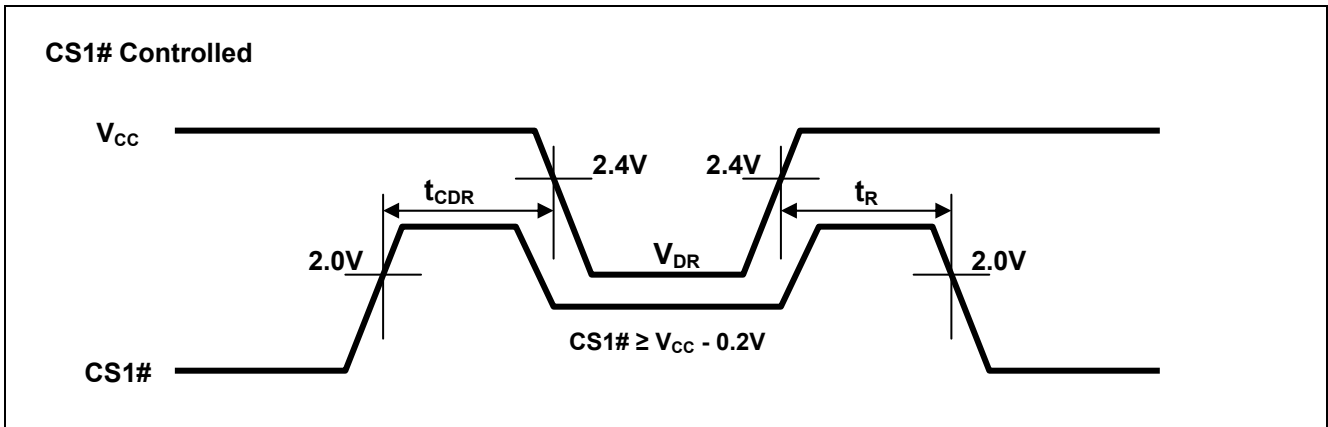
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*34}	
V_{CC} for data retention	V_{DR}	1.5	—	3.6	V	$V_{in} \geq 0V$, $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$ (1) $CS2 \leq 0.2V$ or (2) $CS1\# \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or (3) $LB\# = UB\# \geq V_{CC} - 0.2V$, $CS1\# \leq 0.2V$, $CS2 \geq V_{CC} - 0.2V$	
Data retention current	I_{CCDR}	—	0.45 ^{*32}	2	μA	$\sim +25^{\circ}C$	$V_{CC} = 3.0V$, $V_{in} \geq 0V$, $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$ (1) $CS2 \leq 0.2V$ or (2) $CS1\# \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or (3) $LB\# = UB\# \geq V_{CC} - 0.2V$, $CS1\# \leq 0.2V$, $CS2 \geq V_{CC} - 0.2V$
		—	0.6 ^{*33}	4	μA	$\sim +40^{\circ}C$	
		—	—	7	μA	$\sim +70^{\circ}C$	
		—	—	10	μA	$\sim +85^{\circ}C$	
Chip deselect time to data retention	t_{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t_R	5	—	—	ms		

Note 32. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 25^{\circ}C$), and not 100% tested.

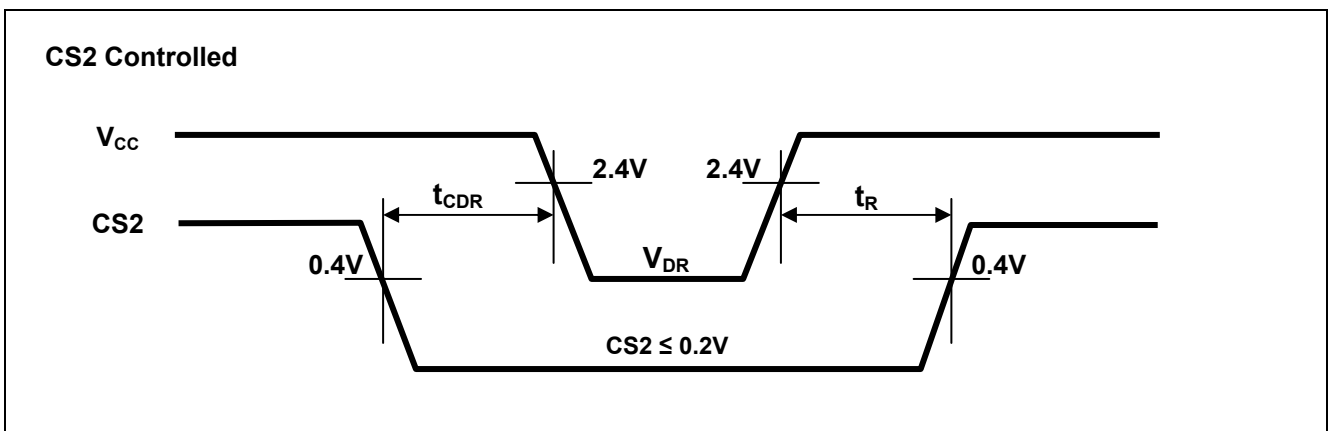
33. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 40^{\circ}C$), and not 100% tested.

34. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.

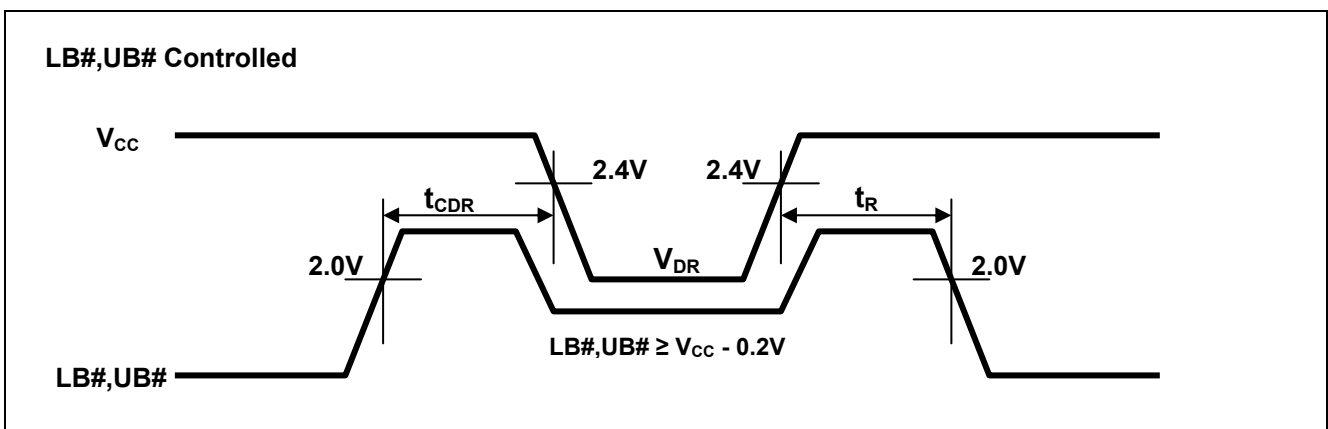
Low Vcc Data Retention Timing Waveforms (CS1# controlled)^{*35}



Low Vcc Data Retention Timing Waveforms (CS2 controlled)^{*35}



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled, Word Mode)^{*36}



Note 35. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

36. $BYTE\# \geq V_{CC} - 0.2V$

Revision History	RMLV0816BGSD Data Sheet
------------------	-------------------------

Rev.	Date	Description	
		Page	Summary
1.00	2014.11.28	—	First Edition issued
2.00	2015.06.26	P.1, 5 P.5 P.13	Standby current I_{SB1} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.) Average operating current I_{CC2} : 25°C 2mA ->1.5mA (typ.) Data retention current I_{CCDR} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.)

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
3. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics product.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; and safety equipment etc.
Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (nuclear reactor control systems, military equipment etc.). You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application for which it is not intended. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.
6. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You should not use Renesas Electronics products or technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. When exporting the Renesas Electronics products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the contents and conditions set forth in this document, Renesas Electronics assumes no responsibility for any losses incurred by you or third parties as a result of unauthorized use of Renesas Electronics products.
11. This document may not be reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhichunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0899

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-8688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141