

N-channel 600 V, 0.370 Ω typ., 10 A MDmesh™ DM2 Power MOSFET in a DPAK package

Datasheet - production data

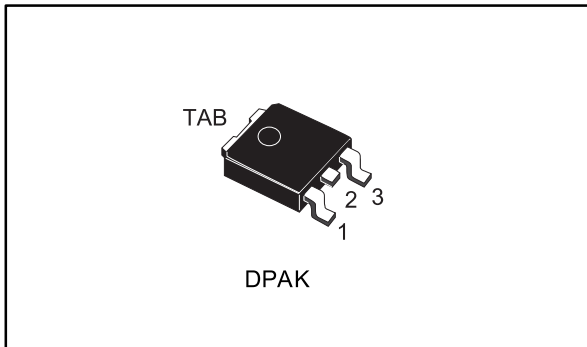
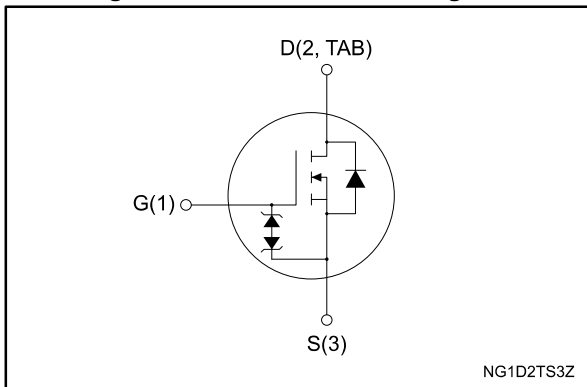


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ $T_{Jmax.}$	$R_{DS(on)}$ max.	I_D	P_{TOT}
STD11N60DM2	650 V	0.420 Ω	10 A	110 W

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

This high voltage N-channel Power MOSFET is part of the MDmesh™ DM2 fast recovery diode series. It offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering it suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STD11N60DM2	11N60DM2	DPAK	Tape and reel

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	10	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	6.3	
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	110	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	40	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

Notes:

- (1) Pulse width is limited by safe operating area.
 (2) $I_{SD} \leq 10\text{ A}$, $di/dt=900\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$
 (3) $V_{DS} \leq 480\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	1.14	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-ambient	50	

Notes:

- (1) When mounted on 1 inch² FR-4 board, 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive	2.5	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	250	mJ

Notes:

- (1) pulse width limited by T_{jmax}
 (2) starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$			1.5	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 600\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			100	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 25\text{ V}$			± 10	μA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 5\text{ A}$		0.370	0.420	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	614	-	pF
C_{OSS}	Output capacitance		-	32	-	
C_{RSS}	Reverse transfer capacitance		-	1.08	-	
$C_{\text{OSS eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$, $V_{\text{GS}} = 0\text{ V}$	-	57	-	pF
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	6.2	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 480\text{ V}$, $I_{\text{D}} = 10\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	16.5	-	nC
Q_{gs}	Gate-source charge		-	3.8	-	
Q_{gd}	Gate-drain charge		-	9.2	-	

Notes:

⁽¹⁾ $C_{\text{OSS eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{OSS} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$, $I_{\text{D}} = 5\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	11.7	-	ns
t_{r}	Rise time		-	6.3	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	31	-	
t_{f}	Fall time		-	9.5	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		10	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		40	A
$V_{SD}^{(3)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$, $I_{SD} = 10 \text{ A}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 10 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	90		ns
Q_{rr}	Reverse recovery charge		-	248		μC
I_{RRM}	Reverse recovery current		-	5.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 10 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	160		ns
Q_{rr}	Reverse recovery charge		-	664		nC
I_{RRM}	Reverse recovery current		-	8.3		A

Notes:

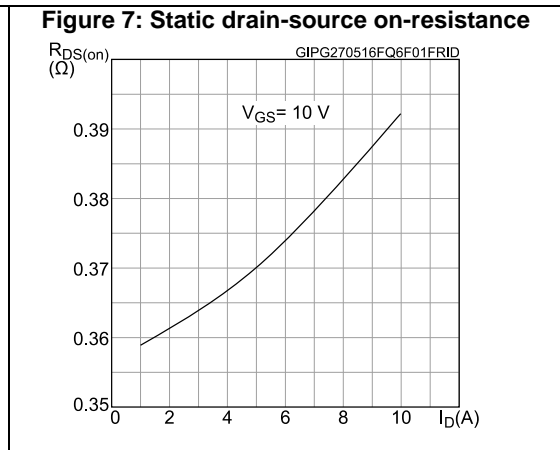
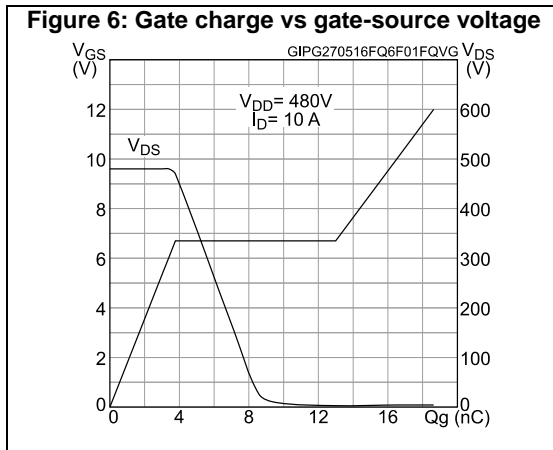
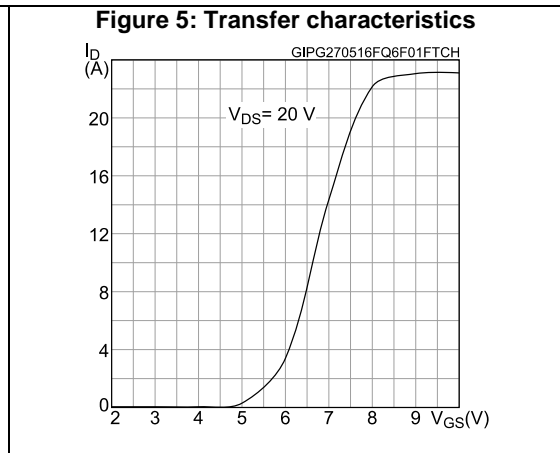
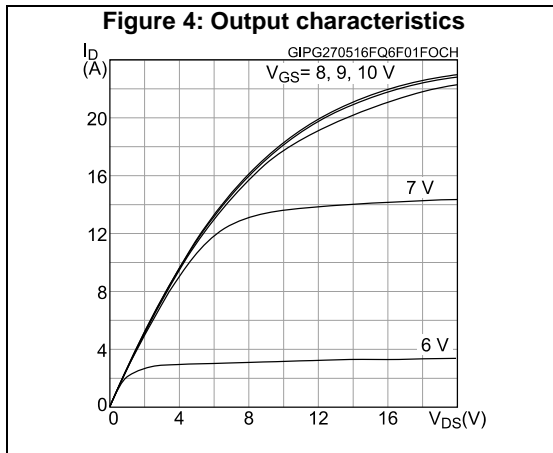
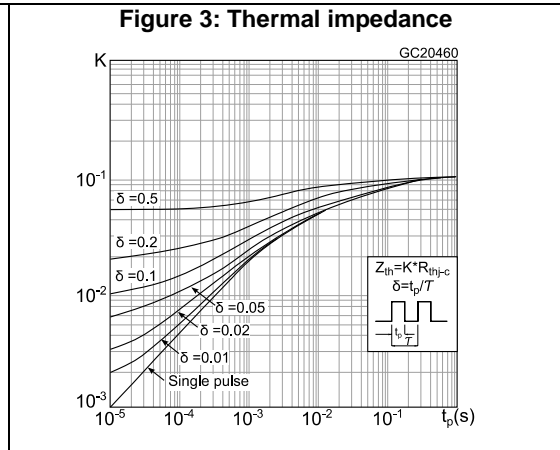
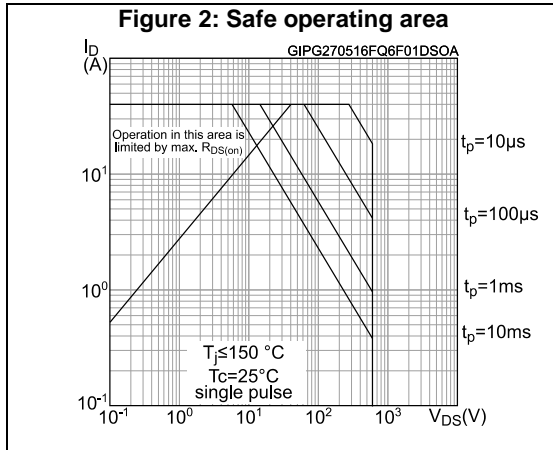
- (1) Limited by maximum junction temperature.
(2) Pulse width is limited by safe operating area.
(3) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

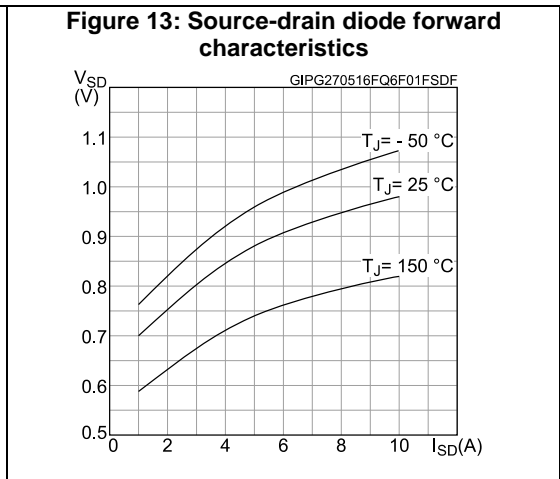
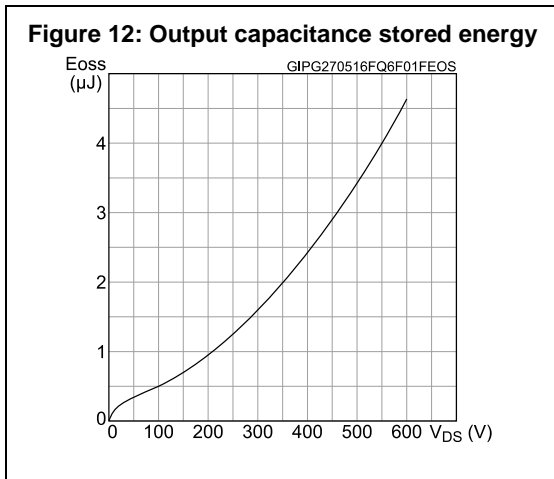
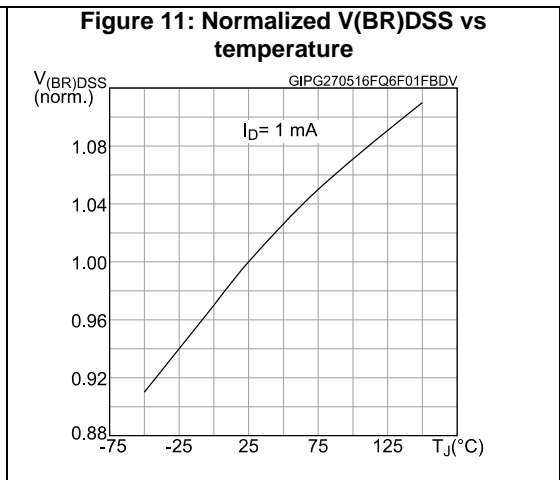
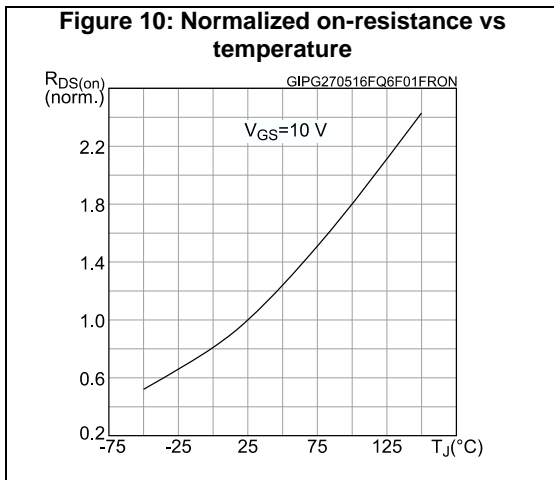
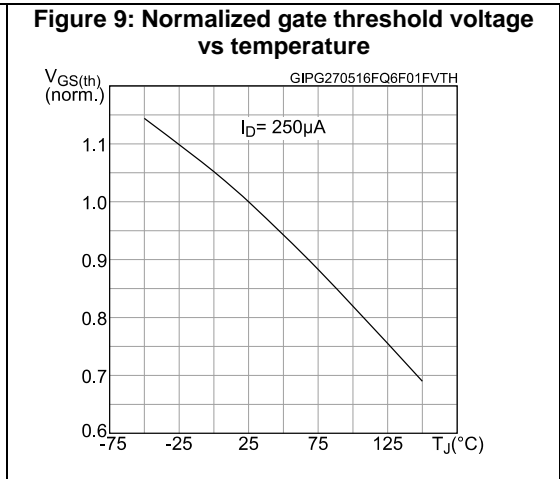
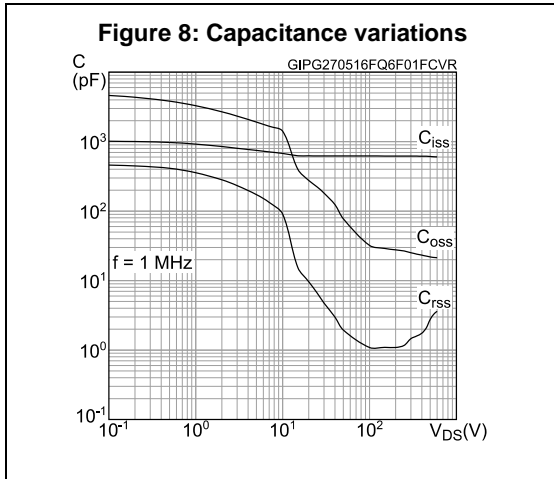
Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 250 \mu\text{A}$, $I_D = 0 \text{ A}$	± 30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

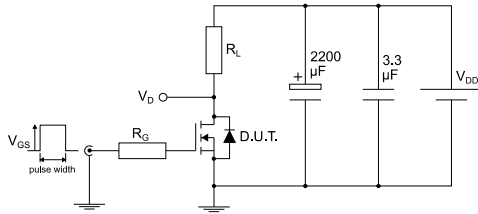
2.1 Electrical characteristics (curves)





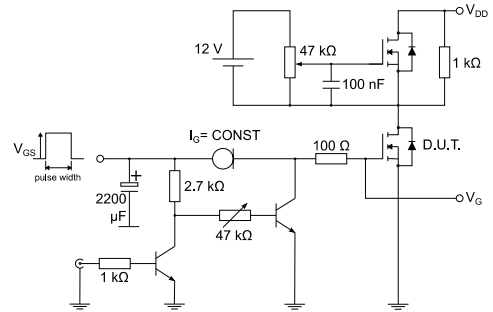
3 Test circuits

Figure 14: Test circuit for resistive load switching times



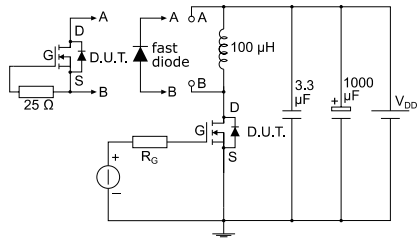
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Figure 15: Test circuit for gate charge behavior



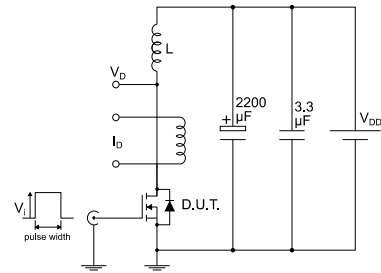
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Figure 16: Test circuit for inductive load switching and diode recovery times



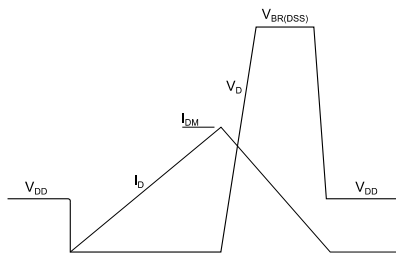
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Figure 17: Unclamped inductive load test circuit



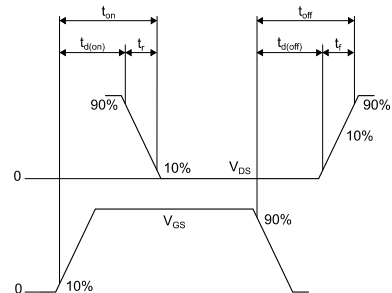
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



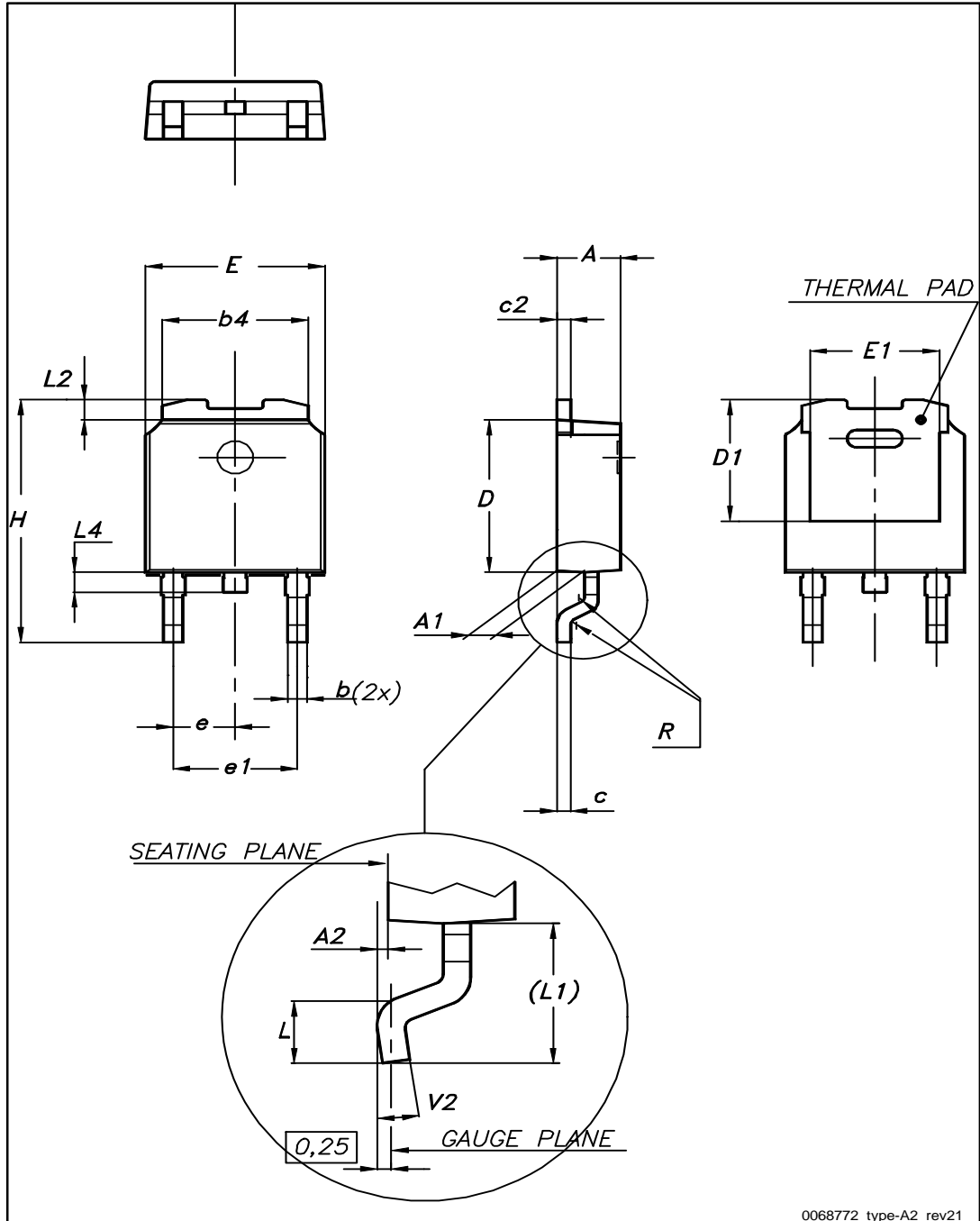
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 20: DPAK (TO-252) type A2 package outline

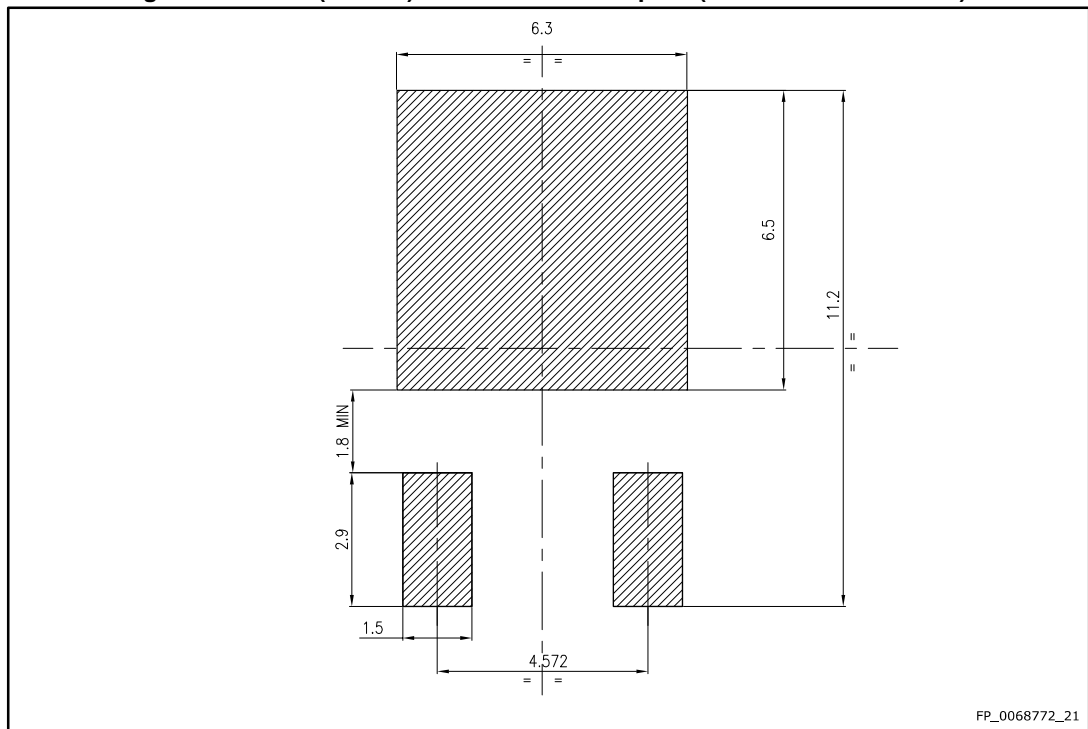


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Table 10: DPAK (TO-252) type A2 mechanical data

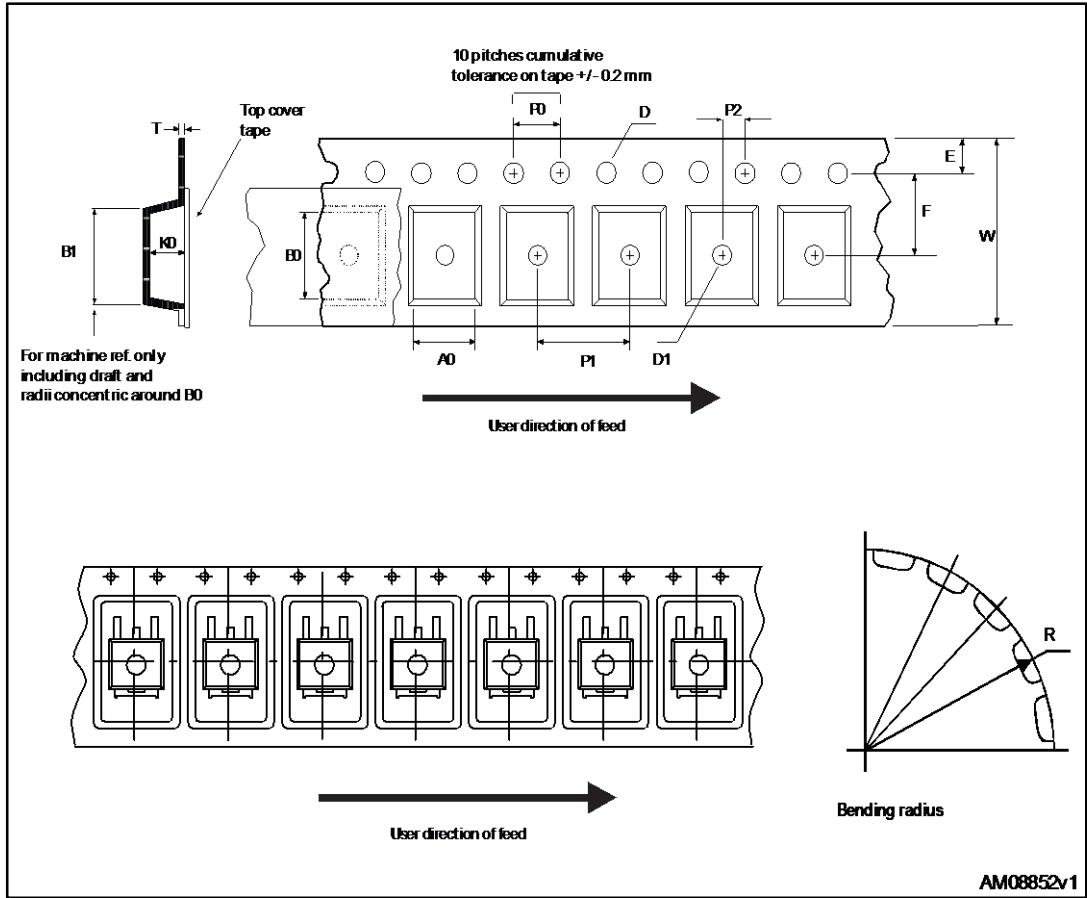
Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 22: DPAK (TO-252) tape outline



5 Revision history

Table 12: Document revision history

Date	Revision	Changes
17-Jun-2016	1	First release.

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