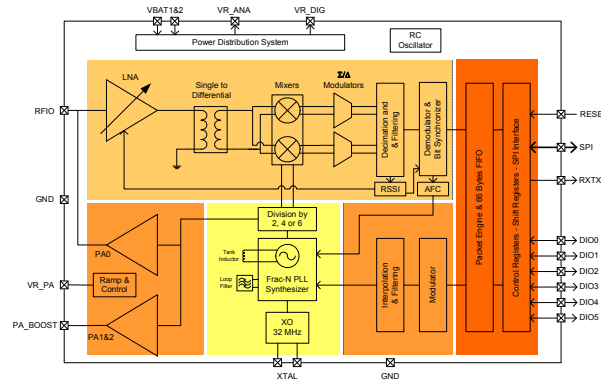## SX1231J Transceiver

Low Power Integrated UHF Transceiver

GENERAL DESCRIPTION

The SX1231J is an ARIB compliant highly integrated RF transceiver which operates over all Japanese sub-GHz frequency bands. Its highly integrated digital architecture minimizes external components and provides flexibility for optimizing the system parameters and performance. The high sensitivity and exceptional blocking performance combined with optimized IIP3 maximizes the range in harshest environments. The industries lowest sleep current, fastest wake times, and low receive current extend the battery life for any application. The transmit output power is programmable up to +17dBm and delivers constant performance over the battery voltage lifetime. TrueRF™ technology enables a low-cost external component count (eliminating SAW filter) while still satisfying ARIB, FCC, and ETSI regulations. The device supports IEEE 15.4d/g mandatory modes.

APPLICATIONS

- Smart metering and IEEE15.4d/g
- Wireless sensor networks
- Home and building automation
- Wireless alarm and security systems
- Industrial monitoring and control
- Active RFID tags
- Remote keyless entry (RKE) and automotive

MARKETS

- Japan: ARIB STD-T67 from 426 to 470 MHz
- Japan: ARIB STD-T108 from 915 to 930 MHz

KEY PRODUCT FEATURES

- High Sensitivity: down to -120 dBm at 1.2 kbps
- Robust Selectivity: 42dB at 25kHz offset
- Bullet-proof front end: IIP3 = -18 dBm, IIP2 = +35 dBm, 80 dB Blocking Immunity, no Image Frequency response
- Low current receive mode = 16 mA
- Low current sleep mode with register retention =100nA
- Programmable TX Power: -18 to +17 dBm in 1dB steps
- Constant RF performance over VDD voltage range
- FSK bit rates up to 300 kb/s
- Fully integrated synthesizer with a resolution of 61 Hz
- FSK, GFSK, MSK, GMSK and OOK modulations
- Built-in bit synchronizer for clock recovery
- Incoming sync word recognition
- 115 dB+ dynamic range RSSI
- Automatic RF sense with ultra-fast AFC
- Packet engine with CRC, AES-128, and 66-byte FIFO
- Built-in temperature sensor and low battery indicator

ORDERING INFORMATION

Part Number	Package	Delivery	MOQ / Multiple
SX1231JIMLTRT	QFN24	Tape & Reel	3000 pieces

- Pb-free, Halogen free, RoHS/WEEE compliant product

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Acronyms

BOM	Bill Of Materials	LSB	Least Significant Bit
BR	Bit Rate	MSB	Most Significant Bit
BW	Bandwidth	NRZ	Non Return to Zero
CCITT	Comité Consultatif International Téléphonique et Télégraphique - ITU	OOK	On Off Keying
CRC	Cyclic Redundancy Check	PA	Power Amplifier
DAC	Digital to Analog Converter	PCB	Printed Circuit Board
ETSI	European Telecommunications Standards Institute	PLL	Phase-Locked Loop
FCC	Federal Communications Commission	POR	Power On Reset
Fdev	Frequency Deviation	RBW	Resolution BandWidth
FIFO	First In First Out	RF	Radio Frequency
FIR	Finite Impulse Response	RSSI	Received Signal Strength Indicator
FS	Frequency Synthesizer	Rx	Receiver
FSK	Frequency Shift Keying	SAW	Surface Acoustic Wave
GUI	Graphical User Interface	SPI	Serial Peripheral Interface
IC	Integrated Circuit	SR	Shift Register
ID	IDentificator	Stby	Standby
IF	Intermediate Frequency	Tx	Transmitter
IRQ	Interrupt ReQuest	uC	Microcontroller
ITU	International Telecommunication Union	VCO	Voltage Controlled Oscillator
LFSR	Linear Feedback Shift Register	XO	Crystal Oscillator
LNA	Low Noise Amplifier	XOR	eXclusive OR
LO	Local Oscillator		

This product datasheet contains a detailed description of the SX1231J performance and functionality. Please consult the Semtech website **www.semtech.com** for the latest updates or errata.

1. General Description

The SX1231J is a single-chip integrated circuit ideally suited for today's high performance ISM band RF applications. The SX1231J's advanced features set, including state of the art packet engine greatly simplifies system design whilst the high level of integration reduces the external BOM to a handful of passive decoupling and matching components. It is intended for use as high-performance, low-cost FSK and OOK RF transceiver for robust frequency agile, half-duplex bi-directional RF links, and where stable and constant RF performance is required over the full operating range of the device down to 1.8V.

Coupled with a link budget in excess of 135 dB, the advanced system features of the SX1231J include a 66 byte TX/RX FIFO, configurable automatic packet handler, listen mode, temperature sensor and configurable DIOs which greatly enhance system flexibility whilst at the same time significantly reducing MCU requirements.

The SX1231J complies with Japanese ARIB regulatory requirements and is available in a 5x 5 mm QFN 24 lead package.

1.1. Simplified Block Diagram
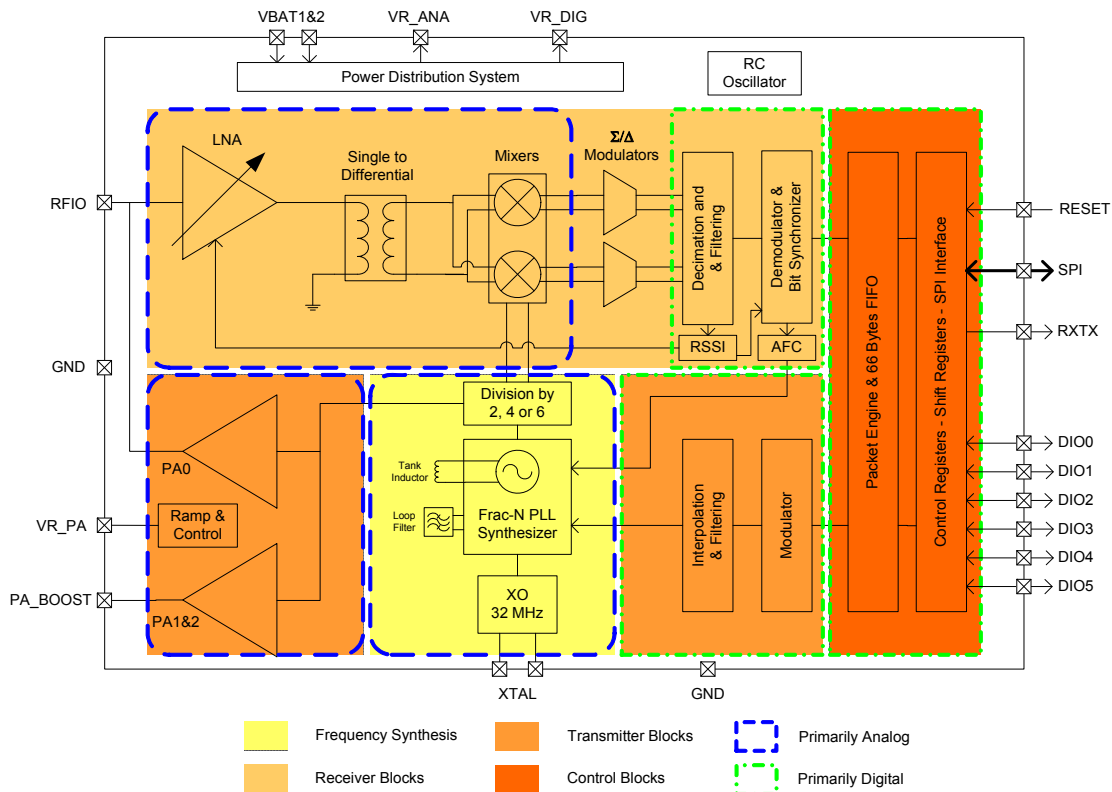
Figure 1.   Block Diagram

1.2. Pin and Marking Diagram

The following diagram shows the pin arrangement of the SX1231J, top view.
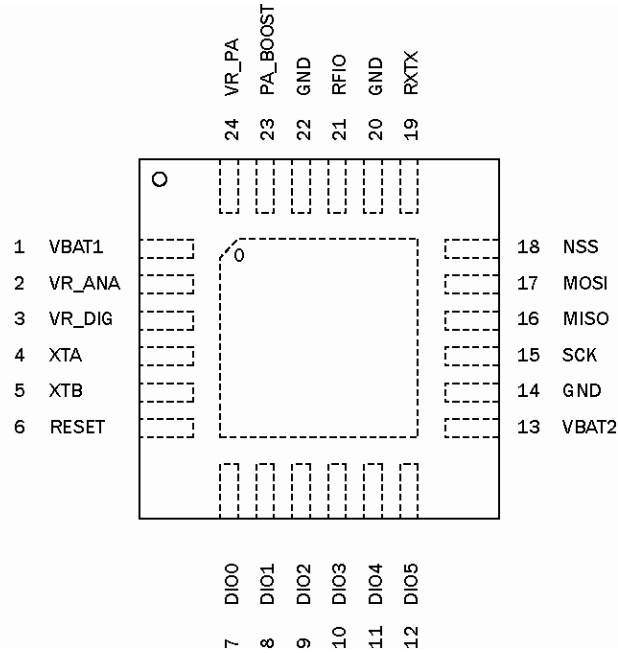
Figure 2.   Pin Diagram (not to scale)
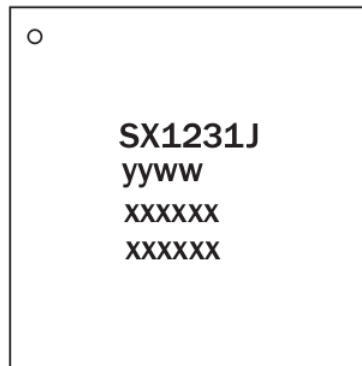
Figure 3.   Marking Diagram

Notes   yyww refers to the date code

xxxxxx refers to the lot number

1.3. Pin Description

Table 1   SX1231J Pinouts

Pin Number		Name	Type	Description
QFN	TSSOP			
0	-	GROUND	-	Exposed ground pad
1	12	VBAT1	-	Supply voltage
2	13	VR_ANA	-	Regulated supply voltage for analogue circuitry
3	14	VR_DIG	-	Regulated supply voltage for digital blocks
4	15	XTA	I/O	XTAL connection
5	16	XTB	I/O	XTAL connection
6	17	RESET	I/O	Reset trigger input
-	18	GND	-	Ground
7	19	DIO0	I/O	Digital I/O, software configured
8	20	DIO1/DCLK	I/O	Digital I/O, software configured
9	21	DIO2/DATA	I/O	Digital I/O, software configured
10	22	DIO3	I/O	Digital I/O, software configured
11	23	DIO4	I/O	Digital I/O, software configured
12	24	DIO5	I/O	Digital I/O, software configured
-	25	GND	-	Ground
13	26	VBAT2	-	Supply voltage
14	27	GND	-	Ground
15	28	SCK	I	SPI Clock input
16	1	MISO	O	SPI Data output
17	2	MOSI	I	SPI Data input
18	3	NSS	I	SPI Chip select input
19	4	RXTX	O	Rx/Tx switch control: high in Tx
20	5	GND	-	Ground
21	6	RFIO	I/O	RF input / output
22	7	GND	-	Ground
23	8	PA_BOOST	O	Optional high-power PA output
-	9	GND	-	Ground
24	10	VR_PA	-	Regulated supply for the PA
-	11	GND	-	Ground

Note   PA_BOOST can be left floating if unused

2. Electrical Characteristics

2.1. ESD Notice

The SX1231J is a high performance radio frequency device. It satisfies:

◆ Class 2 of the JEDEC standard JESD22-A114-B (Human Body Model) on all pins.

◆ Class B of the JEDEC standard JESD22-A115-A (Machine Model) on all pins.

◆ Class IV of the JEDEC standard JESD22-C101C (Charged Device Model) on pins VR_ANA, VR_DIG, RFIO, PA_BOOST, VR_PA, Class III on all other pins.

It should thus be handled with all the necessary ESD precautions to avoid any permanent damage.

2.2. Absolute Maximum Ratings

Stresses above the values listed below may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Table 2   Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit
VDDmr	Supply Voltage	-0.5	3.9	V
Tmr	Temperature	-55	+115	° C
Tj	Junction temperature	-	+125	° C
Pmr	RF Input Level	-	+6	dBm

2.3. Operating Range

Table 3   Operating Range

Symbol	Description	Min	Max	Unit
VDDop	Supply voltage	1.8	3.6	V
Top	Operational temperature range	-40	+85	°C
Clop	Load capacitance on digital ports	-	25	pF
ML	RF Input Level	-	0	dBm

2.4. Chip Specification

The tables below give the electrical specifications of the transceiver under the following conditions: Supply voltage VBAT1= VBAT2=VDD=3.3 V, temperature = 25 °C, *FXOSC* = 32 MHz, F_{RF} = 915 MHz, Pout = +13dBm, 2-level FSK modulation without pre-filtering, FDA = 5 kHz, Bit Rate = 4.8 kb/s and terminated in a matched 50 Ohm impedance, unless otherwise specified.

Note   Unless otherwise specified, the performances in the other frequency bands are similar or better.

2.4.1. Power Consumption

Table 4   Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
IDDSL	Supply current in Sleep mode		-	0.1	1	uA
IDDIDLE	Supply current in Idle mode	RC oscillator enabled	-	1.2	-	uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	-	1.25	1.5	mA
IDDFS	Supply current in Synthesizer mode		-	9	-	mA
IDDR	Supply current in Receive mode		-	16	-	mA
IDDT	Supply current in Transmit mode with appropriate matching, stable across VDD range	RFOP = +17 dBm, on PA_BOOST RFOP = +13 dBm, on RFIO pin RFOP = +10 dBm, on RFIO pin RFOP = 0 dBm, on RFIO pin RFOP = -1 dBm, on RFIO pin	- - - - -	95 45 33 20 16	- - - - -	mA mA mA mA mA

2.4.2. Frequency Synthesis

Table 5   Frequency Synthesizer Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
FR	Synthesizer Frequency Range	Programmable	424 862	- -	510 1020	MHz MHz
FXOSC	Crystal oscillator frequency	See section 5.1	-	32	-	MHz
TS_OSC	Crystal oscillator wake-up time		-	250	500	us
TS_FS	Frequency synthesizer wake-up time to PllLock signal	From Standby mode	-	80	150	us
TS_HOP	Frequency synthesizer hop time at most 10 kHz away from the target	200 kHz step 1 MHz step 5 MHz step 7 MHz step 12 MHz step 20 MHz step 25 MHz step	- - - - - - -	20 20 50 50 80 80 80	- - - - - - -	us us us us us us us
FSTEP	Frequency synthesizer step	FSTEP = FXOSC/2^{19}	-	61.0	-	Hz

FRC	RC Oscillator frequency	After calibration	-	62.5	-	kHz
BRF	Bit rate, FSK	Programmable	1.2	-	300	kbps
BRO	Bit rate, OOK	Programmable	1.2	-	32.768	kbps
FDA	Frequency deviation, FSK	Programmable FDA + BRF/2 =< 500 kHz	0.6	-	300	kHz

2.4.3. Receiver

All receiver tests are performed with *RxBw* = 10 kHz (Single Side Bandwidth) as programmed in *RegRxBw*, receiving a PN15 sequence with a BER of 0.1% (Bit Synchronizer is enabled), unless otherwise specified. The LNA impedance is set to 200 Ohms, by setting bit *LnaZin* in *RegLna* to 1. Blocking tests are performed with an unmodulated interferer. The wanted signal power for the Blocking Immunity, ACR, IIP2, IIP3 and AMR tests is set 3 dB above the nominal sensitivity level.

Table 6   Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RFS_F	FSK sensitivity, highest LNA gain	FDA = 5 kHz, BR = 1.2 kb/s FDA = 5 kHz, BR = 4.8 kb/s FDA = 40 kHz, BR = 38.4 kb/s	- - -	-118 -114 -105	- - -	dBm dBm dBm
		FDA = 5 kHz, BR = 1.2 kb/s *	-	-120	-	dBm
RFS_O	OOK sensitivity, highest LNA gain	BR = 4.8 kb/s	-	-112	-109	dBm
CCR	Co-Channel Rejection		-13	-10	-	dB
ACR	Adjacent Channel Rejection	Offset = +/- 25 kHz Offset = +/- 50 kHz	- 37	42 42	- -	dB dB
BI	Blocking Immunity	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	66 71 79	- - -	dB dB dB
	Blocking Immunity Wanted signal at sensitivity +16dB	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	62 65 73	- - -	dB dB dB
AMR	AM Rejection, AM modulated interferer with 100% modulation depth, fm = 1 kHz, square	Offset = +/- 1 MHz Offset = +/- 2 MHz Offset = +/- 10 MHz	- - -	66 71 79	- - -	dB dB dB
IIP2	2nd order Input Intercept Point Unwanted tones are 20 MHz above the LO	Lowest LNA gain Highest LNA gain	- -	+75 +35	- -	dBm dBm
IIP3	3rd order Input Intercept point Unwanted tones are 1MHz and 1.995 MHz above the LO	Lowest LNA gain Highest LNA gain	- -23	+20 -18	- -	dBm dBm
BW_SSB	Single Side channel filter BW	Programmable	2.6	-	500	kHz

IMR_OOK	Image rejection in OOK mode	Wanted signal level = -106 dBm	27	30	-	dB
TS_RE	Receiver wake-up time, from PLL locked state to *RxReady*	RxBw = 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	- -	1.7 96	- -	ms us
TS_RE_AGC	Receiver wake-up time, from PLL locked state, AGC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s	-	3.0 163		ms us
TS_RE_AGC &AFC	Receiver wake-up time, from PLL lock state, AGC and AFC enabled	RxBw= 10 kHz, BR = 4.8 kb/s RxBw = 200 kHz, BR = 100 kb/s		4.8 265		ms us
TS_FEI	FEI sampling time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_AFC	AFC Response Time	Receiver is ready	-	$4.T_{bit}$	-	-
TS_RSSI	RSSI Response Time	Receiver is ready	-	$2.T_{bit}$	-	-
DR_RSSI	RSSI Dynamic Range	AGC enabled Min Max	- -	-115 0	- -	dBm dBm

*   *Set SensitivityBoost in RegTestLna to 0x2D to reduce the noise floor in the receiver*

2.4.4. Transmitter

Table 7   Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
RF_OP	RF output power in 50 ohms On RFIO pin	Programmable with 1dB steps Max Min	- -	+13 -18	- -	dBm dBm
RF_OPH	Max RF output power, on PA_BOOST pin	With external match to 50 ohms	-	+17	-	dBm
ΔRF_OP	RF output power stability	From VDD=1.8V to 3.6V	-	+/-0.3	-	dB

PHN	Transmitter Phase Noise	50 kHz Offset from carrier
		       868 / 915 MHz bands
		       434 / 315 MHz bands
			
			-
			-
				
				-95
				-99
					
					-
					-
						dBc/
						Hz

ACP	Transmitter adjacent channel power (measured at 25 kHz off-set)	BT=0.5 . Measurement conditions as defined by EN 300 220-1 V2.1.1	-	-	-37	dBm
TS_TR	Transmitter wake up time, to the first rising edge of DCLK	Frequency Synthesizer enabled, *PaRamp* = 10 us, BR = 4.8 kb/s.	-	120	-	us

2.4.5. Digital Specification

Conditions: Temp = 25°C, VDD = 3.3V, FXOSC = 32 MHz, unless otherwise specified.

Table 8   Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Digital input level high		0.8	-	-	VDD
V_{IL}	Digital input level low		-	-	0.2	VDD
V_{OH}	Digital output level high	Imax = 1 mA	0.9	-	-	VDD
V_{OL}	Digital output level low	Imax = -1 mA	-	-	0.1	VDD
F_{SCK}	SCK frequency		-	-	10	MHz
t_{ch}	SCK high time		50	-	-	ns
t_{cl}	SCK low time		50	-	-	ns
t_{rise}	SCK rise time		-	5	-	ns
t_{fall}	SCK fall time		-	5	-	ns
t_{setup}	MOSI setup time	from MOSI change to SCK rising edge	30	-	-	ns
t_{hold}	MOSI hold time	from SCK rising edge to MOSI change	60	-	-	ns
t_{nsetup}	NSS setup time	from NSS falling edge to SCK rising edge	30	-	-	ns
t_{nhold}	NSS hold time	from SCK falling edge to NSS rising edge, normal mode	30	-	-	ns
t_{nhigh}	NSS high time between SPI accesses		20	-	-	ns
T_DATA	DATA hold and setup time		250	-	-	ns

3. Chip Description

Semtech's transceivers SX1231 and SX1231J share the architecture and functionnalities. For a complete description of the feature set, please refer to [1]

4. Configuration and Status Registers

4.1. General Description

Table 9   Registers Summary

Address	Register Name	Reset (built-in)	Default (recommended)	Description
0x00	RegFifo		0x00	FIFO read/write access
0x01	RegOpMode		0x04	Operating modes of the transceiver
0x02	RegDataModul		0x00	Data operation mode and Modulation settings
0x03	RegBitrateMsb		0x1A	Bit Rate setting, Most Significant Bits
0x04	RegBitrateLsb		0x0B	Bit Rate setting, Least Significant Bits
0x05	RegFdevMsb		0x00	Frequency Deviation setting, Most Significant Bits
0x06	RegFdevLsb		0x52	Frequency Deviation setting, Least Significant Bits
0x07	RegFrfMsb		0xE4	RF Carrier Frequency, Most Significant Bits
0x08	RegFrfMid		0xC0	RF Carrier Frequency, Intermediate Bits
0x09	RegFrfLsb		0x00	RF Carrier Frequency, Least Significant Bits
0x0A	RegOsc1		0x41	RC Oscillators Settings
0x0B	RegAfcCtrl		0x00	AFC control in low modulation index situations
0x0C	RegLowBat		0x02	Low Battery Indicator Settings
0x0D	RegListen1		0x92	Listen Mode settings
0x0E	RegListen2		0xF5	Listen Mode Idle duration
0x0F	RegListen3		0x20	Listen Mode Rx duration
0x10	RegVersion		0x23	Semtech ID relating the silicon revision
0x11	RegPaLevel		0x9F	PA selection and Output Power control
0x12	RegPaRamp		0x09	Control of the PA ramp time in FSK mode
0x13	RegOcp		0x1A	Over Current Protection control
0x14	Reserved14		0x40	-
0x15	Reserved15		0xB0	-

Address	Register Name	Reset (built-in)	Default (recom mended)	Description
0x16	Reserved16	0x7B		-
0x17	Reserved17	0x9B		-
0x18	RegLna	0x08	0x88	LNA settings
0x19	RegRxBw	0x86	0x55	Channel Filter BW Control
0x1A	RegAfcBw	0x8A	0x8B	Channel Filter BW control during the AFC routine
0x1B	RegOokPeak	0x40		OOK demodulator selection and control in peak mode
0x1C	RegOokAvg	0x80		Average threshold control of the OOK demodulator
0x1D	RegOokFix	0x06		Fixed threshold control of the OOK demodulator
0x1E	RegAfcFei	0x10		AFC and FEI control and status
0x1F	RegAfcMsb	0x00		MSB of the frequency correction of the AFC
0x20	RegAfcLsb	0x00		LSB of the frequency correction of the AFC
0x21	RegFeiMsb	0x00		MSB of the calculated frequency error
0x22	RegFeiLsb	0x00		LSB of the calculated frequency error
0x23	RegRssiConfig	0x02		RSSI-related settings
0x24	RegRssiValue	0xFF		RSSI value in dBm
0x25	RegDioMapping1	0x00		Mapping of pins DIO0 to DIO3
0x26	RegDioMapping2	0x05	0x07	Mapping of pins DIO4 and DIO5, ClkOut frequency
0x27	RegIrqFlags1	0x80		Status register: PLL Lock state, Timeout, RSSI > Threshold...
0x28	RegIrqFlags2	0x00		Status register: FIFO handling flags, Low Battery detection...
0x29	RegRssiThresh	0xFF	0xE4	RSSI Threshold control
0x2A	RegRxTimeout1	0x00		Timeout duration between Rx request and RSSI detection
0x2B	RegRxTimeout2	0x00		Timeout duration between RSSI detection and *PayloadReady*
0x2C	RegPreambleMsb	0x00		Preamble length, MSB
0x2D	RegPreambleLsb	0x03		Preamble length, LSB
0x2E	RegSyncConfig	0x98		Sync Word Recognition control
0x2F-0x36	RegSyncValue1-8	0x00	0x01	Sync Word bytes, 1 through 8
0x37	RegPacketConfig1	0x10		Packet mode settings
0x38	RegPayloadLength	0x40		Payload length setting
0x39	RegNodeAdrs	0x00		Node address

Address	Register Name	Reset (built-in)	Default (recommended)	Description
0x3A	RegBroadcastAdrs	0x00		Broadcast address
0x3B	RegAutoModes	0x00		Auto modes settings
0x3C	RegFifoThresh	0x0F	0x8F	Fifo threshold, Tx start condition
0x3D	RegPacketConfig2	0x02		Packet mode settings
0x3E-0x4D	RegAesKey1-16	0x00		16 bytes of the cypher key
0x4E	RegTemp1	0x01		Temperature Sensor control
0x4F	RegTemp2	0x00		Temperature readout
0x58	RegTestLna	0x1B		Sensitivity boost
0x59	RegTestTcxo	0x09		TCXO or XTAL input setting
0x6F	RegTestDagc	0x00	0x30	Fading Margin Improvement
0x71	RegTestAfc	0x00		AFC offset for low modulation index AFC
0x50 +	RegTest	-		Internal test registers

Note - *Reset values are automatically refreshed in the chip at Power On Reset*

- *Default values are the Semtech recommended register values, optimizing the device operation*

- *Registers for which the Default value differs from the Reset value are denoted by a * in the tables of section 4*

4.2. Common Configuration Registers

Table 10   Common Configuration Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegFifo (0x00)	7-0	Fifo	rw	0x00	FIFO data input/output
RegOpMode (0x01)	7	SequencerOff	rw	0	Controls the automatic Sequencer (see section 4.2): 0 → Operating mode as selected with Mode bits in RegOpMode is automatically reached with the Sequencer 1 → Mode is forced by the user
	6	ListenOn	rw	0	Enables Listen mode, should be enabled whilst in Standby mode: 0 → Off (see section 4.3) 1 → On
	5	ListenAbort	w	0	Aborts Listen mode when set together with ListenOn=0 See section 4.3.4 for details Always reads 0.
	4-2	Mode	rw	001	Transceiver's operating modes: 000 → Sleep mode (SLEEP) 001 → Standby mode (STDBY) 010 → Frequency Synthesizer mode (FS) 011 → Transmitter mode (TX) 100 → Receiver mode (RX) others → reserved Reads the value corresponding to the current chip mode
	1-0	-	r	00	unused
RegDataModul (0x02)	7	-	r	0	unused
	6-5	DataMode	rw	00	Data processing mode: 00 → Packet mode 01 → reserved 10 → Continuous mode with bit synchronizer 11 → Continuous mode without bit synchronizer
	4-3	ModulationType	rw	00	Modulation scheme: 00 → FSK 01 → OOK 10 - 11 → reserved
	2	-	r	0	unused
	1-0	ModulationShaping	rw	00	Data shaping: in FSK: 00 → no shaping 01 → Gaussian filter, BT = 1.0 10 → Gaussian filter, BT = 0.5 11 → Gaussian filter, BT = 0.3 in OOK: 00 → no shaping 01 → filtering with f_{cutoff} = BR 10 → filtering with f_{cutoff} = 2*BR 11 → reserved
RegBitrateMsb (0x03)	7-0	BitRate(15:8)	rw	0x1a	MSB of Bit Rate (Chip Rate when Manchester encoding is enabled)

RegBitrateLsb (0x04)	7-0	BitRate(7:0)	rw	0x0b	LSB of Bit Rate (Chip Rate if Manchester encoding is enabled) $$BitRate = \frac{FXOSC}{BitRate(15,0)}$$ Default value: 4.8 kb/s
RegFdevMsb (0x05)	7-6	-	r	00	unused
	5-0	Fdev(13:8)	rw	000000	MSB of the frequency deviation
RegFdevLsb (0x06)	7-0	Fdev(7:0)	rw	0x52	LSB of the frequency deviation $$Fdev = Fstep \times Fdev(15,0)$$ Default value: 5 kHz
RegFrfMsb (0x07)	7-0	Frf(23:16)	rw	0xe4	MSB of the RF carrier frequency
RegFrfMid (0x08)	7-0	Frf(15:8)	rw	0xc0	Middle byte of the RF carrier frequency
RegFrfLsb (0x09)	7-0	Frf(7:0)	rw	0x00	LSB of the RF carrier frequency $$Frf = Fstep \times Frf(23;0)$$ Default value: Frf = 915 MHz (32 MHz XO)
RegOsc1 (0x0A)	7	RcCalStart	w	0	Triggers the calibration of the RC oscillator when set. Always reads 0. RC calibration must be triggered in Standby mode.
	6	RcCalDone	r	1	0 → RC calibration in progress 1 → RC calibration is over
	5-0	-	r	000001	unused
RegAfcCtrl (0x0B)	7-6	-	r	00	unused
	5	AfcLowBetaOn	rw	0	Improved AFC routine for signals with modulation index lower than 2. Refer to section 3.5.16 for details 0 → Standard AFC routine 1 → Improved AFC routine
	4-0	-	r	00000	unused
RegLowBat (0x0C)	7-5	-	r	000	unused
	4	LowBatMonitor	rw	-	Real-time (not latched) output of the Low Battery detector, when enabled.
	3	LowBatOn	rw	0	Low Battery detector enable signal 0 → LowBat off 1 → LowBat on
	2-0	LowBatTrim	rw	010	Trimming of the LowBat threshold: 000 → 1.695 V 001 → 1.764 V 010 → 1.835 V 011 → 1.905 V 100 → 1.976 V 101 → 2.045 V 110 → 2.116 V 111 → 2.185 V

RegListen1 (0x0D)	7-6	ListenResolIdle	rw	10	Resolution of Listen mode Idle time (calibrated RC osc): 00 → reserved 01 → 64 us 10 → 4.1 ms 11 → 262 ms
	5-4	ListenResolRx	rw	01	Resolution of Listen mode Rx time (calibrated RC osc): 00 → reserved 01 → 64 us 10 → 4.1 ms 11 → 262 ms
	3	ListenCriteria	rw	0	Criteria for packet acceptance in Listen mode: 0 → signal strength is above *RssiThreshold* 1 → signal strength is above *RssiThreshold* and *SyncAddress* matched
	2-1	ListenEnd	rw	01	Action taken after acceptance of a packet in Listen mode: 00 → chip stays in Rx mode. Listen mode stops and must be disabled (see section 4.3). 01 → chip stays in Rx mode until *PayloadReady* or *Timeout* interrupt occurs. It then goes to the mode defined by *Mode*. Listen mode stops and must be disabled (see section 4.3). 10 → chip stays in Rx mode until *PayloadReady* or *Timeout* interrupt occurs. Listen mode then resumes in Idle state. FIFO content is lost at next Rx wakeup. 11 → Reserved
	0	-	r	0	unused
RegListen2 (0x0E)	7-0	ListenCoefIdle	rw	0xf5	Duration of the Idle phase in Listen mode. $$t_{ListenIdle} = ListenCoefIdle \cdot Listen\mathrm{Re}solIdle$$
RegListen3 (0x0F)	7-0	ListenCoefRx	rw	0x20	Duration of the Rx phase in Listen mode (startup time included, see section 4.2.3) $$t_{ListenRx} = ListenCoefRx \cdot Listen\mathrm{Re}solRx$$
RegVersion (0x10)	7-0	Version	r	0x23	Version code of the chip. Bits 7-4 give the full revision number; bits 3-0 give the metal mask revision number.

4.3. Transmitter Registers

Table 11   Transmitter Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegPaLevel (0x11)	7	Pa0On *	rw	1	Enables PA0, connected to RFIO and LNA
	6	Pa1On *	rw	0	Enables PA1, on PA_BOOST pin
	5	Pa2On *	rw	0	Enables PA2, on PA_BOOST pin
	4-0	OutputPower	rw	11111	Output power setting, with 1 dB steps Pout = -18 + *OutputPower* [dBm] , with PA0 or PA1 Pout = -14 + *OutputPower* [dBm] , with PA1 and PA2 (limited to the 16 upper values of *OutputPower*)
RegPaRamp (0x12)	7-4	-	r	0000	unused
	3-0	PaRamp	rw	1001	Rise/Fall time of ramp up/down in FSK 0000 → 3.4 ms 0001 → 2 ms 0010 → 1 ms 0011 → 500 us 0100 → 250 us 0101 → 125 us 0110 → 100 us 0111 → 62 us 1000 → 50 us 1001 → 40 us 1010 → 31 us 1011 → 25 us 1100 → 20 us 1101 → 15 us 1110 → 12 us 1111 → 10 us
RegOcp (0x13)	7-5	-	r	000	unused
	4	OcpOn	rw	1	Enables overload current protection (OCP) for the PA: 0 → OCP disabled 1 → OCP enabled
	3-0	OcpTrim	rw	1010	Trimming of OCP current: $Imax = 45 + 5 \times OcpTrim(mA)$ 95 mA OCP by default

*Note   *Power Amplifier truth table is available in Table 10.*

4.4. Receiver Registers

Table 12 Receiver Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
Reserved14 (0x14)	7-0	-	r	0x40	unused
Reserved15 (0x15)	7-0	-	r	0xB0	unused
Reserved16 (0x16)	7-0	-	r	0x7B	unused
Reserved17 (0x17)	7-0	-	r	0x9B	unused
RegLna (0x18)	7	LnaZin	rw	1 *	LNA's input impedance 0 → 50 ohms 1 → 200 ohms
	6	-	r	0	unused
	5-3	LnaCurrentGain	r	001	Current LNA gain, set either manually, or by the AGC
	2-0	LnaGainSelect	rw	000	LNA gain setting: 000 → gain set by the internal AGC loop 001 → G1 = highest gain 010 → G2 = highest gain – 6 dB 011 → G3 = highest gain – 12 dB 100 → G4 = highest gain – 24 dB 101 → G5 = highest gain – 36 dB 110 → G6 = highest gain – 48 dB 111 → reserved
RegRxBw (0x19)	7-5	DccFreq	rw	010 *	Cut-off frequency of the DC offset canceller (DCC): $$fc = \frac{4 \times RxBw}{2\pi \times 2^{DccFreq+2}}$$ ~4% of the RxBw by default
	4-3	RxBwMant	rw	10 *	Channel filter bandwidth control: 00 → RxBwMant = 16 10 → RxBwMant = 24 01 → RxBwMant = 20 11 → reserved
	2-0	RxBwExp	rw	101 *	Channel filter bandwidth control: FSK Mode: $$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+2}}$$ OOK Mode: $$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+3}}$$ See Table 13 for tabulated values
RegAfcBw (0x1A)	7-5	DccFreqAfc	rw	100	DccFreq parameter used during the AFC
	4-3	RxBwMantAfc	rw	01	RxBwMant parameter used during the AFC
	2-0	RxBwExpAfc	rw	011 *	RxBwExp parameter used during the AFC

RegOokPeak (0x1B)	7-6	OokThreshType	rw	01	Selects type of threshold in the OOK data slicer: 00 → fixed 10 → average 01 → peak 11 → reserved	
	5-3	OokPeakTheshStep	rw	000	Size of each decrement of the RSSI threshold in the OOK demodulator: 000 → 0.5 dB 001 → 1.0 dB 010 → 1.5 dB 011 → 2.0 dB 100 → 3.0 dB 101 → 4.0 dB 110 → 5.0 dB 111 → 6.0 dB	
	2-0	OokPeakThreshDec	rw	000	Period of decrement of the RSSI threshold in the OOK demodulator: 000 → once per chip 001 → once every 2 chips 010 → once every 4 chips 011 → once every 8 chips 100 → twice in each chip 101 → 4 times in each chip 110 → 8 times in each chip 111 → 16 times in each chip	
RegOokAvg (0x1C)	7-6	OokAverageThreshFilt	rw	10	Filter coefficients in average mode of the OOK demodulator: 00 → f_C ≈ chip rate / 32.π 01 → f_C ≈ chip rate / 8.π 10 → f_C ≈ chip rate / 4.π 11 → f_C ≈ chip rate / 2.π	
	5-0	-	r	000000	unused	
RegOokFix (0x1D)	7-0	OokFixedThresh	rw	0110 (6dB)	Fixed threshold value (in dB) in the OOK demodulator. Used when *OokThresType* = 00	
RegAfcFei (0x1E)	7	-	r	0	unused	
	6	FeiDone	r	0	0 → FEI is on-going 1 → FEI finished	
	5	FeiStart	w	0	Triggers a FEI measurement when set. Always reads 0.	
	4	AfcDone	r	1	0 → AFC is on-going 1 → AFC has finished	
	3	AfcAutoclearOn	rw	0	Only valid if *AfcAutoOn* is set 0 → AFC register is not cleared before a new AFC phase 1 → AFC register is cleared before a new AFC phase	
	2	AfcAutoOn	rw	0	0 → AFC is performed each time *AfcStart* is set 1 → AFC is performed each time Rx mode is entered	
	1	AfcClear	w	0	Clears the AfcValue if set in Rx mode. Always reads 0	
	0	AfcStart	w	0	Triggers an AFC when set. Always reads 0.	
RegAfcMsb (0x1F)	7-0	AfcValue(15:8)	r	0x00	MSB of the AfcValue, 2's complement format	
RegAfcLsb (0x20)	7-0	AfcValue(7:0)	r	0x00	LSB of the AfcValue, 2's complement format *Frequency correction* = AfcValue x Fstep	
RegFeiMsb (0x21)	7-0	FeiValue(15:8)	r	-	MSB of the measured frequency offset, 2's complement	
RegFeiLsb (0x22)	7-0	FeiValue(7:0)	r	-	LSB of the measured frequency offset, 2's complement *Frequency error* = FeiValue x Fstep	
RegRssiConfig (0x23)	7-2	-	r	000000	unused	
	1	RssiDone	r	1	0 → RSSI is on-going 1 → RSSI sampling is finished, result available	
	0	RssiStart	w	0	Trigger a RSSI measurement when set. Always reads 0.	
RegRssiValue (0x24)	7-0	RssiValue	r	0xFF	Absolute value of the RSSI in dBm, 0.5dB steps. RSSI = *-RssiValue/2 [dBm]*	

4.5. IRQ and Pin Mapping Registers

Table 13 IRQ and Pin Mapping Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegDioMapping1 (0x25)	7-6	Dio0Mapping	rw	00	Mapping of pins DIO0 to DIO5
	5-4	Dio1Mapping	rw	00	
	3-2	Dio2Mapping	rw	00	See Table 20 for mapping in Continuous mode
	1-0	Dio3Mapping	rw	00	See Table 21 for mapping in Packet mode
RegDioMapping2 (0x26)	7-6	Dio4Mapping	rw	00	
	5-4	Dio5Mapping	rw	00	
	3	-	r	0	unused
	2-0	ClkOut	rw	111 *	Selects CLKOUT frequency: 000 → FXOSC 001 → FXOSC / 2 010 → FXOSC / 4 011 → FXOSC / 8 100 → FXOSC / 16 101 → FXOSC / 32 110 → RC (automatically enabled) 111 → OFF
RegIrqFlags1 (0x27)	7	ModeReady	r	1	Set when the operation mode requested in *Mode*, is ready - Sleep: Entering Sleep mode - Standby: XO is running - FS: PLL is locked - Rx: RSSI sampling starts - Tx: PA ramp-up completed Cleared when changing operating mode.
	6	RxReady	r	0	Set in Rx mode, after RSSI, AGC and AFC. Cleared when leaving Rx.
	5	TxReady	r	0	Set in Tx mode, after PA ramp-up. Cleared when leaving Tx.
	4	PllLock	r	0	Set (in FS, Rx or Tx) when the PLL is locked. Cleared when it is not.
	3	Rssi	rwc	0	Set in Rx when the *RssiValue* exceeds *RssiThreshold.* Cleared when leaving Rx.
	2	Timeout	r	0	Set when a timeout occurs (see *TimeoutRxStart* and *TimeoutRssiThresh*) Cleared when leaving Rx or FIFO is emptied.
	1	AutoMode	r	0	Set when entering Intermediate mode. Cleared when exiting Intermediate mode. Please note that in Sleep mode a small delay can be observed between *AutoMode* interrupt and the corresponding enter/exit condition.
	0	SyncAddressMatch	r/rwc	0	Set when Sync and Address (if enabled) are detected. Cleared when leaving Rx or FIFO is emptied. This bit is read only in Packet mode, rwc in Continuous mode

RegIrqFlags2 (0x28)	7	FifoFull	r	0	Set when FIFO is full (i.e. contains 66 bytes), else cleared.
	6	FifoNotEmpty	r	0	Set when FIFO contains at least one byte, else cleared
	5	FifoLevel	r	0	Set when the number of bytes in the FIFO strictly exceeds *FifoThreshold*, else cleared.
	4	FifoOverrun	rwc	0	Set when FIFO overrun occurs. (except in Sleep mode) Flag(s) and FIFO are cleared when this bit is set. The FIFO then becomes immediately available for the next transmission / reception.
	3	PacketSent	r	0	Set in Tx when the complete packet has been sent. Cleared when exiting Tx.
	2	PayloadReady	r	0	Set in Rx when the payload is ready (i.e. last byte received and CRC, if enabled and *CrcAutoClearOff* is cleared, is Ok). Cleared when FIFO is empty.
	1	CrcOk	r	0	Set in Rx when the CRC of the payload is Ok. Cleared when FIFO is empty.
	0	LowBat	rwc	-	Set when the battery voltage drops below the Low Battery threshold. Cleared only when set by the user.
RegRssiThresh (0x29)	7-0	RssiThreshold	rw	0xE4 *	RSSI trigger level for *Rssi* interrupt : - *RssiThreshold* / 2 [dBm]
RegRxTimeout1 (0x2A)	7-0	TimeoutRxStart	rw	0x00	*Timeout* interrupt is generated *TimeoutRxStart*$*16*T_{bit}$ after switching to Rx mode if *Rssi* interrupt doesn't occur (i.e. *RssiValue > RssiThreshold)* 0x00: *TimeoutRxStart* is disabled
RegRxTimeout2 (0x2B)	7-0	TimeoutRssiThresh	rw	0x00	*Timeout* interrupt is generated *TimeoutRssiThresh*$*16*T_{bit}$ after *Rssi* interrupt if *PayloadReady* interrupt doesn't occur. 0x00: *TimeoutRssiThresh* is disabled

4.6. Packet Engine Registers

Table 14 Packet Engine Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegPreambleMsb (0x2c)	7-0	PreambleSize(15:8)	rw	0x00	Size of the preamble to be sent (from *TxStartCondition* fulfilled). (MSB byte)
RegPreambleLsb (0x2d)	7-0	PreambleSize(7:0)	rw	0x03	Size of the preamble to be sent (from *TxStartCondition* fulfilled). (LSB byte)
RegSyncConfig (0x2e)	7	SyncOn	rw	1	Enables the Sync word generation and detection: 0 → Off 1 → On
	6	FifoFillCondition	rw	0	FIFO filling condition: 0 → if *SyncAddress* interrupt occurs 1 → as long as *FifoFillCondition* is set
	5-3	SyncSize	rw	011	Size of the Sync word: (*SyncSize* + 1) bytes
	2-0	SyncTol	rw	000	Number of tolerated bit errors in Sync word
RegSyncValue1 (0x2f)	7-0	SyncValue(63:56)	rw	0x01 *	1st byte of Sync word. (MSB byte) Used if *SyncOn* is set.
RegSyncValue2 (0x30)	7-0	SyncValue(55:48)	rw	0x01 *	2nd byte of Sync word Used if *SyncOn* is set and *(SyncSize +1)* >= 2.
RegSyncValue3 (0x31)	7-0	SyncValue(47:40)	rw	0x01 *	3rd byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 3.
RegSyncValue4 (0x32)	7-0	SyncValue(39:32)	rw	0x01 *	4th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 4.
RegSyncValue5 (0x33)	7-0	SyncValue(31:24)	rw	0x01 *	5th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 5.
RegSyncValue6 (0x34)	7-0	SyncValue(23:16)	rw	0x01 *	6th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 6.
RegSyncValue7 (0x35)	7-0	SyncValue(15:8)	rw	0x01 *	7th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* >= 7.
RegSyncValue8 (0x36)	7-0	SyncValue(7:0)	rw	0x01 *	8th byte of Sync word. Used if *SyncOn* is set and *(SyncSize +1)* = 8.

RegPacketConfig1 (0x37)	7	PacketFormat	rw	0	Defines the packet format used: 0 → Fixed length 1 → Variable length
	6-5	DcFree	rw	00	Defines DC-free encoding/decoding performed: 00 → None (Off) 01 → Manchester 10 → Whitening 11 → reserved
	4	CrcOn	rw	1	Enables CRC calculation/check (Tx/Rx): 0 → Off 1 → On
	3	CrcAutoClearOff	rw	0	Defines the behavior of the packet handler when CRC check fails: 0 → Clear FIFO and restart new packet reception. No *PayloadReady* interrupt issued. 1 → Do not clear FIFO. *PayloadReady* interrupt issued.
	2-1	AddressFiltering	rw	00	Defines address based filtering in Rx: 00 → None (Off) 01 → Address field must match *NodeAddress* 10 → Address field must match *NodeAddress* or *BroadcastAddress* 11 → reserved
	0	-	rw	0	unused
RegPayloadLength (0x38)	7-0	PayloadLength	rw	0x40	If PacketFormat = 0 (fixed), payload length. If PacketFormat = 1 (variable), max length in Rx, not used in Tx.
RegNodeAdrs (0x39)	7-0	NodeAddress	rw	0x00	Node address used in address filtering.
RegBroadcastAdrs (0x3A)	7-0	BroadcastAddress	rw	0x00	Broadcast address used in address filtering.
RegAutoModes (0x3B)	7-5	EnterCondition	rw	000	Interrupt condition for entering the intermediate mode: 000 → None (AutoModes Off) 001 → Rising edge of *FifoNotEmpty* 010 → Rising edge of *FifoLevel* 011 → Rising edge of *CrcOk* 100 → Rising edge of *PayloadReady* 101 → Rising edge of *SyncAddress* 110 → Rising edge of *PacketSent* 111 → Falling edge of *FifoNotEmpty* (i.e. FIFO empty)
	4-2	ExitCondition	rw	000	Interrupt condition for exiting the intermediate mode: 000 → None (AutoModes Off) 001 → Falling edge of *FifoNotEmpty* (i.e. FIFO empty) 010 → Rising edge of *FifoLevel* or *Timeout* 011 → Rising edge of *CrcOk* or *Timeout* 100 → Rising edge of *PayloadReady* or *Timeout* 101 → Rising edge of *SyncAddress* or *Timeout* 110 → Rising edge of *PacketSent* 111 → Rising edge of *Timeout*
	1-0	IntermediateMode	rw	00	Intermediate mode: 00 → Sleep mode (SLEEP) 01 → Standby mode (STDBY) 10 → Receiver mode (RX) 11 → Transmitter mode (TX)

RegFifoThresh (0x3C)	7	TxStartCondition	rw	1 *	Defines the condition to start packet transmission : 0 → *FifoLevel* (i.e. the number of bytes in the FIFO exceeds *FifoThreshold)* 1 → *FifoNotEmpty* (i.e. at least one byte in the FIFO)
	6-0	FifoThreshold	rw	0001111	Used to trigger *FifoLevel* interrupt.
RegPacketConfig2 (0x3D)	7-4	InterPacketRxDelay	rw	0000	After *PayloadReady* occurred, defines the delay between FIFO empty and the start of a new RSSI phase for next packet. Must match the transmitter's PA ramp-down time. - Tdelay = 0 if *InterpacketRxDelay* >= 12 - Tdelay = $(2^{InterpacketRxDelay})$ / *BitRate* otherwise
	3	-	rw	0	unused
	2	RestartRx	w	0	Forces the Receiver in WAIT mode, in Continuous Rx mode. Always reads 0.
	1	AutoRxRestartOn	rw	1	Enables automatic Rx restart (RSSI phase) after *PayloadReady* occurred and packet has been completely read from FIFO: 0 → Off. *RestartRx* can be used. 1 → On. Rx automatically restarted after *InterPacketRxDelay*.
	0	AesOn	rw	0	Enable the AES encryption/decryption: 0 → Off 1 → On (payload limited to 66 bytes maximum)
RegAesKey1 (0x3E)	7-0	AesKey(127:120)	w	0x00	1st byte of cipher key (MSB byte)
RegAesKey2 (0x3F)	7-0	AesKey(119:112)	w	0x00	2nd byte of cipher key
RegAesKey3 (0x40)	7-0	AesKey(111:104)	w	0x00	3rd byte of cipher key
RegAesKey4 (0x41)	7-0	AesKey(103:96)	w	0x00	4th byte of cipher key
RegAesKey5 (0x42)	7-0	AesKey(95:88)	w	0x00	5th byte of cipher key
RegAesKey6 (0x43)	7-0	AesKey(87:80)	w	0x00	6th byte of cipher key
RegAesKey7 (0x44)	7-0	AesKey(79:72)	w	0x00	7th byte of cipher key
RegAesKey8 (0x45)	7-0	AesKey(71:64)	w	0x00	8th byte of cipher key
RegAesKey9 (0x46)	7-0	AesKey(63:56)	w	0x00	9th byte of cipher key
RegAesKey10 (0x47)	7-0	AesKey(55:48)	w	0x00	10th byte of cipher key
RegAesKey11 (0x48)	7-0	AesKey(47:40)	w	0x00	11th byte of cipher key
RegAesKey12 (0x49)	7-0	AesKey(39:32)	w	0x00	12th byte of cipher key
RegAesKey13 (0x4A)	7-0	AesKey(31:24)	w	0x00	13th byte of cipher key

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegAesKey14 (0x4B)	7-0	AesKey(23:16)	w	0x00	14th byte of cipher key
RegAesKey15 (0x4C)	7-0	AesKey(15:8)	w	0x00	15th byte of cipher key
RegAesKey16 (0x4D)	7-0	AesKey(7:0)	w	0x00	16th byte of cipher key (LSB byte)

4.7. Temperature Sensor Registers

Table 15   Temperature Sensor Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegTemp1 (0x4E)	7-4	-	r	0000	unused
	3	TempMeasStart	w	0	Triggers the temperature measurement when set. Always reads 0.
	2	TempMeasRunning	r	0	Set to 1 while the temperature measurement is running. Toggles back to 0 when the measurement has completed. The receiver can not be used while measuring temperature
	1-0	-	r	01	unused
RegTemp2 (0x4F)	7-0	TempValue	r	-	Measured temperature -1°C per Lsb Needs calibration for accuracy

4.8. Test Registers

Table 16   Test Registers

Name (Address)	Bits	Variable Name	Mode	Default Value	Description
RegTestLna (0x58)	7-0	SensitivityBoost	rw	0x1B	High sensitivity or normal sensitivity mode: 0x1B → Normal mode 0x2D → High sensitivity mode
RegTestTcxo (0x59)	7-0	TcxoOn	rw	0x09	Selects XTAL or TCXO input: 0x09 → Normal XTAL mode 0x19 → Clipped sine TCXO input
RegTestDagc (0x6F)	7-0	ContinuousDagc	rw	0x30 *	Fading Margin Improvement, refer to 3.5.4 0x00 → Normal mode 0x20 → Improved margin, use if *AfcLowBetaOn=1* 0x30 → Improved margin, use if *AfcLowBetaOn=0*
RegTestAfc (0x71)	7-0	LowBetaAfcOffset	rw	0x00	AFC offset set for low modulation index systems, used if *AfcLowBetaOn=1*. *Offset = LowBetaAfcOffset x 488 Hz*

5. Application Information

Application information shown here is SX1231J-specific. More application information relevant to the SX1231J can be found in [1].

5.1. Reference Design

Please contact your Semtech representative for evaluation tools, reference designs and design assistance. Note that all schematics shown in this section are full schematics, listing ALL required components, including decoupling capacitors.
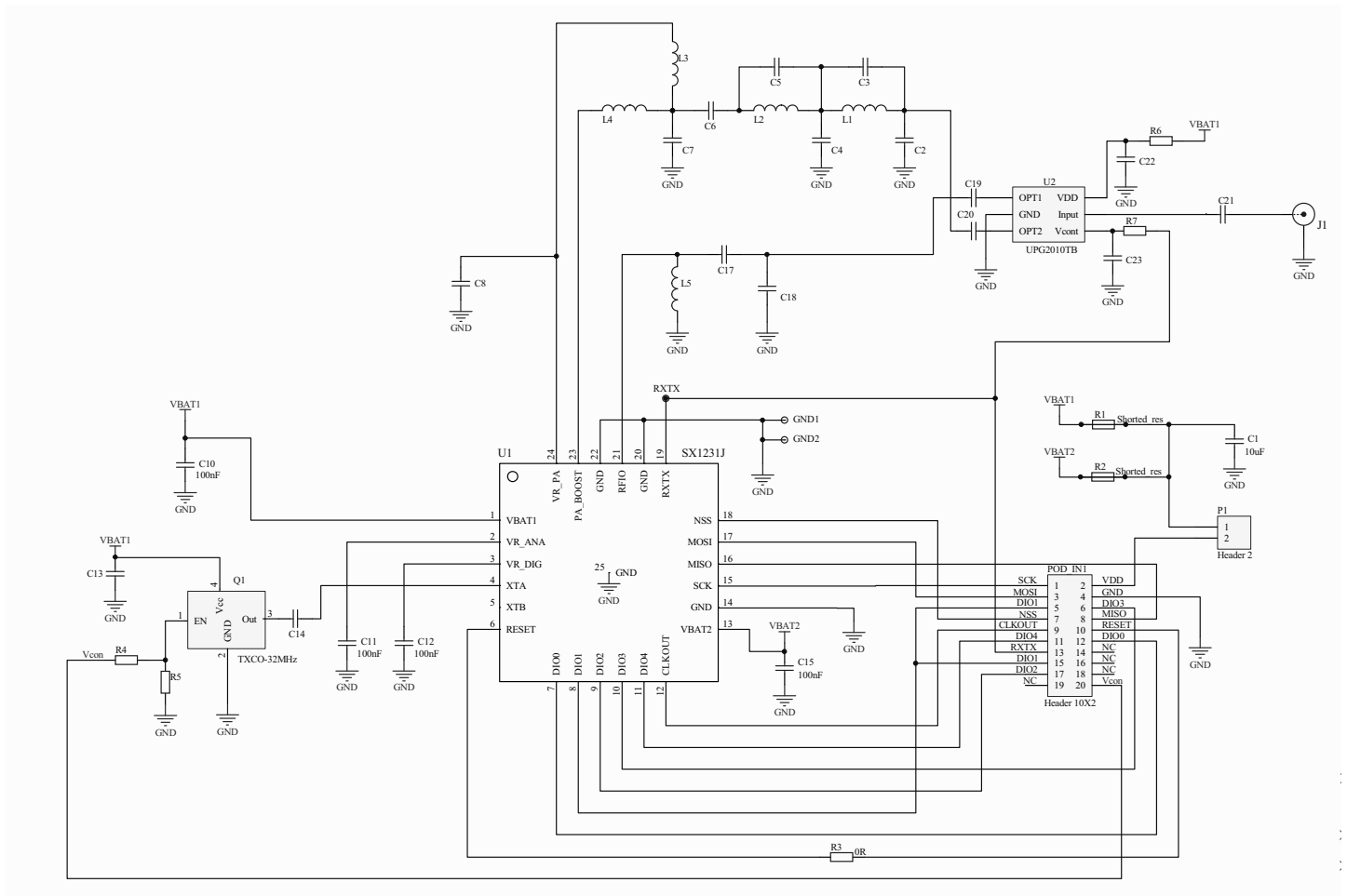
Figure 4.   SX1231J Evaluation Module Schematics

Table 17   SX1231J Evaluation Module BOM

RefDes	Geom	Value			Qty	Description
		426MHz	469MHz	920MHz		
IC						
U1	QFN24	SX1231J			1	SX1231J Low-Power UHF Integrated Transceiver
U2	6 pin mini-mold	upg2010TB			1	SPDT RF Switch
Resistors						
R3	402	0R			1	Thick Film Resistor ±5%, 1/16W
R6	402	15K			1	Thick Film Resistor ±5%, 1/16W
R7	402	68K			1	Thick Film Resistor ±5%, 1/16W
Capacitors						
C1	603	10µF			1	Multilayer ceramic capacitors X5R ±20%, 6.3V
C2	402	8.2pF	8.2pF	5.6pF	1	Multilayer ceramic capacitors C0G ±0.5pF, 50V
C4	402	15pF	15pF	6.8pF	1	Multilayer ceramic capacitors C0G ±5%, 50V
C5	402	2.7pF	2.7pF	1.2pF	1	Multilayer ceramic capacitors C0G ±0.25pF, 50V
C6	402	33pF	22pF	10pF	1	Multilayer ceramic capacitors C0G ±5%, 50V
C7	402	18pF	12pF	3.9pF	1	Multilayer ceramic capacitors C0G ±5%, 50V
C8,C13,C14	402	10nF			3	Multilayer ceramic capacitors X7R ±10%, 25V
C10,C11,C12,C15	402	100nF			4	Multilayer ceramic capacitors X7R ±10%, 16V
C17	402	10nH	10nH	5.6nH	1	Wirewound Inductor ±0.2nH
C18	402	4.7pF	4.7pF	5.6pF	1	Multilayer ceramic capacitors C0G ±0.5pF, 50V
C19,C20,C21	402	100pF			3	Multilayer ceramic capacitors C0G ±0.25pF, 50V
C22,C23	402	1nF			2	Multilayer ceramic capacitors C0G ±0.5pF, 50V
Inductors						
L1	402	10nH	10nH	6.8nH	1	Wirewound Inductor ±0.2nH
L2	402	12nH	12nH	6.8nH	1	Wirewound Inductor ±0.2nH
L3	402	33nH			1	Wirewound Inductor ±5%
L4	402	12nH	10nH	4.7nH	1	Wirewound Inductor ±0.2nH
L5	402	33nH	33nH	3.9nH	1	Wirewound Inductor ±5%
Crystal						
Q1	3225	32.000MH	32.000MH	30.000M	1	TCXO, surface mount type, ±2.5ppm,
Do not Populate						
R1,R2	Shorted 0402				0	
R4,R5,C3,C18	402	DNP			0	
L5	402				0	

Notes   - Inductor values may change when using multilayer type components, but nearly equal performance should be attained

- In very cost-sensitive and/or size-constrained applications where it is acceptable to degrade the receiver sensitivity, L5 and C17 and C18 can be omitted

5.2. Regulatory Compliance

The SX1231J performance is such that it complies with narrowband and wideband Japanese regulations. This is mostly achieved thanks to the excellent spectral purity and best in-class Local Oscillator phase noise.

5.2.1. ARIB STD-T67

The ARIB STD-T67 standard mandates narrow 12.5kHz channels at about 426, 449 and 469MHz. With the proposed reference design, Semtech recommends the following RF settings:

- GFSK modulation, with BT=0.5

- Bit Rate = 2.4 kbps, Fdev = +/-3 kHz

- RxBw = 5.2 kHz, corresponding to a double side bandwidth of 10.4 kHz

- Pout = +10 mW, as limited by STD-T67

Under these conditions, the SX1231J fulfills all the requirements of the STD-T67 with significant margin, namely:

- 99% energy bandwidth is lower than 8.5 kHz

- Spurious emissions meet the -26 dBm limit with more than 20 dB of margin

- Adjacent Channel leakage power with more than 15 dB margin

- The observed sensitivity is typ. -118 dBm with BER=0.1%, and -120 dBm with BER=1%

- Spurious response rejection does not apply with SX1231J's Direct Conversion architecture

- At 12.5 kHz and 25 kHz offsets, the typical selectivity is respectively 36dB and 57dB (requirement: 30dB), and can be improved to typ. 55dB, respectively 59dB with the use of a tighter internal Channel Filter (RxBw=3.9 kHz). Using a narrower filter increases the constraint on the Local Oscillator stability accordingly (TCXO performance).

Other sets of bit rates and deviation frequencies may of course be possible.

5.2.2. ARIB STD-T108

The ARIB STD-T108 standard focuses on wider channels of 200 kHz or more in the 915-930 MHz band. Under these conditions, there is more flexibility as to the choice of the RF settings.

The SX1231J will fulfill the requirements of the STD-T108 in Middle Power (up to 250mW), Low Power (up to 20mW) and Ultra Low Power (up to 1mW) modes. An external Power Amplifier will be required to increase the output power over +17dBm. With its spectral purity, the SX1231J can meet the 99% energy bandwidth, spectral mask, Adjacent Channel Leakage Power and Spurious emissions limits of the standard with significant margin.
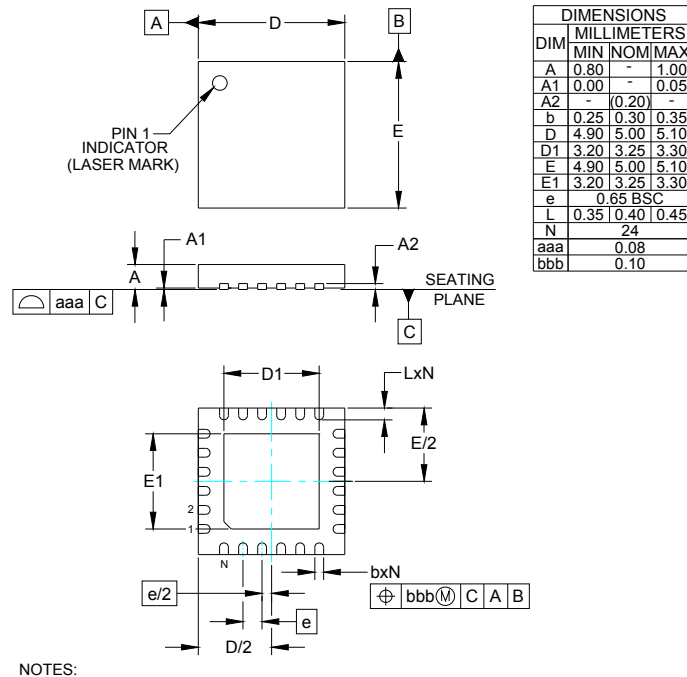
In particular, the SX1231J complies with the radio Type 1 (+13dBm) constraints for Smart Metering and Sensor Networks applications, under the Common Signaling Mode as defined in the IEEE 802.15.4g.

Please contact your local Semtech representative for a detailed report on the STD-T67 or STD-T108 compliance of the SX1231J.

6. Packaging Information

6.1. QFN 24 Encapsulation

The SX1231J is available in a 24-lead QFN package as show in Figure 5.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	-	1.00
A1	0.00	-	0.05
A2	-	(0.20)	-
b	0.25	0.30	0.35
D	4.90	5.00	5.10
D1	3.20	3.25	3.30
E	4.90	5.00	5.10
E1	3.20	3.25	3.30
e	0.65 BSC		
L	0.35	0.40	0.45
N	24		
aaa	0.08		
bbb	0.10		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

Figure 5.   QFN 24 Package Outline Drawing and Land Pattern

6.2. Thermal Impedance

The thermal impedance of this package, calculated from a package in still air, on a 4-layer FR4 PCB, as per the Jedec standard, is Theta ja = 23.8° C/W typ.

6.3. Tape & Reel Specification

Carrier Tape				Reel					
Tape Width (W)	Pocket Pitch (P)	Ao / Bo	Ko	Reel Size	Reel Width	Min. Trailer Length	Min. Leader Length	QTY per	Unit
12 +/-0.30	8 +/-0.10	5.25 +/-0.20	1.10 +/-0.10	330.2	12.4	400	400	3000	mm
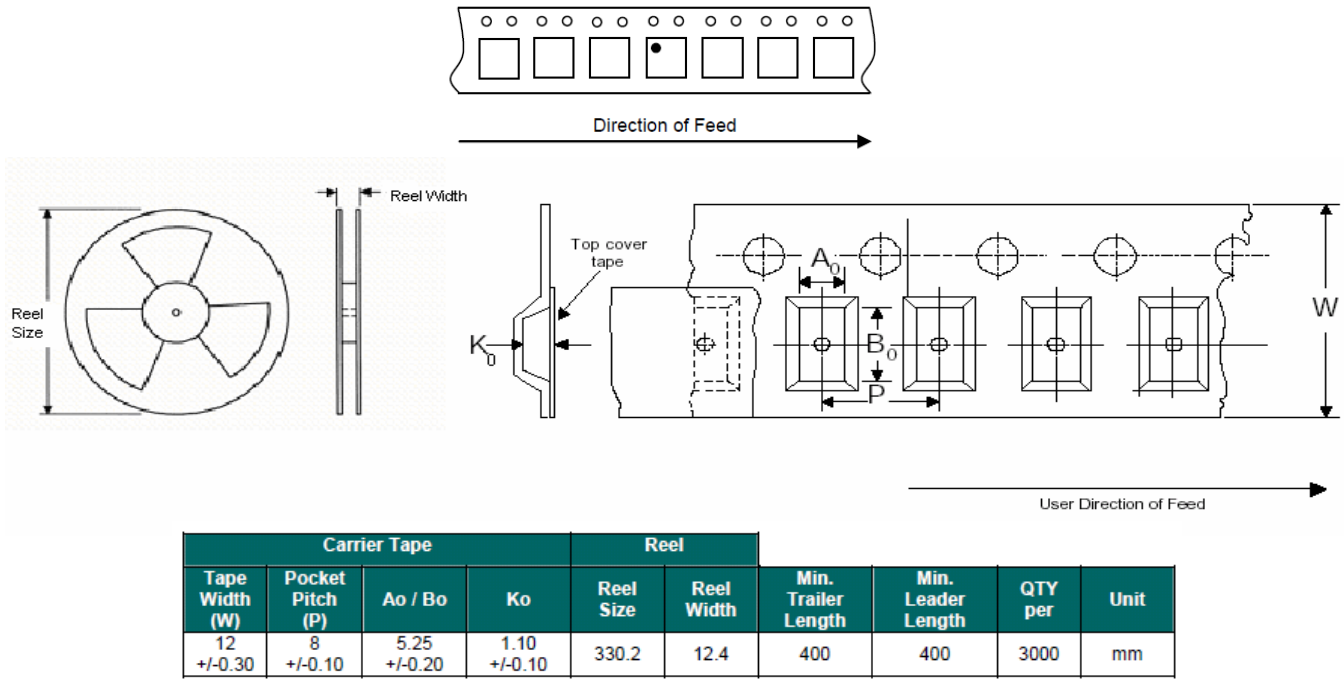
Figure 6.   Tape & Reel Specification, QFN Package

Note   Single Sprocket holes

7. References

[1]   SX1231 Datasheet. Please consult the Semtech website **www.semtech.com** on a regular basis for news and updates.

8. Revision History

Table 18   Revision History

Revision	Date	Comment
1	Jan 2012	First FINAL datasheet version
2	April 2012	Minor edits Mention STD-T108

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