PIC16(L)F1526/1527 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1526/1527 family devices that you have received conform functionally to the current Device Data Sheet (DS41458**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1526/1527 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 6, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1526/1527 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1), (2)			
	DEV<8:0>	REV<4:0> Silicon Revision		
		A2	A3	A5
PIC16F1526	01 0101 100	—	0 0011	0 0101
PIC16LF1526	01 0101 110	0 0010	0 0011	0 0101
PIC16F1527	01 0101 101	—	0 0011	0 0101
PIC16LF1527	01 0101 111	0 0010	0 0011	0 0101

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F151X/152X Memory Programming Specification"* (DS41442) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A5
High-Frequency Internal Oscillator (HFINTOSC)	HFINTOSC Operation	1.1	HFINTOSC is not stable when VDD < 2.3V.	X		
High-Frequency Internal Oscillator (HFINTOSC)	HFINTOSC Operation	1.2	HFINTOSC Max. VDD at -40°C.		X	
FVR	FVR Ready Bit (FVRRDY)	2.1	FVRRDY bit may not get set at low VDD and low-operating temperature.	X		
FVR	Gain Amplifier	2.2	Higher than expected current consumption.	X	X	X
EUSART	Break generation – SREN bit	3.1	Break generation in Asynchronous mode is inaccurate.	X		
EUSART	Auto-baud – WUE and ABDEN bits	3.2	Setting WUE and ABDEN simultaneously does not perform auto-baud correctly.	X		
Oscillator	HFINTOSC Ready/Stable bit	4.1	Bits remained set to ‘1’ after initial trigger.	X	X	
Oscillator	Clock Switching	4.2	Clock switching can cause a single corrupted instruction.	X	X	X
Oscillator	Oscillator Start-up Timer (OST) bit	4.3	OST bit remains set.	X	X	X
MSSP (Master Synchronous Serial Port)	SPI Master mode	5.1	Buffer Full (BF) bit or MSSP Interrupt Flag (SSPIF) bit becomes set half SCK cycle too early.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: High-Frequency Internal Oscillator (HFINTOSC)

1.1 Internal Oscillator Min. VDD

The High-Frequency Internal Oscillator requires a minimum voltage of 2.3V to operate.

Work around

None.

Affected Silicon Revisions

A2	A3	A5					
X							

1.2 HFINTOSC Max. VDD at -40°C

For the LF devices only, the High-Frequency Internal Oscillator may stop working at -40°C when VDD is 3.6V.

Work around

None.

Affected Silicon Revisions

A2	A3	A5					
	X						

2. Module: FVR

2.1 FVR Stable Bit

After the FVR is stabilized, the FVR Ready bit may not be set when the temperature is -40°C and VDD = 1.8V.

Work around

Operate above -30°C or with VDD >2.0V.

Affected Silicon Revisions

A2	A3	A5					
X							

2.2. Gain Amplifier

Higher than expected, current consumption can be experienced if one or both (if available) gain amplifiers are enabled when the FVR is not is use.

Work around

In order to minimize current consumption when the FVR is disabled, the gain amplifier(s) should be turned off by clearing the Buffer Gain Selection bits.

Affected Silicon Revisions

A2	A3	A5					
X	X	X					

3. Module: EUSART

3.1 Break Generation – SREN bit

In Asynchronous mode, when the SENDB bit is set during an active character transmission, then the TX pin will improperly be forced low and the transmit time will be extended to a total of 13-bit times. During the extension, both the TRMT and TXIF flags will be set, thus giving a false indication that the transmitter is inactive.

Work around

Ensure that the transmitter is not active by sensing if the TRMT flag is set before setting the SENDB bit.

Affected Silicon Revisions

A2	A3	A5					
X							

3.2 Auto-baud – WUE and ABDEN bits

Setting WUE and ABDEN simultaneously does not perform auto-baud correctly. The resulting number in SPBRG, after the Break and Sync character, is indeterminate.

Work around

Set only the WUE bit to enable wake from Sleep. Upon waking, immediately set the ABDEN bit to activate auto-baud.

Affected Silicon Revisions

A2	A3	A5					
X							

4. Module: Oscillator

4.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and the HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set, they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A2	A3	A5					
X	X						

4.2 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue does not affect the Two-Speed start-up or the Fail-Safe Clock Monitor operation.

Work around

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When switching from an internal oscillator (INTOSC) to an external oscillator clock source, first switch to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

A2	A3	A5					
X	X	X					

4.3 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, and the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators, which takes longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A2	A3	A5					
X	X	X					

5. Module: MSSP (Master Synchronous Serial Port)

5.1 SPI Master mode

When the MSSP is used in SPI Master mode and the CKE bit is clear (CKE = 0), the Buffer Full (BF) bit and the MSSP Interrupt Flag (SSPIF) bit becomes set half an SCK cycle early. If the user software immediately reacts to either of the bits being set, a write collision may occur as indicated by the WCOL bit being set.

Work around

To avoid a write collision one of the following methods should be used:

Method 1: Add a software delay of one SCK period after detecting the completed transfer (the BF bit or SSPIF bit becomes set) and prior to writing to the SSPBUF register. Verify the WCOL bit is clear after writing to SSPBUF. If the WCOL bit is set, clear the bit in software and rewrite the SSPBUF register.

Method 2: As part of the MSSP initialization procedure, set the CKE bit (CKE = 1).

Affected Silicon Revisions

A2	A3	A5					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41458**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (02/2011)

Initial release of this document.

Rev B Document (03/2011)

Added Silicon Revision A3; Added PIC16F1526 and PIC16F1527 devices; Added Module 1.2.

Rev C Document (02/2012)

Added Module 4, Oscillator; Other minor corrections.

Data Sheet Clarifications: Added Module 1, Oscillator.

Rev D Document (09/2013)

Added Silicon Revision A5; Other minor corrections.

Rev E Document (11/2014)

Added Module 5, MSSP; Other minor corrections.

Data Sheet Clarifications: Removed Module 1, Oscillator.

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