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CONTINUITY OF SPECIFICATIONS

There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

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BCM4325

IEEE 802.11 a/b/g MAC/Baseband/Radio Plus Bluetooth 3.0 + HS and FM Receiver Single-Chip Combination

GENERAL DESCRIPTION

The Broadcom® BCM4325 single-chip device provides the highest level of integration for a mobile or handheld wireless systems with integrated IEEE 802.11™ a/b/g MAC/baseband/radio, Bluetooth® 3.0 + HS and a FM radio receiver.

Designed to address the needs of highly mobile devices that require minimal power consumption and board area, the BCM4325 provides a compact ultra-small form-factor solution with minimal external components. This solution drives down the costs of mass volumes, while allowing for flexibility in the size, form, and function of handheld devices.

Utilizing advanced design techniques and process technologies to deliver low active and idle power, the BCM4325 extends system battery life while maintaining consistent connectivity and high throughput.

An SDIO system interface (4b, 1b, or SPI) is provided for WLAN and an independent, high-speed UART is provided for the Bluetooth section.

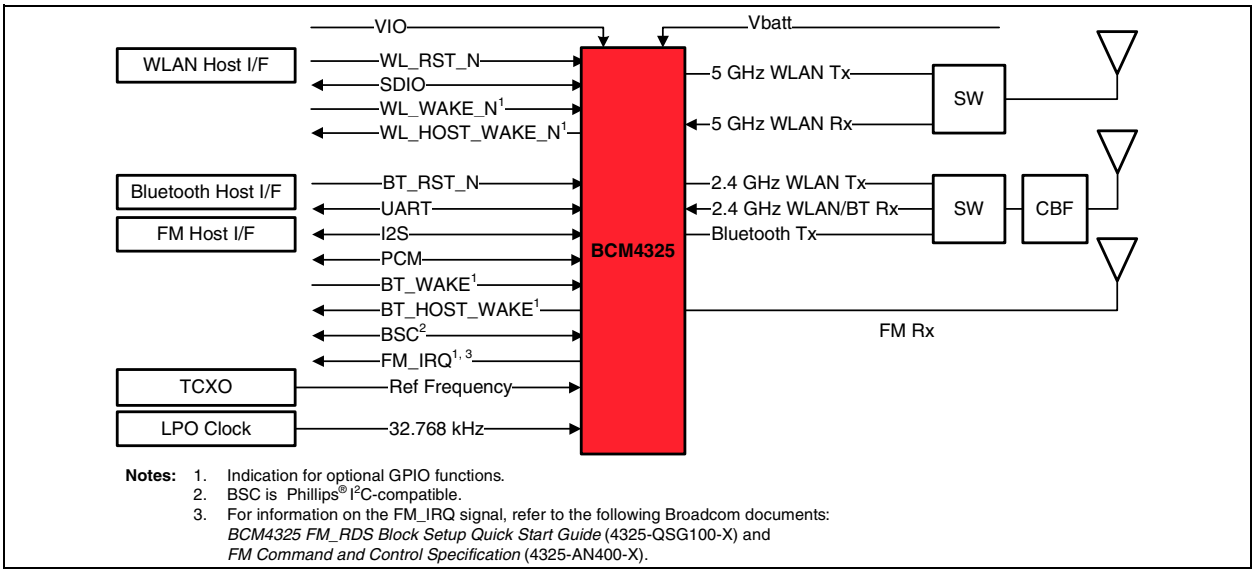
A unique feature of the BCM4325 is its implementation of highly sophisticated InConcert™ (IEEE 802.15.2) radio coexistence algorithms and hardware mechanisms.

InConcert provides the highest possible degree of collaboration between Bluetooth® and WLAN using a shared 2.4 GHz antenna, along with coexistence support for external radio technologies such as GPS, WiMax and Ultra Wide-Band (UWB).

As a result, the overall quality of simultaneous voice, video, and data transmission on a handheld system is enhanced while minimizing the PCB footprint.

Designed to support flexible power supply topologies, including operation directly from the rechargeable battery in a mobile platform, the BCM4325 integrates a power management unit with five LDOs and two switching regulators.

The integrated CMOS WLAN 2.4 GHz and 5 GHz power amplifiers provide sufficient output power to meet the needs of most WLAN devices, without the need for an external PA. Furthermore, the integrated buck-boost regulator allows the internal power amplifiers to operate at optimal performance, even at low Vbatt supply voltages. Transmit and receive baluns are also integrated.



Notes: 1. Indication for optional GPIO functions.
2. BSC is Phillips® I²C-compatible.
3. For information on the FM_IRQ signal, refer to the following Broadcom documents: *BCM4325 FM_RDS Block Setup Quick Start Guide* (4325-QSG100-X) and *FM Command and Control Specification* (4325-AN400-X).

Figure 1: Functional Block Diagram

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FEATURES

General Features

- Supports a battery voltage ranging from 2.3V to 5.5V with the internal buck-boost switching regulator
- Low power consumption and dynamic power management maximize battery life of handheld devices
- Five LDO regulators and two switching regulators with an on-chip, programmable power management unit
- Integrated CMOS power amplifiers deliver greater than 20 dBm of linear output power
- Supports a single 2.4 GHz antenna shared between WLAN and Bluetooth
- Internal fractional nPLL allows support for a wide range of reference clock frequencies.
- 2k-bit OTP for storing board parameters
- 196-ball flip-chip FBGA package (7.5 mm x 7.5 mm x 1.05 mm, 0.5 mm pitch) and 339-pin WLCSP package (6.51 mm x 5.81 mm x 0.42 mm, 0.25 mm pitch). Dimensions are nominal, see Figure 35 on page 115 and Figure 36 on page 116 for maximum dimensions)
- Provides an ultra-small form-factor solution and ultra low-power consumption to support low-cost requirements

IEEE 802.11x Features

- Single-band 2.4 GHz 802.11 b/g or dual-band 2.4 GHz and 5 GHz 802.11 a/b/g pin-compatible options
- Integrated WLAN CMOS power amplifiers deliver greater than 20 dBm of linear output power.
- Provides external coexistence handshake interface to support additional wireless technologies such as GPS, WiMax, or UWB
- Supports SDIO v1.2 (4-bit and 1-bit) and SPI, with SDIO clock speeds up to 50 MHz
- Integrated ARM7® RISC processor and on-chip memory for complete WLAN subsystem functionality minimizing the need to wake up the applications processor for standard WLAN functions. This allows for further minimization of power consumption, while maintaining the capability to field upgrade with future features.
- Security
  - WPA™ and WPA2™ (Personal) support for powerful encryption and authentication
  - AES and TKIP acceleration hardware for faster data encryption and 802.11i compatibility
  - Cisco® Compatible Extension—(CCX, CCX 2.0, CCX 3.0, CCX 4.0) certified
  - SecureEasySetup™ for simple Wi-Fi® setup and WPA2/WPA security configuration
  - Wi-Fi Protected Setup (WPS)
- Supports IEEE 802.11d, e (WMM, QoS, WMM-PS), h, i, j (k, r, and w in the future)
- Worldwide regulatory support – Global products supported with worldwide homologated design

Bluetooth Features

- Bluetooth Core specification 3.0 + HS compliant when combined with Bluetooth 3.0 + HS qualified host software, including Alternate MAC/PHY, read encryption key size, enhanced power control, and unicast connectionless data.
- Supports extended Synchronous Connections (eSCO), for enhanced voice quality by allowing for retransmission of dropped packets
- Adaptive Frequency Hopping (AFH) for reducing radio frequency interference
- Bluetooth Class 1 support with PA bias adjust
- Interface support—Host Controller Interface (HCI) using a high-speed UART interface and PCM for audio data
- Integrates the InConcert collaborative WLAN coexistence, including the 802.15.2 3-wire coexistence support
- Supports dual Advanced Audio Distribution Profile (A2DP) for stereo sound
- Automatic frequency detection for standard crystal and TCXO values
- Embedded ARM7 RISC processor and on-chip memory

FM Radio Features

- FM receiver
  - 76 MHz to 108 MHz FM bands
  - European Radio Data Systems (RDS) and North American Radio Broadcast Data System (RBDS) modulation support
- I^2C-compatible BSC communications support
- Stereo analog output
- I^2S and PCM interfaces

REVISION HISTORY

Revision	Date	Description
4325-DS04-R	6/30/09	**Updated:** • Title • “General Decsription: on page i • “Bluetooth Features” on page ii • “Overview” on page 1 • Table 2, ”Crystal Interface Signal Characteristics,” on page 6 • Table 3, ”LPO Signal Requirements,” on page 9 • “Bluetooth Features” on page 11 • “Bluetooth 2.1 and 3.0 Features” on page 14 • “Bluetooth UART Interface” on page 20 • “One-Time-Programmable (OTP) Memory” on page 33 • “JTAG Interface” on page 34 • Table 8, ”196-Ball FBGA Signal Descriptions,” on page 43 • Table 9, ”339-Pin WLCSP Signal Descriptions,” on page 52 • Table 14, ”WLAN GPIO Functions and Strapping Options,” on page 67 • Table 21, ”ESD Specifications,” on page 75 • Table 22, ”Environmental Ratings,” on page 76 • Table 23, ”Recommended Operating Conditions and DC Characteristics,” on page 76 • “WLAN Receiver Blocking Performance” on page 86 • “SDIO Host Timing Requirement” on page 107 • Table 57, ”Ordering Information,” on page 120
4325-DS03-R	3/11/09	**Updated:** • General Description on page i • Features on page ii • “Overview” on page 1 • “Mobile Phone Usage Model” on page 2 • “Power Supply Topology” on page 4 • “Reset Circuits” on page 5 • “Crystal Interface and Clock Generation” on page 6 • Table 2, ”Crystal Interface Signal Characteristics,” on page 6 • Figure 6, ”Recommended Oscillator Configuration,” on page 7 • “Frequency Selection” on page 8 • Table 3, ”LPO Signal Requirements,” on page 9 • “Broadcom Serial Control (BSC) Bus” on page 23 • Table 6, ”196-Ball FBGA Signal Assignments by Ball Number,” on page 37 • Table 7, ”339-Pin WLCSP Signal Assignments by Pin Number and X- and Y-Coordinates,” on page 39 • Table 8, ”196-Ball FBGA Signal Descriptions,” on page 43 • Table 9, ”339-Pin WLCSP Signal Descriptions,” on page 53 • Table 14, ”WLAN GPIO Functions and Strapping Options,” on page 68 • Table 15, ”BT GPIO Signals,” on page 69 • Table 17, ”BT/FM Interface I/O Status,” on page 72 • Table 18, ”WLAN Interface I/O Status,” on page 74 • Table 20, ”Absolute Maximum Ratings,” on page 76

Revision	*Date*	*Description*
		• Section 16 ”Operating Conditions and DC Characteristics” on page 76 (title changed; was DC Characteristics) • Section ”Recommended Operating Conditions” on page 77 (heading changed; was DC Characteristics) • Table 21, ”ESD Specifications,” on page 76 • Table 22, ”Environmental Ratings,” on page 77 • Table 23, ”Recommended Operating Conditions and DC Characteristics,” on page 77 • Table 24, ”Bluetooth and FM Current Consumption,” on page 78 • Table 25, ”WLAN Current Consumption using Power Topology #1 (Vbatt with Buck-Boost),” on page 79 • Table 26, ”Bluetooth Receiver RF Specifications,” on page 80 • Table 27, ”Bluetooth Transmitter RF Specifications,” on page 82 • Table 28, ”FM Receiver Specifications,” on page 83 • Table 31, ”2.4 GHz Band Local Oscillator Specifications,” on page 87 • Table 32, ”2.4 GHz Band Receiver RF Specifications,” on page 88 • Table 34, ”2.4 GHz Band Transmitter RF Specifications,” on page 89 • Table 35, ”5 GHz Band Receiver RF Specifications,” on page 90 • Table 39, ”CLDO,” on page 93 • Table 40, ”LNLDOi,” on page 94 • Table 42, ”Buck-Boost Regulator,” on page 96 • Figure 16, ”UART Timing,” on page 97 • Table , ”SDIO Host Timing Requirement,” on page 108 • Table , ”Reset and Regulator Control Signal Sequencing,” on page 108 • Table , ”Signal and Power-up Sequence Timing Diagrams,” on page 108 • “Package Thermal Characteristics” on page 114 • “Miscellaneous Characteristics” on page 115 • Table 57, ”Ordering Information,” on page 121 **Added:** • Figure 32, ”Power-Up Timing for WL ON and BT ON (WL REG_ON signal connected to WL_RST_N, BT separated),” on page 112 • Figure 33, ”Power-Up Timing for WL OFF and BT ON (WL REG_ON signal connected to WL_RST_N, BT separated),” on page 113 • Figure 34, ”Power-Up Timing for WL ON and BT OFF (WL REG_ON signal connected to WL_RST_N, BT separated),” on page 113

Revision	*Date*	*Description*
4325-DS02-R	08/15/08	**Updated:** • Figure 8, ”Power Supply Building Blocks,” on page 27. • Table 3, ”Crystal Interface Signal Characteristics,” on page 31. • Voltage for integrated LDO pins in Table 7 on page 44 and Table 8 on page 53. • Table 19, ”Absolute Maximum Ratings,” on page 75. • Table 20, ”Recommended Operating Conditions and DC Characteristics,” on page 75. • Table 28, ”2.4-GHz Band Transmitter RF Specifications,” on page 85. • Table 30, ”2.4-GHz Receiver Performance Specifications,” on page 86. • Table 49, ”196-Ball FBGA Package Thermal Characteristics,” on page 110. • Figure 28, ”339-Pin WLCSP Mechanical Information,” on page 113. • Table 52, ”Ordering Information,” on page 118.Added: • Figure 9, ”Power Topology Example,” on page 28. • Table 15, ”Pin Default Pull-Up/Pull-Down,” on page 69. • Table 16, ”BT/FM Interface I/O Status,” on page 71. • Table 17, ”WLAN Interface I/O Status,” on page 72. • Table 21, ”Bluetooth and FM Current,” on page 76. • “SDIO Timing” on page 102. • Section 21 ”Power-Up Sequence and Timing” on page 105. • Figure 24, ”Power-Up Timing for WL Off and BT Off (VDDC Provided Externally),” on page 108. • Table 51, ”Miscellaneous Characteristics,” on page 111. • Figure 30, ”WLAN Section Second Metal Keepout Area,” on page 115.
4325-DS01-R	12/14/07	**Updated:** • General Description on page i • Features on page ii • Figure 2, ”BCM4325 Block Diagram,” on page 1 • Section 2 ”Bluetooth + FM Subsystem Overview” on page 2 • Integrated Section 3 into Section 2 ”Bluetooth + FM Subsystem Overview” on page 2 • Section 4 ”Microprocessor and Memory Unit for Bluetooth”: “External Reset” on page 11 • Section 6 ”FM Receiver Subsystem”: - RDS/RBDS” on page 18 - Other Features” on page 18 • Section 8 ”WLAN 802.11 Radio Subsystem”: “Transmitter Path” on page 25 • Section 12 ”BCM4325 On-Chip Power Supplies”: - Figure 8, ”BCM4325 Power Supply Building Blocks,” on page 28 - BCM4325 Example Power Supply Topology” on page 29 - Removed “BCM4325 Power Supply Applications–Power Efficiency • Section 13 ”Frequency References”: - Table 3, ”Crystal Interface Signal Characteristics,” on page 32 - Figure 11, ”Recommended Oscillator Configuration,” on page 33 - Figure 12, ”Recommended TCXO Connection,” on page 33

Revision	Date	Description
4325-DS01-R (Cont.)	12/14/07	**Added:** • Section 14 ”Pinout and Signal Descriptions”: - Table 6, ”339-Pin WLCSP Signal Assignments by Pin Number and X- and Y-Coordinates,” on page 38 - Table 7, ”196-Ball FBGA Signal Descriptions,” on page 42 - Table 8, ”339-Pin WLCSP Signal Descriptions,” on page 51 - Table 9, ”BT_VDDO Domain (1.8V to 3.3V),” on page 63 - Table 10, ”VDDIO Domain (1.8V to 3.3V),” on page 64 - Table 11, ”VDDIO_RF Domain (1.8V to 3.3V),” on page 65 - Table 12, ”VDDIO_SD Domain (1.8V to 3.3V),” on page 65 • “WLAN GPIO Signals” on page 66 • Section 17 ”WLAN RF Specifications” - Table 24, ”2.4-GHz Band Transmitter RF Specifications,” on page 81 - Table 26, ”2.4-GHz Receiver Performance Specifications,” on page 82 - Table 29, ”5-GHz Band Local Oscillator Frequency Generator Specifications,” on page 83 • Section 18 ”BCM4325 Internal Regulator Electrical Specifications”: - Table 31, ”CLDO,” on page 85 - Table 32, ”LNLDOi,” on page 86 - Table 34, ”Core Buck Regulator,” on page 87 - Table 35, ”Buck-Boost Regulator,” on page 88 - Added: “Regulator Current” on page 89 - Removed Analog/RF Buck Regulator section • Section 22 ”Mechanical Information”: “339-Pin WLCSP Mechanical Information” on page 107 • Table 46, ”Environmental Characteristics,” on page 105 • Section 24 ”WLCSP Keepout Area”
4325-DS00-R	03/22/07	Initial release

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Overview

The Broadcom® BCM4325 single-chip device provides the highest level of integration for a mobile or handheld wireless system, with integrated IEEE 802.11™ a/b/g (MAC/baseband/radio), Bluetooth® 3.0 + HS, and an FM receiver. Designed to address the needs of highly mobile devices that require minimal power consumption and board area, the BCM4325 provides a compact ultra-small form-factor solution with minimal external components. This solution drives down the costs for mass volumes, while allowing for flexibility in size, form, and function of handheld devices. It is targeted at addressing the needs of highly mobile devices that require minimal power consumption and reliable operation.

Figure 2 shows the interconnects for the major physical blocks in the BCM4325 and associated external interfaces, which are described in greater detail in subsequent sections of this document.

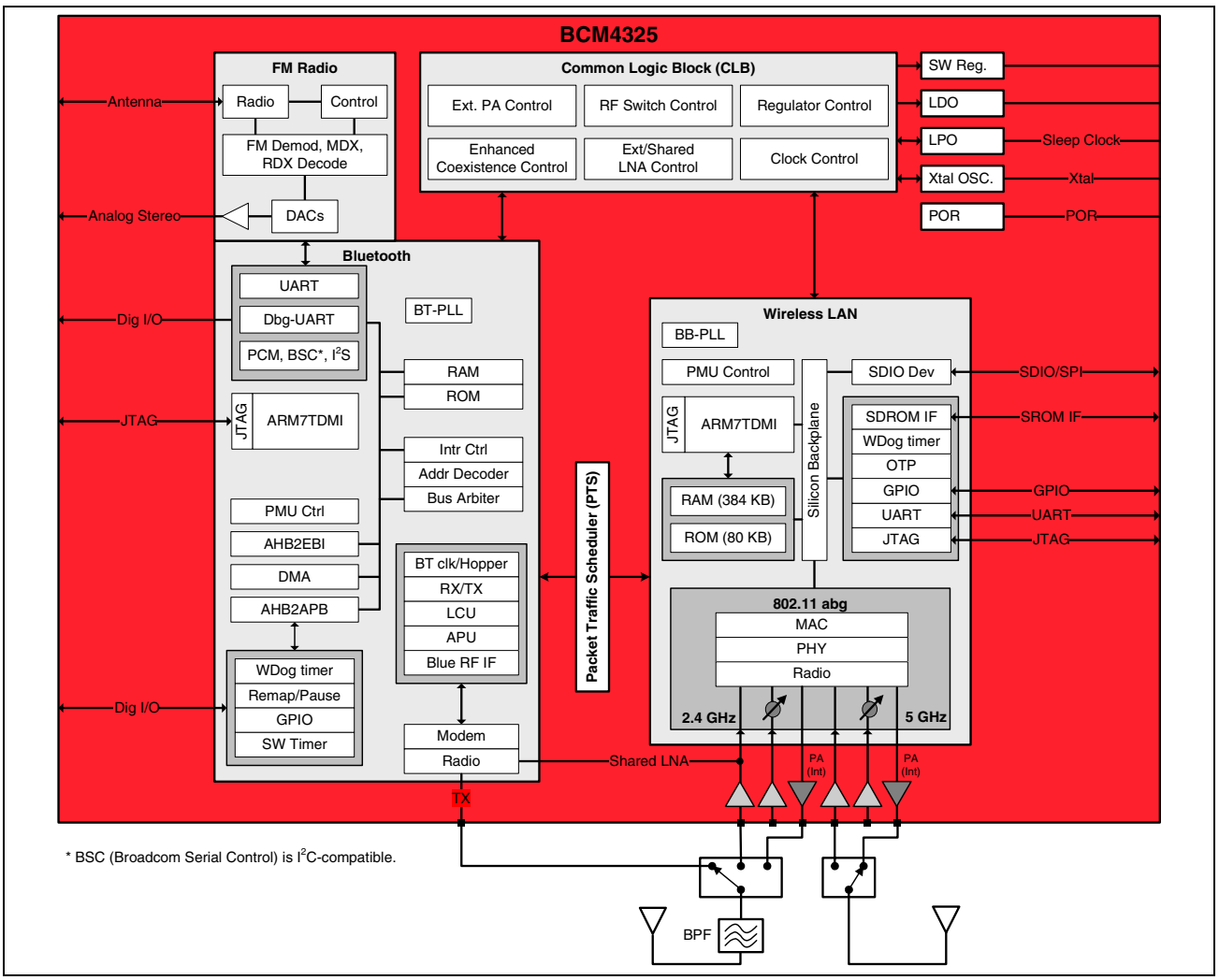


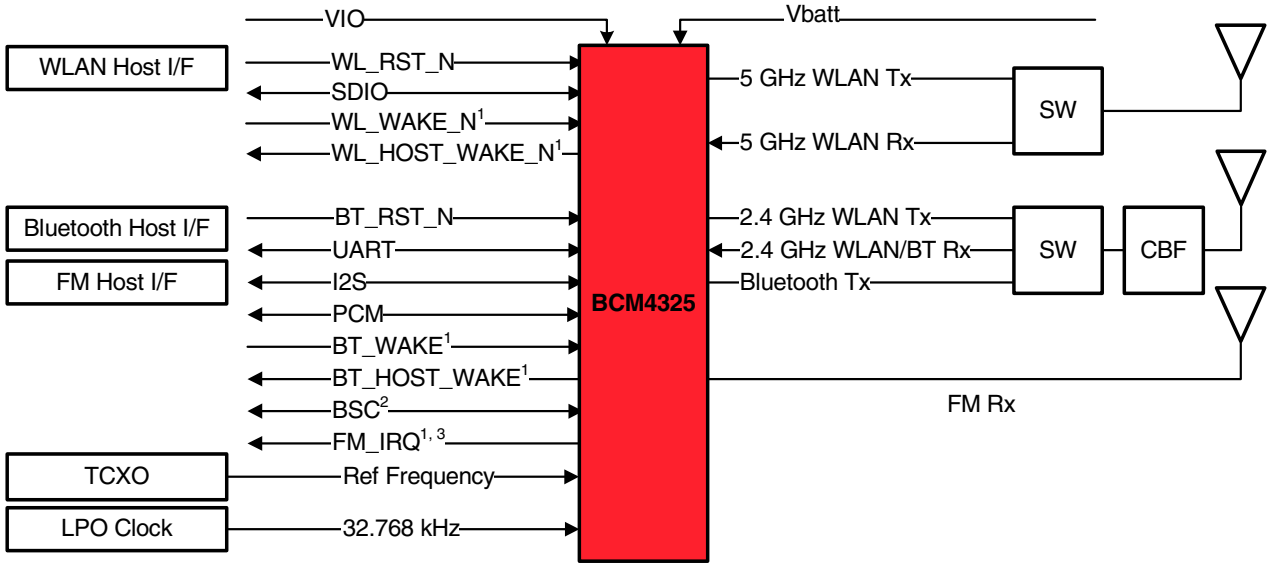
Figure 2: BCM4325 Block Diagram

MOBILE PHONE USAGE MODEL

The BCM4325 incorporates a number of unique features to simplify integration into mobile phone platforms. Its flexible PCM and UART interfaces enable it to transparently connect with the existing circuits. In addition, the TCXO and LPO inputs allow the use of existing handset features to further minimize the size, power, and cost of the complete system.

- The PCM interface provides multiple modes of operation to support both master and slave as well as hybrid interfacing to single or multiple external codec devices.
- The UART interface supports hardware flow control with tight integration to power control side band signaling to support the lowest power operation.
- The TCXO interface accommodates any of the typical reference frequencies used by cell phones.
- The BSC and analog FM interfaces are available for legacy systems.
- New FM digital interfaces can use either I^2S or PCM.
- The highly linear design of the radio transceiver ensures that the device has the lowest output of spurious emissions regardless of the state of operation. It has been fully characterized in the global cellular bands.
- The transceiver design has excellent blocking (eliminating desensitization of the Bluetooth receiver) and inter-modulation performance (distortion of the transmitted signal caused by the mixing of the cellular and Bluetooth transmissions) in the presence of any cellular transmission (GSM, GPRS, CDMA, WCDMA, or iDEN). Minimal external filtering is required for integration inside the handset.

The BCM4325 is designed to provide direct interface with new and existing handset designs, as shown in Figure 3.



Notes: 1. Indication for optional GPIO functions.
2. BSC is Phillips® I^2C-compatible.
3. For information on the FM_IRQ signal, refer to the following Broadcom documents: *BCM4325 FM_RDS Block Setup Quick Start Guide* (4325-QSG100-X) and *FM Command and Control Specification* (4325-AN400-X).

Figure 3: BCM4325 System Block Diagram

Section 2: On-Chip Power Supplies and Reset

The BCM4325 contains power supply building blocks, including one buck-boost switching regulator, one buck switching regulator, and five low-noise LDOs to simplify power supply design for Bluetooth and WLAN interfaces in embedded designs. From a single host power supply, power configurations can be implemented using the BCM4325 on-chip power elements to create a self contained design. All of the regulators are available with the 339-pin WLCSP package. The 196-ball FBGA package does not provide access to LNLDO4.

Figure 4 shows available voltage and current from each integrated regulator.

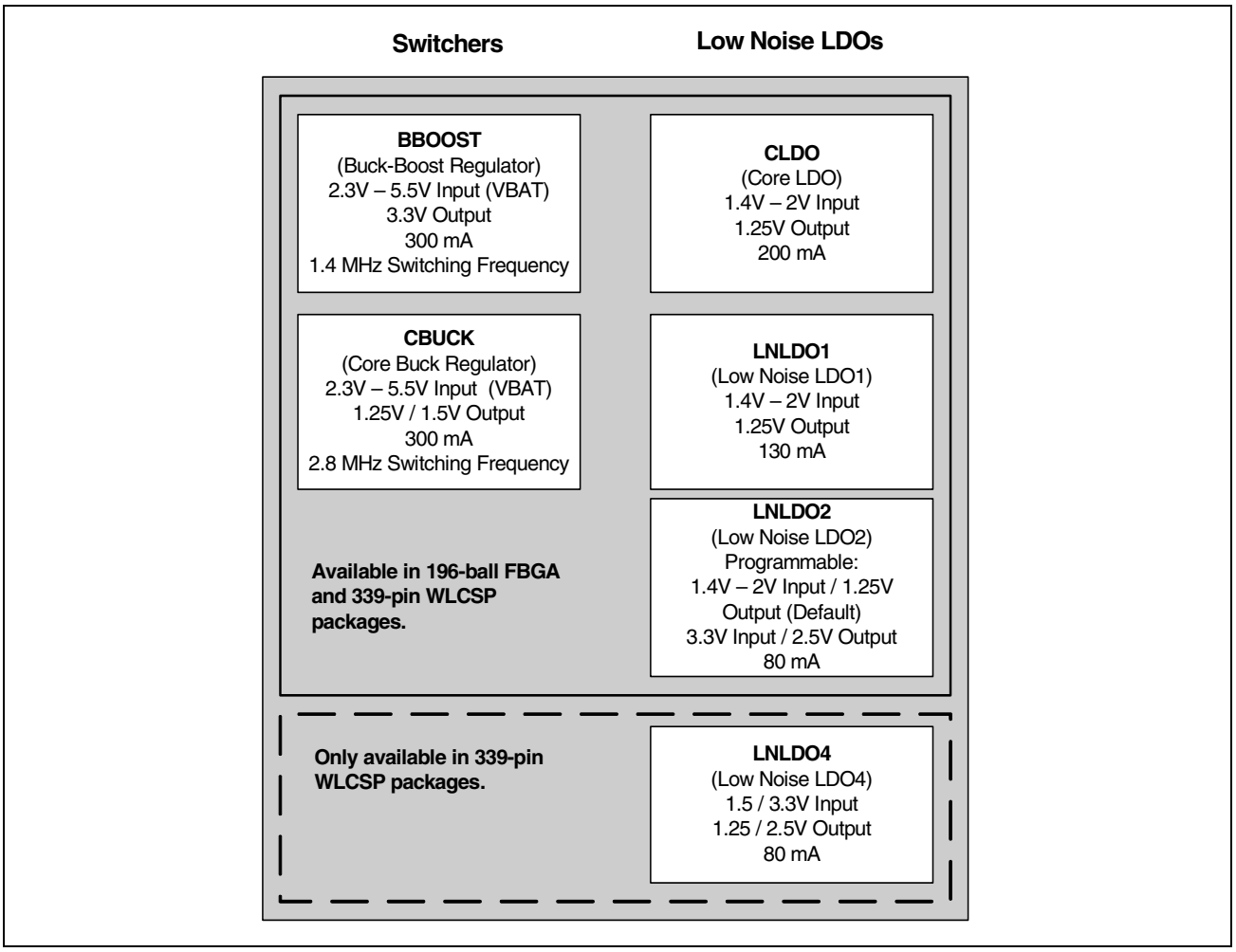


Figure 4: Power Supply Building Blocks

POWER SUPPLY TOPOLOGY

At least seven different power supply topologies can be supported by the voltage regulators available on the BCM4325. Figure 5 shows one example of a power topology for an application with Bluetooth Class 1 PA, FM and WLAN supplied by a variable battery voltage (Vbatt).

To achieve maximum performance from the integrated WLAN Power Amplifiers (PAs), the VDDPA power supply voltages must remain within the recommended operating voltage range. If the supply voltage to the PA deviates outside this range, the linearity of the PA will be degraded, resulting in lower throughput and shorter range. To avoid this condition, the buck-boost regulator can be used to provide a constant 3.3V supply to the PA over the full range of the Vbatt voltage variation. The trade-off is the additional components required for the buck-boost regulator versus the impaired performance if it is not used.

Complete details of all seven power supply topologies are provided in the *BCM4325 Power Supply Topologies* application note (document number 4325-AN60X-R), available on docSAFE.

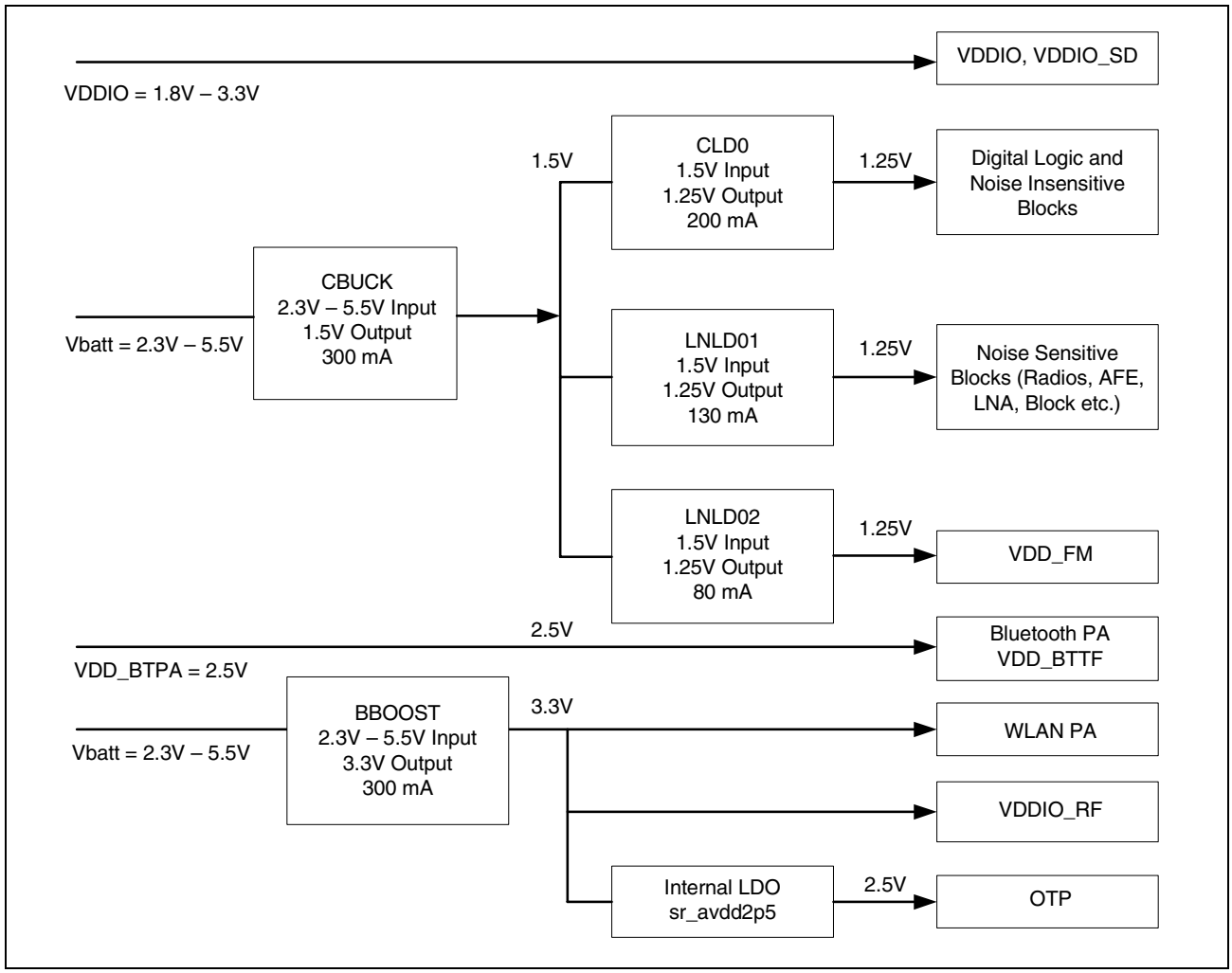


Figure 5: Power Topology Example

RESET CIRCUITS

The BCM4325 has four signals (see Table 1) that enable or disable the Bluetooth and WLAN circuits, and the internal regulator blocks, allowing the host to control power consumption.

Table 1: Reset Control Signals

Signal	*Description*
WL_REG_ON	This signal is used by the PMU (with BT_REG_ON) to decide whether or not to power down the internal BCM4325 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. If WL_RST_N is low (regardless of the BT_RST_N state), the WLAN core is powered off.
BT_REG_ON	This signal is used by the PMU (with WL_REG_ON) to decide whether or not to power down the internal BCM4325 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled.
WL_RST_N	Low asserting reset for the WLAN core. This pin must be driven high or low (not left floating).
BT_RST_N	Low asserting reset for the Bluetooth core. This pin must be driven high or low (not left floating).

Note: WL_REG_ON and BT_REG_ON are OR gated together in the BCM4325.

For detailed timing diagrams of these signals and the required power-up sequences, see Section 22: “Power-Up Sequence and Timing” on page 107.

Section 3: Frequency References

The BCM4325 uses the following external frequency references for normal and low-power operational modes:

- An external crystal or external frequency reference driven by a temperature-compensated crystal oscillator (TCXO) signal for generating all radio frequencies and normal operation clocking.
- An external 32.768-kHz Low Power Oscillator (LPO) for low-power mode timing.

Crystal Interface and Clock Generation

The BCM4325 uses a fractional-N synthesizer to generate the radio frequencies, clocks, and data/packet timing that enables it to operate using a wide range of frequency references. An external source, such as a TCXO or a crystal interfaced directly to the BCM4325, can be used. The default frequency reference setting is a 26 MHz crystal or TCXO. Table 2 list the requirements and characteristics for the crystal or frequency reference.

Table 2: Crystal Interface Signal Characteristics

Parameter	*Crystal*	*External Freq. Reference*	*Units*
Frequency range	12–52 MHz in 2 ppm steps[d]	12–52 MHz, in 2-ppm steps [b]	–
Crystal load capacitance	12 [e]	N/A	pF
ESR (maximum)	60	–	Ω
Power dissipation, max	200	–	uW
Input signal AC amplitude	N/A	400 to 1200 [f]	mVp-p
Signal type	N/A	Square wave or sine wave	–
Input impedance	N/A	≥ 1 ≤ 4.7	MΩ pF
Phase noise (maximum for f = 26 MHz [a]) 1 kHz 10 kHz 100 kHz 1 MHz	 – – – –	 ≤ –100 ≤ –115 ≤ –120 ≤ –140	 dBc/Hz dBc/Hz dBc/Hz dBc/Hz
Auto-detection frequencies when using LPO [b, c]	12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 38.4	12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 38.4	MHz
Frequency tolerance plus over temperature without trimming	±20	±20	ppm
Initial frequency tolerance trimming range	±50	±50	ppm
Time for stable system clock after power up or XTAL_PU assertion	Warm-up time < 6 ms	Maximum hold time for host < 6 ms	ms

a. For a clock reference other than 26 MHz, 20*log10(f/26) dB should be added to the limits, where f = the reference clock frequency in MHz.
b. Auto-detection of frequencies requires that the crystal or external frequency reference have less than 50 ppm of variation, and the external LPO frequency have less than 200 ppm of variation at the time of auto-detection.
c. 52 MHz frequency reference is also supported. The BT_TM6 signal should be pulled low for 52 MHz clock reference.
d. The frequency step size is approximately 80 Hz resolution.
e. The precise value of load capacitance to center the frequency tolerance is dependent on board layout; see Broadcom reference schematics for exact values.

f. If the input signal amplitude is below 800 mV p-p, contact your Broadcom representative for applications assistance. DC coupled digital clock with swing less than 1.32V is supported.

CRYSTAL OSCILLATOR

The BCM4325 can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 6.

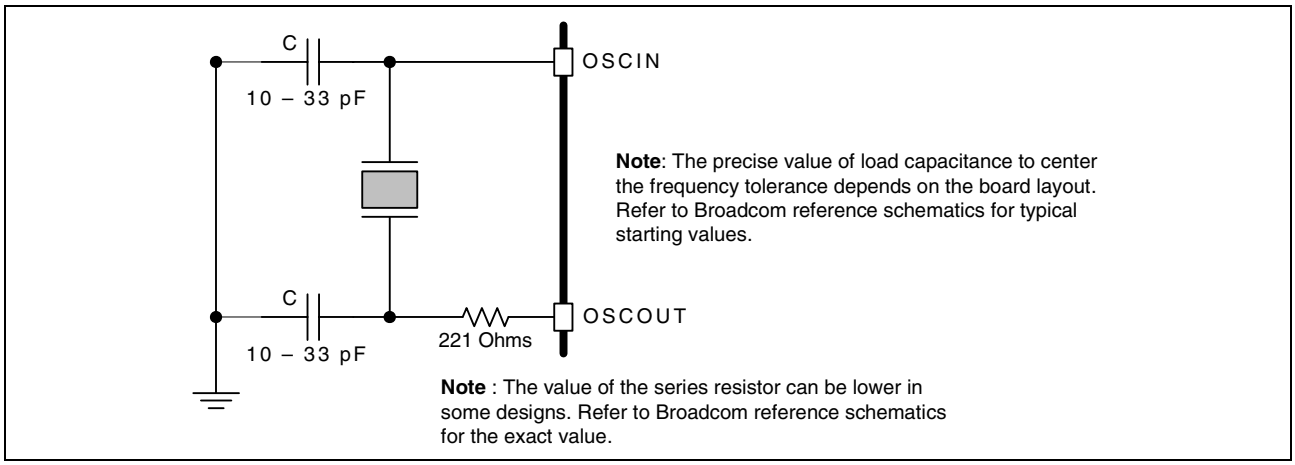


Figure 6: Recommended Oscillator Configuration

EXTERNAL FREQUENCY REFERENCE

As an alternative to a crystal, an external frequency reference, such as a TCXO signal, can be connected to the OSCIN pin on the BCM4325 via a D.C. blocking capacitor, as shown in Figure 7. The external frequency reference input is designed to not change the loading on the TCXO when the BCM4325 is powered up or powered down.

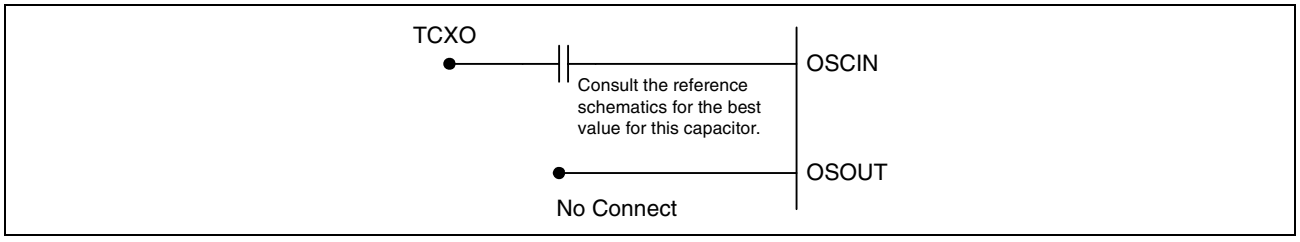


Figure 7: Recommended TCXO Connection

FREQUENCY SELECTION

Any frequency within the ranges specified for the crystal and TCXO reference may be used. These include not only the standard handset references frequencies of 12, 13, 14.4, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, 38.4, and 52 MHz, but any other frequency between these as desired by the system designer. The BCM4325 must have the reference frequency set correctly in order for any of the UART or PCM interfaces to function correctly, since all bit timing is derived from the reference frequency.

The reference frequency for the BCM4325 may be set in one of the following ways:

- Specify the frequency in the nvram.txt file.
- Auto-detect the standard handset reference frequencies using an external LPO clock.

The BCM4325 is set at the factory to a default frequency of 26 MHz. For a typical design using a crystal it is recommended that the default frequency be used.

For applications such as handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the BCM4325 automatically detects the reference frequency and programs itself to the correct reference frequency. In order for auto-frequency detection to work correctly, the BCM4325 must have a valid and stable 32.768-kHz LPO clock present during power-on reset.

FREQUENCY TRIMMING

The BCM4325 uses a fractional-N synthesizer to digitally fine tune the frequency reference input to within ±2 ppm tuning accuracy. This trimming function can be applied to either the crystal or an external frequency source such as a TCXO. Unlike the typical crystal trimming methods used, the BCM4325 changes the frequency using a fully digital implementation and is much more stable and unaffected by either the crystal characteristics or the temperature. The input impedance and loading characteristics remain unchanged on either the TCXO or the crystal during the trimming process and are unaffected by process and temperature variations.

The option of whether to use frequency trimming would be determined by a cost trade-off between the cost of the crystal and the added manufacturing cost associated with frequency trimming. Frequency trimming value can be stored in the host and written back to the BCM4325.

LPO Clock Interface

An additional frequency reference is the LPO clock that the BCM4325 uses to provide low-power mode timing for park, hold, and sniff. The LPO clock should be provided externally to the device from a stable and accurate 32.768-kHz source.

Table 3: LPO Signal Requirements

Parameter	*LPO Clock*	*Units*
Nominal input frequency	32.768	kHz
Frequency accuracy	±200 [a]	ppm
Duty cycle	30% to 70%	–
Jitter (when FM is used)	less than 1	Hz (integrated from 300 Hz to 15 kHz)
Input signal amplitude	200 to 1800	mV, p-p
Signal type	Square wave or sine wave	–
Input impedance[b]	>100k < 5	Ω pF

a. ±150 if FM is used. See *Broadcom Bluetooth® SoC Crystal, TCXO, RFIC, and LPO User Guide* (43XX_20XX-1xx-R) for details.
b. When power is applied, or switched off.

Section 4: Bluetooth + FM Subsystem Overview

The Broadcom BCM4325 includes a Bluetooth® 3.0 + HS compliant standalone baseband processor with an integrated 2.4 GHz transceiver, integrated FM and RDS/RBDS receiver, and an integrated FM baseband processor. It features the highest level of integration and eliminates all critical external components, thus minimizing the footprint and system cost of implementing a Bluetooth and FM solution. The BCM4325 is firmware upgradable for future specifications.

The BCM4325 is the optimal solution for any voice or data application that requires the Bluetooth SIG standard Host Controller Interface (HCI) using a high-speed UART and PCM. The BCM4325 incorporates all Bluetooth 2.1 + EDR features including eSCO, AFH, Fast Connect, all EDR packet types and lengths, and all errata. The BCM4325 also includes InConcert and other industry-collaborative coexistence solutions.

Note: The BCM4325 is designed to be firmware upgradable to any foreseeable future enhancements to the Bluetooth specification by the Bluetooth SIG.

The Bluetooth radio transceiver provides enhanced radio performance to meet the most stringent industrial temperature applications and the tightest integration into mobile handsets and portable devices. It is fully compatible with all standard TCXO frequencies and provides full radio compatibility to operate simultaneously with GPS and cellular radios.

The BCM4325 also integrates a complete FM and RDS/RBDS solution. The integrated solution saves power and board space, minimizes the BOM, and maximizes interface flexibility over a separate Bluetooth and FM solution. The FM subsystem can operate independently of Bluetooth and achieve full performance while Bluetooth is operating. It is designed to cover from 76 MHz, up to 108 MHz, bands (US, Europe, Japan) and to operate from a 32 kHz LPO input. The FM subsystem supports an I^2C-compliant Broadcom Serial Control (BSC) interface and analog outputs for legacy systems, as well as digital interface options, such as I^2S and PCM. The I^2S and PCM interfaces support 48 kHz operation and can be configured as either master or slave. The analog interface consists of high-quality, line-level stereo DACs.

The BCM4325 FM subsystem includes advanced RDS/RBDS capability. The BCM4325 synchronizes, demodulates, and decodes RDS/RBDS signals including CRC processing, post data filter detection, signal quality estimation, and buffering thus making it easy for an external application to read and process the RDS/RBDS data.

The FM radio provides excellent reception, with 1 µV for 26 dB (S+N)/N typical sensitivity and greater than 60 dB SNDR capability, allowing easier system integration and antenna design. The FM subsystem includes many sought after features, including signal-dependant mono/stereo blend, soft mute, and signal bandwidth control. The system has digital RSSI, signal quality, and IF frequency error indicators for system monitoring. The FM subsystem contains embedded automatic search and scan features, and large RDS data buffers to simplify the interface with an external host.

FEATURES

BLUETOOTH FEATURES

Major Bluetooth features of the BCM4325 include:

- Supports key features of upcoming Bluetooth standards
- Class 1 support with PA bias adjust
- Support for BT v3.0 + HS features combined with Broadcom's v3.0 + HS qualified host software, including alternate MAC/PHY, read encryption key size, enhanced power control, and unicast connectionless data.
- Fully supports Bluetooth Core Specification version 2.1 + EDR features:
  - Adaptive Frequency Hopping (AFH)
  - Quality of Service (QoS)
  - Extended Synchronous Connections (eSCO)—Voice Connections
  - Fast Connect
  - Secure Simple Pairing (SSP)
  - Sniff Subrating (SSR)
  - Encryption Pause Resume (EPR)
  - Extended Inquiry Response (EIR)
  - Link Supervision Timeout (LST)
- Maximum UART baud rates up to four Mbps
- Supports Bluetooth Enhanced Data Rate (EDR)
- Supports maximum Bluetooth data rates over HCI UART
- Multipoint operation with up to seven active slaves
  - Maximum of seven simultaneous active ACL links
  - Maximum of three simultaneous active SCO and eSCO with scatternet support
- Scatternet operation with up to four active piconets with background scan and support for scatter mode
- High-speed HCI UART transport support with low-power out-of-band BT_WAKE and HOST_WAKE signaling (see "Host Controller Power Management" on page 16)
- Channel quality driven data rate and packet type selection
- Standard Bluetooth test modes
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth clock request
  - Bluetooth standard park, hold, and sniff
  - Deep sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power oscillator (LDO), which can be used during power save mode for better timing accuracy

FM RADIO FEATURES

Major FM Radio features include:

- 76 MHz to 108 MHz FM bands supported (US, Europe, and Japan)
- Excellent FM radio performance with 1 μV sensitivity for 26 dB (S+N)/N
- FM subsystem control using the BSC bus or through the Bluetooth HCI interface
- Signal dependent stereo/mono blending
- Signal dependent soft mute
- Auto search and tuning modes
- Audio silence detection
- RSSI, IF frequency, status indicators
- RDS and RBDS demodulator and decoder with filter and buffering functions
- Automatic frequency jump
- FM subsystem operates from 32 kHz low-power oscillator (LPO) or reference clock inputs
- Improved audio interface capabilities with full-featured PCM, I^2S, and analog stereo DAC
- I^2S can be master or slave

BLUETOOTH RADIO

The BCM4325 includes an integrated radio transceiver, optimized for use in 2.4 GHz Bluetooth wireless systems. Its design provides low-power, low-cost, robust communications for applications operating in the globally available, 2.4 GHz, unlicensed ISM band. The radio transceiver is fully compliant with Bluetooth radio and EDR specifications and meets or exceeds the requirements to provide the highest communication link quality of service.

Note: Sharing a single 2.4 GHz antenna between the Bluetooth and WLAN sections is supported when an appropriate SP3T switch is used in the external RF signal path.

TRANSMIT

The BCM4325 features a fully integrated zero-IF transmitter. The baseband transmit data is digitally GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier (PA), and RF filtering. The transmitter path also incorporates new modulation schemes π/4-DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR.

Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK, Π/4DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

Power Amplifier

The fully integrated PA provides a maximum output signal level (see Table 27: "Bluetooth Transmitter RF Specifications," on page 81) using a highly linearized, temperature compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, no external filters are required for meeting Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications where the Bluetooth is integrated next to the cellular radio minimal external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions.

The integrated power amplifier is Bluetooth Class 2 compliant and includes power control adjustment with a 28 dB range and 4 dB nominal step size. The integrated power amplifier can be configured as a PA driver to an external power amplifier for full Bluetooth Class 1 compliance.

RECEIVE

The receiver path uses a low-IF scheme to down convert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front end topology with built-in out-of-band attenuation enables the BCM4325 to be used in most applications with no off-chip filtering. For integrated handset operation where the Bluetooth function is integrated close to the cellular transmitter, minimal external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer takes the low-IF received signal and performs an optimal frequency tracking and bit synchronization algorithm.

Receiver Signal Strength Indicator

The radio portion of the BCM4325 provides an Receiver Signal Strength Indicator (RSSI) signal to the baseband so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

LOCAL OSCILLATOR GENERATION

Local Oscillator generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The local oscillator generation subblock employs an architecture for high immunity to local oscillation pulling during PA operation. The BCM4325 uses an internal RF and IF loop filter.

CALIBRATION

The BCM4325 radio transceiver features an automated calibration scheme that is fully self contained in the radio. No user interaction is required during normal operation or during manufacturing to provide the optimal performance. Calibration optimizes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

Section 5: Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time critical functions required for high performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

Bluetooth 2.1 and 3.0 Features

The BBC supports the following Bluetooth 2.1 features:

- Extended Inquiry Response (EIR) — Shortens the time to retrieve device name, specific profile and mode.
- Encryption Pause Resume (EPR) — Enables the use of Bluetooth technology in a much more secure environment.
- Sniff Subrating (SSR) — Optimizes power consumption for low duty cycle asymmetrical data flow, which subsequently extends battery life.
- Simple Pairing (SP) — Reduces the number of steps with minimal or no user interaction when connecting two devices.
- Link Supervision Timeout (LST)

In addition, the BBC is compliant with the Bluetooth Core specification 3.0 + HS when combined with Bluetooth 3.0 + HS qualified host software—including Alternate MAC/PHY, read encryption key size, enhanced power control, and unicast connectionless data.

Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number depending on the link controller state, Bluetooth clock, and the device address.

Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the Link Control Unit (LCU). This layer consists of the command controller that takes commands from the software and other controllers that are either activated or configured by the command controller to perform the link control tasks.

Each task performs a different state function in the Bluetooth link controller.

- Major states
  - Standby
  - Connection
- Substates
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Park
  - Sniff
  - Hold

TEST MODE SUPPORT

The BCM4325 fully supports Bluetooth Test mode as described in Part 1 of the *Specification of the Bluetooth System Version 2.1*. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM4325 also supports enhanced testing features to simplify RF debugging and qualification and type approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

BLUETOOTH POWER MANAGEMENT UNIT

The Bluetooth Power Management Unit (PMU) provides power management features that can be invoked by either software through power management registers, or packet handling in the baseband core.

The power management functions provided by the BCM4325 are:

- RF Power Management
- Host Controller Power Management
- BBC Power Management
- FM Power Management

RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

Host Controller Power Management

When running in UART mode, the BCM4325 may be configured so that dedicated signals are used for power management hand shaking between the BCM4325 and the host. The basic power saving functions supported by those handshaking signals include the standard Bluetooth defined power savings modes and standby modes of operation.

An alternative to using the BT_WAKE and HOST_WAKE signalling uses the CTS and RTS as a combination of UART handshake signals during normal operation and as BT_WAKE and HOST_WAKE when the device is in a power saving mode.

Table 4 describes the power control handshake signals used with the UART interface.

Table 4: Power Control Pin Description

Signal	*Mapped to Pin*	*Type*	*Description*
BT_WAKE	BT_GPIO_0	I	Bluetooth device wakeup. Signal from the host to the BCM4325 indicating that the host requires attention. • Asserted: Bluetooth device must wakeup or remain awake. • Deasserted: Bluetooth device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.
HOST_WAKE	BT_GPIO_1	O	Host wake up. Signal from the BCM4325 to the host indicating that the BCM4325 requires attention. • Asserted: Host device must wakeup or remain awake. • Deasserted: Host device may sleep when sleep criteria are met. The polarity of this signal is software configurable and can be asserted high or low.

Note: Successful operation of the power management handshaking signals requires coordination between the BCM4325 firmware and the host software.

BBC Power Management

The following are low power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection modes are sniff, hold, and park. While in these modes, the BCM4325 runs on the low-power oscillator and wakes up after a predefined time period.

FM Power Management

The BCM4325 FM subsystem can operate independently of, or in tandem with, the Bluetooth RF and BBC subsystems. The FM subsystem power management scheme operates in conjunction with the Bluetooth RF and BBC subsystems.

ADAPTIVE FREQUENCY HOPPING

The BCM4325 gathers link quality statistics on a channel by channel basis to facilitate channel assessment and channel map selection. The link quality is determined using both RF and baseband signal processing to provide a more accurate frequency-hop map.

ADVANCED BLUETOOTH/WLAN COEXISTENCE

The BCM4325 includes advanced coexistence technologies that are only possible with a Bluetooth/WLAN integrated die solution. These coexistence technologies are targeted at small form factor platforms such as cell phones and media players, including applications such as VoWLAN + SCO and Video-over-WLAN + High-Fidelity BT stereo. Support is provided for platforms that share a single antenna between Bluetooth and 802.11g. Dual antenna applications are also supported. The BCM4325 radio architecture allows for lossless simultaneous Bluetooth and WLAN reception for shared antenna applications. This is possible only via an integrated solution (shared LNA and joint AGC algorithm). It has superior performance versus implementations that need to arbitrate between Bluetooth and WLAN reception.

The BCM4325 integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. The Packet Traffic Scheduler (PTS) can suitably schedule future packet transmissions (versus merely supporting arbitration on a packet-by-packet basis as employed in discrete Bluetooth/WLAN solutions) and can factor in beacon arrival times, duration of upcoming packet transmissions, etc. Information is exchanged between the Bluetooth and WLAN cores without host processor involvement.

The BCM4325 also supports Transmit Power Control (TPC) on the STA together with standard Bluetooth TPC to limit mutual interference and receiver desensitization. Preemption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth frames. Improved channel classification techniques have been implemented in Bluetooth for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

FAST CONNECTION (INTERLACED PAGE AND INQUIRY SCANS)

The BCM4325 supports page scan and inquiry scan modes that significantly reduce the average inquiry response and connection times. These scanning modes are compatible with the Bluetooth version 2.1 page and inquiry procedures.

Section 6: Microprocessor and Memory Unit for Bluetooth

The Bluetooth microprocessor core is based on ARM7TDMIS® 32 bit RISC processor with embedded ICE-RT debug and JTAG interface units. It runs software from the link control layer, up to the Host Controller Interface (HCI).

The ARM core is paired with a memory unit that contains 256 KB of ROM memory for program storage and boot ROM, 48 KB of RAM for data scratchpad and patch RAM code. The internal boot ROM allows for flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM memory.

External patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions. These patches may be downloaded from the host to the BCM4325 through the UART transports. The mechanism for downloading via UART is identical to the proven interface of the BCM2045 device.

RAM, ROM, and Patch Memory

The BCM4325 Bluetooth core has 48 KB of internal RAM which is mapped between general purpose scratch pad memory and patch memory and 256 KB of ROM used for the lower layer protocol stack, test mode software, and boot ROM. The patch memory capability enables the addition of code changes for purposes of feature additions and bug fixes to the ROM memory.

Section 7: Bluetooth Peripheral Transport Unit

PCM Interface for Bluetooth and SCO Audio

The PCM Interface on the BCM4325 can connect to linear PCM Codec devices in master or slave mode. In master mode, the BCM4325 generates the BT_PCM_CLK and BT_PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM4325.

The BCM4325 supports up to three SCO or eSCO channels through the PCM Interface and each channel can be independently mapped to any of the available slots in a frame.

The configuration of the PCM interface may be adjusted by the host through the use of Vendor Specific HCI Commands.

Figure 8 shows three options for connecting a BCM4325 to a PCM codec device as either a master or slave connection.

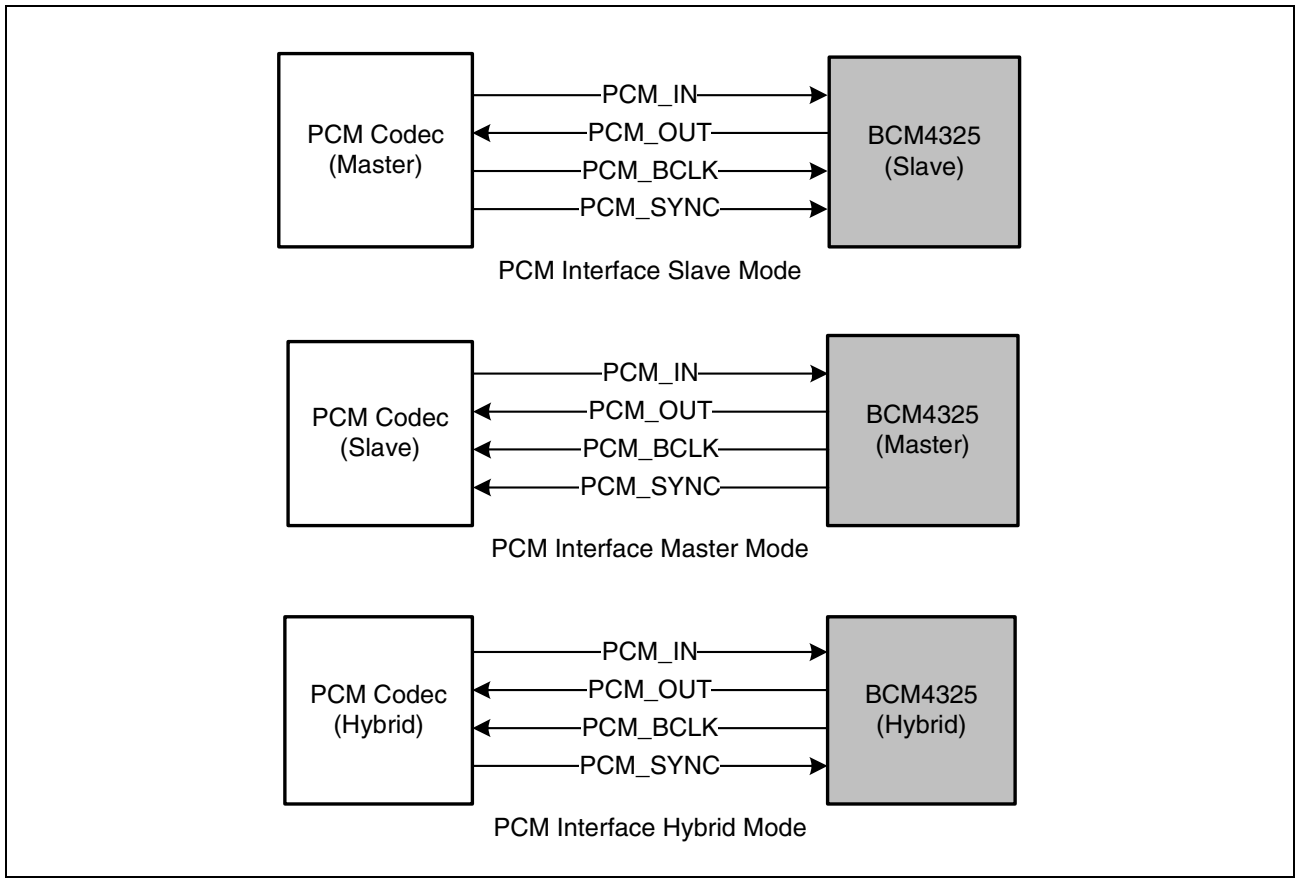


Figure 8: PCM Interface with Linear PCM Codec

SLOT MAPPING

The BCM4325 supports up to three simultaneous full-duplex SCO or eSCO channels. These three channels are time multiplexed onto the single PCM interface by using a time slotting scheme where the 8-kHz audio sample interval is divided into up to 16 slots. The number of slots is dependant on the selected interface rate of 128 kHz, 256 kHz, 512 kHz, 1024 kHz, or 2048 kHz. The corresponding number of slots for these interface rates is one, two, four, eight and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

FRAME SYNC

The BCM4325 supports both short and long frame sync types in both master and slave configurations. In the short frame sync mode, the frame sync signal is an active-high pulse at the 8 kHz audio frame rate that is a single-bit period in width and synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In the long frame sync mode, the frame sync signal is again an active-high pulse at the 8 kHz audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

DATA FORMATTING

The BCM4325 may be configured to generate and accept several different data formats. The BCM4325 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits is configurable to support various data formats on the PCM interface. The remaining three bits are ignored on the input, and may be filled with 0s, 1s, sign bit, or a programmed value on the output. The default format is 13-bit, 2's complement data, left-justified, and clocked MSB first.

PCM INTERFACE FOR FM AUDIO

The BCM4325 also supports a mode where the FM stereo audio is output over the PCM Interface in master or slave mode. A BT_PCM_SYNC sample rate of 48 kHz is supported with associated BT_PCM_CLK rate of 1.536 MHz. The BT_PCM_SYNC signal follows the short frame sync format. In this FM audio mode, the BT_PCM_IN signal is ignored and FM audio is output on the BT_PCM_OUT signal. The FM stereo audio is presented MSB first onto the BT_PCM_OUT signal with the 16 bits of left-channel data first followed by the 16 bits of right-channel data.

BLUETOOTH UART INTERFACE

The Bluetooth UART physical interface is a standard, 4-wire interface (RX, TX, RTS, CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected via a vendor specific UART HCI command. The BCM4325 has a 480-byte receive FIFO and a 480-byte transmit FIFO to support EDR. The interface supports the Bluetooth 3.0 UART HCI specification.

The BCM4325 has the added capability to perform wake-on-activity, where it can be asleep and have activity on the RX or CTS inputs to wake up the chip.

In order to support both high and low baud rates efficiently, the UART clock can be selected as either 24 or 48 MHz. Generally, the higher speed clock is needed for baud rates over 3 Mbaud, however a lower speed clock may be used to achieve a more accurate baud rate under 3 Mbaud. The baud rate of the BCM4325 UART is controlled by two values. The first is a UART clock divisor (also called the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (also called the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

When setting the baud rate manually, the UART clock divisor is an 8-bit value that is stored as a 256 desired divisor. For example, a desired divisor of 13 is stored as 256 – 13 = 243 = 0xF3.

The baud rate adjustment is also an 8-bit value, of which the four MSBs are the number of additional clock cycles to insert in the first half of each bit time, and the four LSBs are the number of clock cycles to insert in the second half of each bit time. If either of these two values is over eight, it is rounded to eight.

To program the baud rate for high-rate mode (greater than 1.5 Mbaud), divide UART clock by the desired rate to compute the number of UART clock cycles per bit. This number must be from eight to 15 for the high-rate mode, and is programmed into the DLBR as 256 minus the number of clocks. For three Mbaud, the calculation would be as follows:

24,000,000/3,000,000 = 8 and 256 – 8 = 248 = 0xF8.

To compute normal 2048 baud rate mode (<1.5 Mbaud), the calculation is expressed as:

24 MHz/((16xUART clock divisor) + total inserted 24 MHz clock cycles)

Table 5 contains example values to generate common baud rates.

Table 5: Common Baud Rate Examples

Desired Baud Rate (bps)	*UART Clock Divisor[a]*	*Baud Rate Adjustment*		*Actual Baud Rate (bps)*	*Error (%)*
		High Nibble	*Low Nibble*		
4000000	0xF4	0x00	0x00	4000000	0.00
3692000	0xF3	0x00	0x00	3692308	0.01
3000000	0xF8	0x00	0x00	3000000	0.00
2000000	0xF4	0x00	0x00	2000000	0.00
1500000	0xFF	0x00	0x00	1500000	0.00
1444444	0xFE	0x00	0x01	1454544	0.70
921600	0xFF	0x05	0x05	923077	0.16
460800	0xFD	0x02	0x02	461538	0.16
230400	0xFA	0x04	0x04	230796	0.17
115200	0xF3	0x00	0x00	115385	0.16
57600	0xE6	0x00	0x00	57692	0.16
38400	0xD9	0x01	0x00	38400	0.00
28800	0xCC	0x00	0x00	28846	0.16
19200	0xB2	0x01	0x01	19200	0.00
14400	0x98	0x00	0x00	14423	0.16
9600	0x64	0x02	0x02	9600	0.00

a. The value in this column is 256 minus the desired divisor.

Normally, the UART baud rate is set by a configuration record downloaded after reset or automatic baud rate detection and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is provided through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The BCM4325 UART operates correctly with the host UART, if the combined baud rate error of the two devices is within ±5%.

AUTO-BAUDRATE DETECTION

The BCM4325 may be put into a state where it attempts to automatically detect the baud rate. This is done by holding the BT_UART_CTS_N signal low during reset or power up. An auto-baud character A (0x41) or the HCI_RESET command {0x01, 0x03, 0x0C, 0x00} can be sent from the host to train the BCM4325 UART when this feature is used.

The corresponding successful returns from BCM4325 auto-baud response are:

{0x41, 0x30, 0x34, 0x31} for the autobaud character

{0x04, 0x0E, 0x04, 0x01, 0x03, 0x0C, 0x00, 0x34, 0x31} for the HCI_RESET command

The run-time configuration download through the vendor specified commands is required to further configure the BCM4325 for normal operations. The BCM4325 can automatically detect baud rates up to the external crystal frequency divided by 16.

I^2S INTERFACE

The 3-wire I^2S interface for FM audio supports both master and slave modes. Input reference clock frequencies of 13 MHz, 19.2 MHz, 26 MHz, and 38.4 MHz are supported.

The three I^2S signals are:

I^2S Clock:	I2S_SCK
I^2S Word Select:	I2S_WS
I^2S Data Out:	I2S_SDO

I2S_SCK and I2S_WS become outputs in Master mode and inputs in Slave mode, while I2S_SDO always stays as an output. I^2S data input is not supported. The channel word length is 16 bits and the data is justified so that the MSB of the left channel data is aligned with the MSB of the I^2S bus, per the I^2S specification. The MSB of each data word is transmitted one bit clock cycle after the I2S_WS transition, synchronous with the falling edge of bit clock. Left channel data is transmitted when I2S_WS is low, and right channel data is transmitted when I2S_WS is high. Data bits sent by the BCM4325 are synchronized with the falling edge of I2S_SCK and should be sampled by the receiver on the rising edge of I2S_SSCK.

The clock rate in master mode is either of the following:

48 kHz x 32 bits per frame = 1.536 MHz

48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider. In Slave mode, any clock rate is supported to a maximum of 3.072 MHz.

The I2S_SCK interface is available as multiplexed signals onto:

- PCM interface
- Class 1 control signals

Section 8: FM Receiver Subsystem

The BCM4325 includes a completely integrated FM radio receiver with RDS/RBDS, covering all FM bands from 76 MHz to 108 MHz. The receiver is controlled through commands on the BSC bus or the HCI. FM audio is available as stereo analog output or in digital form through I^2S or PCM. The FM subsystem can operate independently or in tandem with the Bluetooth subsystem and can be powered up or down separately.

SENSITIVITY

The internal LNA has a noise figure (NF) of 6 dB, which helps achieve excellent sensitivity of –107 dBm, or 1 μV in 50Ω.

PLL TUNING

Clocks are locked to a reference clock or a 32.768 kHz external LPO, and no factory alignment is required.

DIGITAL FM OUTPUT

The FM radio audio is available digitally through the shared PCM and I^2S pins and the sampling rate is nominally at 48 kHz. The PCM interface runs off either the FM or the Bluetooth clock. The BCM4325 supports 3-wire I^2S audio interface in either master or slave configuration. The master or slave configuration is selected via HCI commands. In addition, multiple sampling rates are supported, derived from either the FM or Bluetooth clocks.

ANALOG FM OUTPUT

The demodulated FM audio signal is available as line-level analog stereo output, generated by twin internal 16-bit DACs.

BROADCOM SERIAL CONTROL (BSC) BUS

The BCM4325 implements an I^2C-compatible BSC slave bus interface to control the FM subsystem. The BSC bus interface depends on the reference clock input being active. The interface supports a clock rate up to 400 kHz. The BSC slave address is programmable using the UART HCI interface and requires a configuration download. The interface supports 7-bit addressing mode and may require external pull-ups. Initial BSC communication has to be conducted at 100 kHz.

RDS/RBDS

The BCM4325 integrates a RDS/RBDS demodulator and decoder with programmable filtering and buffering functions. The RDS/RBDS data can be read out through either the HCI or BSC interfaces.

In addition, the RDS/RBDS functionality supports the following:

- Block decoding, error correction and synchronization
- Storage capability up to 126 blocks of RDS data
- Full or partial block B match detect and interrupt to host
- Audio pause detection with programmable parameters
- Program Identification (PI) code detection and interrupt to host
- Automatic frequency jump
- Block E filtering
- Soft mute
- Signal dependant mono/stereo blend
- Programmable de-emphasis

OTHER FEATURES

- Single-ended or differential FM RF input
- Auto search and tuning
- Digital-level indicator (RSSI, IF Frequency)
- Low current consumption

Section 9: Wireless LAN Functional Description

INTRODUCTION TO IEEE STD 802.11

IEEE Std 802.11 defines two different ways to configure a wireless network: ad hoc mode and infrastructure mode. In ad hoc mode, nodes are brought together to form a network on the fly, whereas infrastructure mode uses fixed access points through which mobile nodes can communicate. These network access points are sometimes connected to wired networks through bridging or routing functions.

The medium access control (MAC) layer is a contention-resolution protocol that is responsible for maintaining order in the use of a shared wireless medium. IEEE 802.11 specifies both contention-based and contention-free channel access mechanisms. The contention-based scheme is also called the distributed coordination function and the contention-free scheme is also called the point coordination function.

The distributed coordination function employs a carrier sense multiple access with collision avoidance (CSMA/CA) protocol. In this protocol, when the MAC receives a packet to be transmitted from its higher layer, the MAC first listens to ensure that no other node is transmitting. If the channel is clear, it then transmits the packet. Otherwise, it chooses a random backoff factor that determines the amount of time the node must wait until it is allowed to transmit its packet. During periods in which the channel is clear, the MAC waiting to transmit decrements its backoff counter, and when the channel is busy, it does not decrement its backoff counter. When the backoff counter reaches zero, the MAC transmits the packet. Because the probability that two nodes will choose the same backoff factor is low, collisions between packets are minimized. Collision detection, as employed in Ethernet, cannot be used for the radio frequency transmissions of devices following IEEE 802.11. The IEEE 802.11 nodes are half-duplex—when a node is transmitting, it cannot hear any other node in the system that is transmitting because its own signal drowns out any others arriving at the node.

Optionally, when a packet is to be transmitted, the transmitting node can first send out a short request to send (RTS) packet containing information on the length of the packet. If the receiving node hears the RTS, it responds with a short clear to send (CTS) packet. After this exchange, the transmitting node sends its packet. When the packet is received successfully, as determined by a cyclic redundancy check (CRC), the receiving node transmits an acknowledgment (ACK) packet. This back and forth exchange is necessary to avoid the hidden node problem. Hidden node is a situation where node A can communicate with node B, node B can communicate with node C, but node A cannot communicate with node C. For instance, although node A can sense that the channel is clear, node C can be transmitting to node B. This protocol alerts node A that node B is busy, and that it must wait before transmitting its packet.

IEEE 802.11A/G MAC FEATURES

The IEEE 802.11a/g MAC features include:

- Programmable independent basic service set (IBSS), or infrastructure mode
- Passive scanning
- Network allocation vector (NAV), inter-frame space (IFS), and timing synchronization function (TSF) functionality
- Backoff
- RTS/CTS procedure
- Transmission of response frames (ACK/CTS)
- Address filtering of RX frames as specified by IBSS rules

- Multirate support
- Frame-bursting and afterburner
- Programmable target beacon transmission time (TBTT), beacon transmission/cancellation and programmable announcement traffic indication message (ATIM) window
- CF conformance: setting NAV for neighborhood point coordination function operation
- Privacy through a variety of Wired Equivalent Privacy (WEP) encryption schemes and dynamically programmable WEP keys
- Power management
- Statistics counters for MIB support

IEEE 802.11A/G MAC DESCRIPTION

The MAC core provides the support required for the transmission and reception of sequences of packets, together with related timing, without any packet-by-packet driver interaction. Time critical tasks requiring response times of only a few milliseconds are handled in the MAC core. This achieves the required timing on the medium while keeping the host driver easier to write and maintain. Also, incoming packets are buffered in the MAC core, which allows the MAC driver to process them in bursts as and when it gets access to the buffers.

The MAC driver interacts with the MAC core to prepare queues of packets to transmit and to analyze and forward received packets. The internal blocks of the MAC core are connected to a Programmable State Machine (PSM) through an internal bus. See Figure 9.

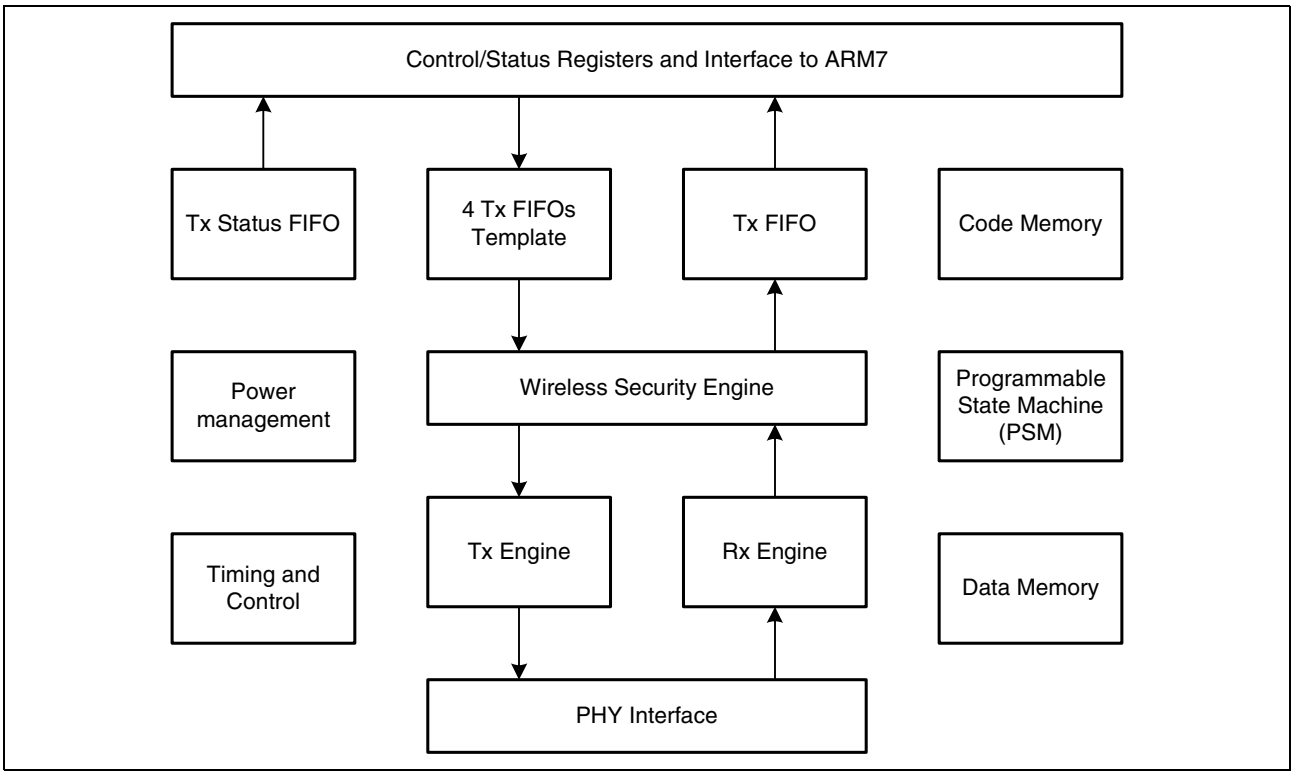


Figure 9: IEEE 802.11a/g MAC Block Diagram

There are registers for controlling and monitoring the status of the MAC core and interfacing with the TX/RX FIFOs. There are four transmit FIFOs: asynchronous, priority, Broadcast/Multicast (BC/MC) and ATIM. Each transmit FIFO is 3 KB deep. In addition to the transmit FIFOs, there is a 1-KB template area for response frames. Whenever the CPU has a frame to transmit, the CPU queues the frame into one of the transmit FIFOs with a TX descriptor containing TX control information. The PSM schedules the transmission on the medium depending on the frame type, transmission rules in IEEE 802.11 protocol, and the current medium occupancy scenario. After the transmission is completed and an ACK is received, a TX status is returned to the host confirming the same in the TX status FIFO.

The MAC contains a single 4.5 KB RX FIFO. Whenever a frame is received, the frame is sent to the ARM processor along with an RX descriptor that contains additional information about the frame reception conditions.

The Power Management block maintains the information regarding the power management state of the core to help in dynamic decisions by the core regarding frame transmission.

The WEP block performs the required WEP operation on the TX/RX frames. The WEP block supports separate transmit and receive keys with four shared keys and 50 link-specific keys. The link-specific keys are used to establish a secure link between any two STAs, with the required key being shared between only those two STAs and hence excluding all the other STAs in the same network from deciphering the communication between those two STAs. The WEP block supports the following encryption schemes that can be selected on a per destination basis:

- None: The WEP block acts as a passthrough
- WEP: 40-bit secure key and 24-bit IV as defined in IEEE Std 802.11-1999
- WEP128: 104-bit secure key and 24-bit IV
- WEP2: 128-bit secure key and 128-bit IV
- TKIP: 802.11i
- AES: 802.11i

The transmit engine is responsible for the byte flow from the TX FIFO to the PHY interface through the WEP block and the addition of an FCS (CRC-32) as required by IEEE 802.11. Similarly, the receive engine is responsible for byte flow from the PHY interface to the RX FIFO through the WEP block and for detection of errors in the RX frame.

The timing block performs the TSF, NAV, and IFS functionality as described in IEEE 802.11-1999.

The Programmable State Machine (PSM) coordinates the operation of different hardware blocks required for both transmission and reception. The PSM also maintains the statistics counters required for MIB support.

IEEE 802.11A/G PHY FEATURES

The integrated IEEE 802.11a/g physical layer device (PHY) features include:

- Data rates of 1, 2, 5.5, 6, 9, 11, 12, 18, 24, 36, 48, and 54 Mbit/s
- Programmable antenna selection
- Automatic gain control (AGC)
- Available per packet channel quality and signal strength measurements
- Dual antenna support with single weight combiner

IEEE 802.11A/G PHY DESCRIPTION

The Wireless Local Area Network (WLAN) PHY integrated in this IC provides baseband processing at data rates of 1, 2, 5.5, 6, 9, and 11, 12, 18, 24, 36, 48, and 54 Mbit/s, as specified in the direct sequence spread spectrum (DSSS) and orthogonal frequency division multiplexing (OFDM) portions of IEEE 802.11a/g. This core acts as an intermediary between the MAC on the one hand, and the integrated 2.4 GHz/5 GHz radio integrated circuit on the other, converting back and forth between packets and baseband waveforms.

An overview of the operations carried out by the PHY is shown on Figure 10. Upon transmission, physical layer framing is first added to a packet received from the MAC. The resulting bits are then scrambled, modulated, filtered, and finally sent to the radio through a pair of 80 MHz, 9-bit Digital-to-Analog Converters (DACs). Modulation is selected per packet as either differential binary phase shift keying (DBPSK), differential quadrature phase shift keying (DQPSK), complementary code keying (CCK), or OFDM. The first two types of modulation provide data rates of 1 Mbps and 2 Mbps, respectively, and require spreading the modulated symbols with a length 11 Barker code. CCK modulation is used for data rates of 5.5 Mbps and 11 Mbps and inherently includes the spreading. OFDM modulation is used for data rates of 6, 9, 12, 18, 24, 36, 48, and 54 Mbps. A high data rate is achieved by using multiple carriers that are modulated using binary or quadrature phase shift keying (BPSK or QPSK) or using 16- or 64-quadrature amplitude modulation (16 QAM or 64 QAM).

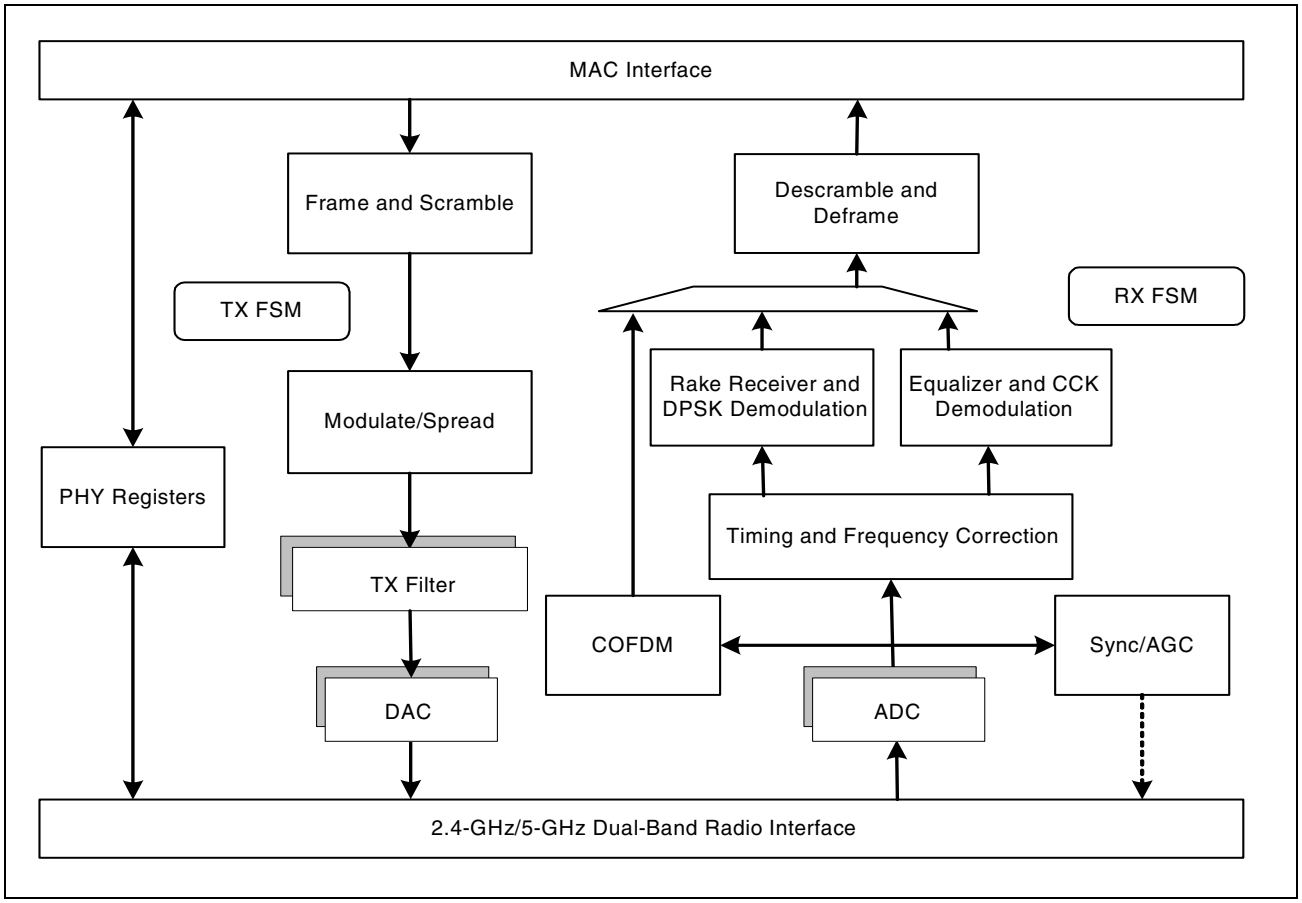


Figure 10: IEEE 802.11a/g PHY Block Diagram

On reception, the reverse operations are performed. The inphase (I) and quadrature (Q) baseband waveforms coming from a pair of 40 MHz, 9-bit ADCs are demodulated into bits and then descrambled and deframed. To improve the likelihood of correct reception, however, the waveforms are subjected to timing and frequency offset corrections (adapted throughout packet reception) prior to demodulation.

Additionally, the receiver must perform synchronization at the start of packet reception, which includes automatic gain control (AGC), antenna selection, and frequency offset and timing estimation. A state machine coordinates all of these activities (using information from the PHY framing) to decide how to handle the packet body.

A register interface accessible from both the MAC and the host allows programming of the PHY parameters, although information generally needed per packet is passed as part of the packet itself. For example, this is true of preamble type and data rate on transmission, as well as the channel metrics signal quality (SQ) and signal strength on reception. The internal radio registers are accessed indirectly through the PHY registers.

Section 10: WLAN 802.11 Radio Subsystem

The BCM4325 includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4 GHz or 5 GHz Wireless LAN systems. It is designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM or 5 GHz U-NII bands. With an external transmit power amplifier, it develops full output power per the IEEE 802.11a/g Specification. The transmit and receive sections include all on-chip filtering, mixing, and gain control functions.

Note: Sharing a single 2.4 GHz antenna between the Bluetooth and WLAN sections is supported when an appropriate SP3T switch is used in the external RF signal path.

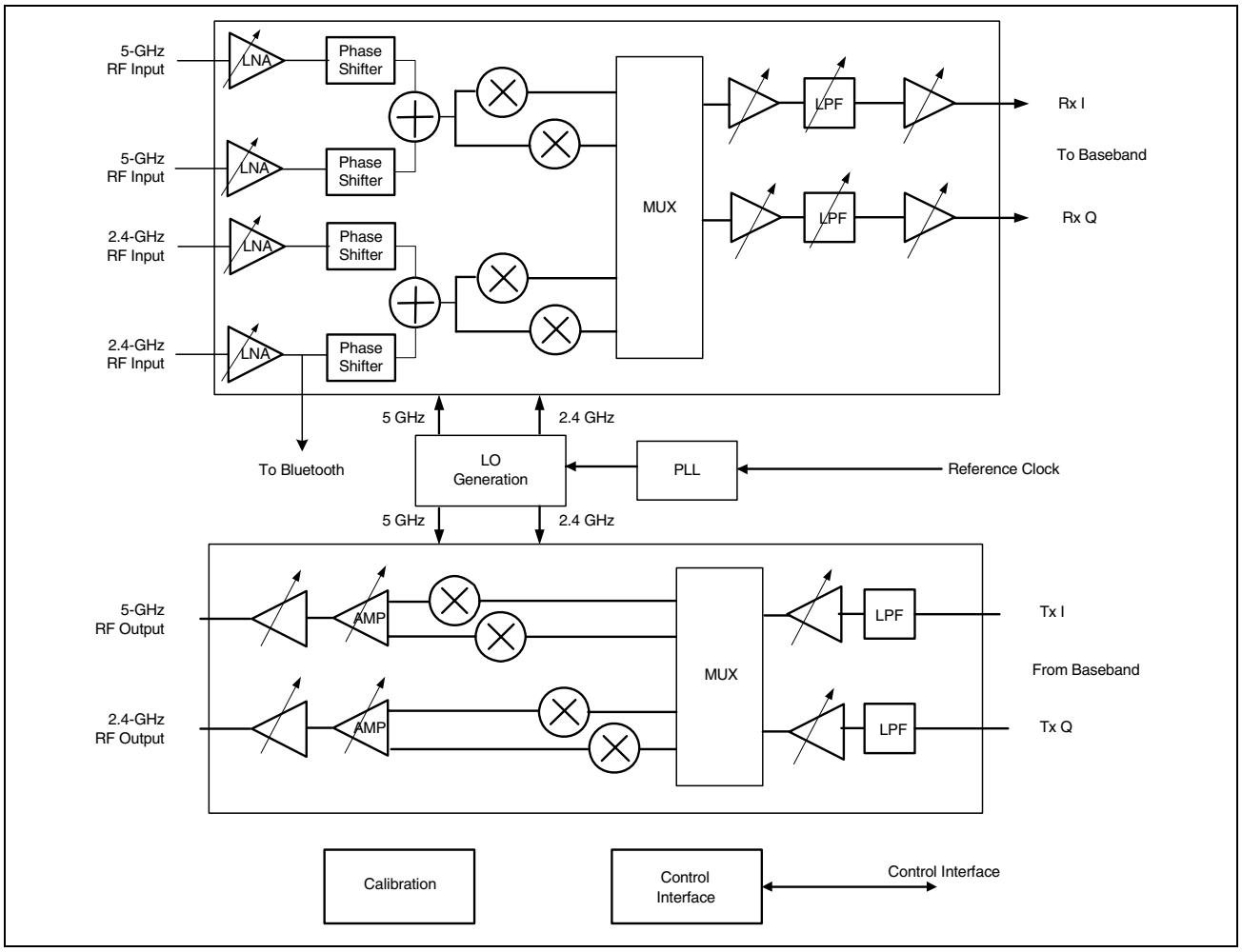


Figure 11: Radio Functional Block Diagram

RECEIVER PATH

The BCM4325 has a wide dynamic range, direct conversion receiver. It employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the entire 5 GHz U-NII band. The excellent noise figure of the receiver makes an external LNA unnecessary.

TRANSMITTER PATH

A linear, on-chip power amplifier is included. This power amplifier is capable of delivering 20 dBm of nominal output power and adheres to IEEE 802.11a and 802.11g specifications. The Tx gain has a 32 dB range with a resolution of 0.25 dB. Baseband data is modulated and upconverted to the 2.4 GHz ISM or 5 GHz U-NII bands, respectively.

CALIBRATION

The BCM4325 features dynamic on-chip calibration, eliminating process variation across components. This enables the BCM4325 to be used in high volume applications, because calibration routines are not required during manufacturing testing. These calibration routines are performed periodically in the course of normal radio operation. An example of this is automatic calibration of the baseband filters for optimum transmit and receive performance.

Section 11: WLAN Power Management

The BCM4325 has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the BCM4325 integrated RAM is a high Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only.

Additionally, the BCM4325 includes an advanced WLAN power management unit (PMU). The PMU provides significant power savings by putting the BCM4325 into various power management states appropriate to the current environment and activities that are being performed. The power management unit enables and disables internal regulators, switches, and other blocks based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them. Power up sequences are fully programmable. Configurable, free running counters (running at 32 kHz LPO clock) in the PMU are used to turn on/turn off individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM4325 WLAN power states are described as follows:

- Power-down mode — The BCM4325 is effectively powered off by shutting down all internal regulators. The chip is brought out of this mode by external logic reenabling the internal regulators.
- Active mode — All BCM4325 WLAN functions are powered up and fully functional with active carrier sensing and frame transmission and receiving. All required regulators are enabled and put in the most efficient mode (PWM or Burst) based on the load current. Clock speeds are dynamically adjusted by the PMU.
- Sleep mode — The WLAN radio, AFE, PLLs, and the ROMs are powered down. The rest of the BCM4325 remains powered up in an IDLE state. All main clocks are shut down. The 32 kHz LPO clock is available only for the PMU. This condition is necessary to allow the PMU to wake up the chip and transition to active mode. In Sleep mode, the primary power consumed is due to leakage current. The external switcher and internal baseband switcher are put into Burst mode (for better efficiency at low load currents).

Section 12: WLAN System Interfaces

SDIO V1.2

The BCM4325 WLAN section supports SDIO version 1.2 for both the 1-bit (25 Mbps), 4-bit (100 Mbps) modes, and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This out-of-band interrupt signal notifies the host when the WLAN device needs to turn on the SDIO interface.

The ability to force control of the gated clocks from within the WLAN chip is also provided.

Three SDIO functions are supported:

- Function 0—Standard SDIO function (Max BlockSize/ByteCount = 32B)
- Function 1—Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize/ ByteCount = 64B)
- Function 2—WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount = 512B)

Detailed SDIO pin description and signal connection block diagrams are provided in Section 14: “Pinout and Signal Descriptions” on page 37.

GPIO Interface

There are five General Purpose I/O (GPIO) pins available on the FBGA package and 15 on the WLCSP package, which can be used to connect to various external devices. Upon power up and reset, these pins become tri-stated. Subsequently, they can be programmed to be either input or output pins via the GPIO control register. An internal pull-up resistor is included on each GPIO. If a GPIO output enable is not asserted, and the corresponding GPIO signal is not being driven externally, the GPIO is read as high.

One-Time-Programmable (OTP) Memory

Various hardware configuration parameters may be stored in an internal 2k-bit OTP memory, which is read by system software after device reset. In addition, customer-specific parameters, including the System Vendor ID and the MAC address can be stored, depending on the specific board design.

The initial state of all bits in an unprogrammed OTP device is 0. Once any bits are programmed to a 1, they can never be reprogrammed back to 0. The entire OTP array can be programmed in a single write cycle using a utility provided with Broadcom's WLAN manufacturing test tools. Alternatively multiple write cycles can be used to selectively program specific bytes, but only bits which are still in the 0 state can be altered during each programming cycle.

Prior to OTP programming, all values should be verified using the appropriate editable nvram.txt file, which is provided with the reference board design package. Documentation on the OTP development process is available at Broadcom’s Customer Support Portal (CSP) at http://www.broadcom.com/support.

As an alternative to using the internal OTP, an external 4-wire SPROM interface can be enabled.

External Coexistence Interface

An external handshake interface is provided to enable signaling between the device and an external co-located wireless device, such as GPS, WiMax or UWB, to manage wireless medium sharing for optimum performance. The provided signals are:

- ERCX_STATUS
- ERCX_RF_ACTIVE
- ERCX_TX_FREQ
- ERCX_TX_PRISEL (WLCSP package only)
- ERCX_TXCONF (WLCSP package only)

JTAG Interface

The BCM4325 supports the IEEE 1149.1 JTAG boundary scan standard for performing device package and PCB assembly testing during manufacturing. In addition, the JTAG interface allows Broadcom to assist customers by using proprietary debug and characterization test tools during board bringup. Therefore, it is highly recommended to provide access to the JTAG pins by means of test points or a header on all PCB designs.

WLAN UART Debug Interface

Two universal asynchronous receiver/transmitter (UART) interfaces are provided for the 339-pin WLCSP package (one UART interface for the 196-ball FBGA package) that can be attached to RS-232 data termination equipment (DTE) for exchanging and managing data with other serial devices. These UART interfaces are primarily used for debugging during development. Each interface is compatible with the industry standard 16550 UART. One UART provides TX and RX signals only. The other UART provides a full set of control signals. Hardware assisted flow control is provided. FIFO size is 64 × 8.

Section 13: Software Architecture

HOST SOFTWARE ARCHITECTURE

The host driver provides a transparent connection between the host operating system and the BCM4325 media (for example, WLAN) by presenting a network driver interface to the host operating system and communicating with the BCM4325 over an interface-specific bus (SPI, SDIO, and so on) to:

- Forward transmit and receive frames between the host network stack and the BCM4325 device, and
- Pass control requests from the host to the BCM4325 device, returning the BCM4325 device responses

The driver communicates with the BCM4325 over the bus using a control channel and a data channel to pass control messages and data messages. The actual message format is based on the BDC protocol.

DEVICE SOFTWARE ARCHITECTURE

The wireless device, protocol, and bus drivers are run on the embedded ARM® processor and a Broadcom-defined operating system called HNDRTE that enables the transfer of 1500-byte Ethernet frames and control frames (using BDC message sets) over the SDIO interface between the host and the device.

This transfer requires a message-oriented (framed) interconnect between the host and device. The SDIO bus is an addressed bus—each host-initiated bus operation contains an explicit device target address—and does not natively support a higher level data frame concept. Broadcom has implemented a hardware/software message encapsulation scheme that ignores the bus operation code address and prefixes each frame with a 4-byte length tag for framing. The device presents a packet level interface over which data, control and asynchronous event (from the device) packets are supported.

The data and control packets received from the bus are initially processed by the bus driver and then passed on to the protocol driver. If the packets are data packets, they are transferred to the wireless device driver (and out through its medium), and a data packet received from the device medium follows the same path in the reverse direction. If the packets are control packets, the protocol header is decoded by the protocol driver. If the packets are wireless IOCTL packets, the IOCTL API of the wireless driver is called to configure the wireless device. The microcode running in the D11 core processes all time critical tasks.

REMOTE DOWNLOADER

The remote downloader is used to download the BCM4325 firmware image into the device from the host. When the BCM4325 device powers up, it is ready to receive the firmware image from the host system.

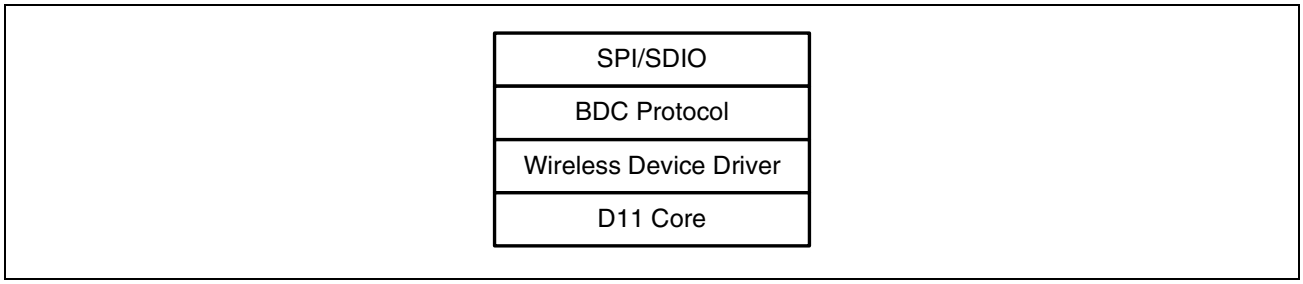


Figure 12: Device Software Architecture

WIRELESS CONFIGURATION UTILITY

The device driver that supports the Broadcom IEEE 802.11 family of wireless solutions provides an input/output control (IOCTL) interface for making advanced configuration settings. The IOCTL interface makes it possible to make settings that are normally not possible when using just the native operating system-specific IEEE 802.11 configuration mechanisms. The utility uses IOCTLs to query or set a number of different driver/chip operating properties.

Section 14: Pinout and Signal Descriptions

SIGNAL ASSIGNMENTS

196-BALL FBGA PINOUT

Table 6: 196-Ball FBGA Signal Assignments by Ball Number

Ball	Signal
A1	SR_VFB1
A2	SR_VBAT1B
A3	SR_VLX1
A4	WL_RST_N
A5	RF_SW_CTRL_N_3
A6	AMODE_TX_PU
A7	RF_SW_CTRL_N_0
A8	WRF_DISABLE_N
A9	WRF_EXTCOUPLE_AIN
A10	WRF_EXTCOUPLE_GIN
A11	WRF_VDDPAG_3P3
A12	WRF_RFOUTP_G
A13	AVSS
A14	WRF_RFOUTP_A
B1	SR_AVDD2P5
B2	SR_PLDO
B3	SR_VBAT1A
B4	JTAG_TRST_N
B5	RF_SW_CTRL_P_3
B6	RF_SW_CTRL_N_1
B7	RF_SW_CTRL_P_0
B8	GMODE_TX_PU
B9	WRF_AFE_AVDD_RXADC
B10	WRF_AFE_TEST_IN
B11	AVSS
B12	AVSS
B13	WRF_VDDPAA_3P3
B14	AVSS
C1	SR_VNLDO
C2	SR_TESTSWG
C3	SR_PVSS
C4	TDO
C5	TEST_SE
C6	VDDIO_RF
C7	WRF_AFE_DIGIT_TEST1
C8	WRF_AFE_TEST_OPI
C9	WRF_AFE_TEST_ONI
C10	WRF_AFE_TSSI_A
C11	AVSS
C12	AVSS
C13	AVSS
C14	AVSS
D1	SR_VFBBB
D2	WL_REG_ON
D3	SR_AVSS
D4	TMS
D5	LV_TESTMODE
D6	GMODE_EXT_LNA_GAIN
D7	WRF_AFE_AVDD_TXDAC
D8	WRF_AFE_TEST_ONQ
D9	WRF_AFE_TEST_OPQ
D10	WRF_AFE_AVDD_AUX
D11	WRF_AFE_TEST_IP
D12	WRF_VDDTX_1P2
D13	AVSS
D14	WRF_RFINP_A1
E1	SR_VLX1BB
E2	SR_VBATBB
E3	BT_REG_ON
E4	VSS
E5	TDI
E6	TAP_SEL
E7	RF_SW_CTRL_P_1
E8	VSS
E9	WRF_AFE_TSSI_G
E10	WRF_BBPLL_VDD_1P2
E11	WRF_AFE_TEST_QP
E12	WRF_AFE_IQADC_VREF
E13	WRF_VDDRX_1P2
E14	WRF_RFINN_A1_XFMR
F1	SR_VLX2BB
F2	SR_PVSSB
F3	ERCX_STATUS
F4	VDDIO
F5	TCK
F6	AMODE_RX_PU
F7	GMODE_RX_PU
F8	VSS
F9	VDDIO_RF
F10	VDDIO_RF
F11	WRF_AFE_TEST_QN
F12	AVSS
F13	WRF_PA_100UA
F14	WRF_RFINP_G1
G1	SR_VOUTBB
G2	WL_GPIO_6
G3	WL_GPIO_1
G4	ERCX_RF_ACTIVE
G5	WL_GPIO_0
G6	VDDIO
G7	VSS
G8	BT_VDDO
G9	VDDC
G10	AVSS
G11	WRF_GPIO_OUT1
G12	WRF_VDDLO_1P2
G13	AVSS
G14	WRF_RFINN_G1_XFMR
H1	SPROM_DOUT
H2	SDIO_DATA_1
H3	WL_UART_RX0
H4	VDDC
H5	OTP_VDD25
H6	VDDIO
H7	ERCX_TX_FREQ
H8	SPROM_DIN
H9	BT_GPIO_1
H10	VDDC
H11	WRF_GPIO_OUT2
H12	WRF_VDDVCO_1P2
H13	WRF_VDDPFDCP_1P2
H14	AVSS
J1	VDDIO_SD
J2	WL_GPIO_2
J3	SDIO_DATA_2
J4	WL_UART_TX0
J5	WL_GPIO_7
J6	SPROM_CS
J7	BT_PCM_CLK
J8	BT_TM6
J9	BT_GPIO_0
J10	BT_VSSC_0
J11	BT_VDDC
J12	WRF_VDDD_1P2
J13	WRF_VDDCAB_1P2
J14	BT_RFION
K1	SDIO_CLK
K2	XTAL_PU
K3	SPROM_CLK
K4	SDIO_CMD
K5	BT_PCM_IN
K6	BT_GPIO_4
K7	BT_GPIO_5
K8	BT_GPIO_7
K9	BT_TM1
K10	BT_GPIO_2
K11	WRF_VDDA_1P2
K12	BT_VDDRF
K13	BTFM_VSS
K14	BT_RFIOP
L1	VOUT_CLDO
L2	SDIO_DATA_0
L3	VDDIO_SD
L4	BT_SDA

Ball	Signal
L5	BT_PCM_OUT
L6	BT_GPIO_6
L7	BT_UART_RXD
L8	BT_TM2
L9	FM_ADVSS
L10	VDD_XTAL
L11	WRF_RES_EXT
L12	WRF_EXTREFIN
L13	BT_VDDIFIFP
L14	BT_VDDTF
M1	VOUT_LNLDO1
M2	VIN_CLDO
M3	VIN_LNLDO1
M4	BT_VSSC_0
M5	BT_PCM_SYNC
M6	BT_GPIO_3
M7	FM_AUDIO_OUT1
M8	FM_ADVDD
M9	FM_AUDIO_OUT2
M10	FM_VDDVCO
M11	FM_CVAR
M12	BTFM_VSS
M13	BT_VDDVCO
M14	BTFM_VSS
N1	VIN_LNLDO2
N2	BT_VDDO
N3	AVDD2P5_LDO
N4	BT_VDDC
N5	BT_SCL
N6	BT_UART_RTS_N
N7	BT_COEX_OUT0
N8	BT_TM0
N9	BT_RST_N
N10	FM_VDDPLL
N11	BTFM_VSS
N12	N/C
N13	N/C
N14	BTFM_VSS
P1	VREF_LDO
P2	AVSS1_LDO
P3	VOUT_LNLDO2
P4	BT_UART_TXD
P5	BT_UART_CTS_N
P6	SDIO_DATA_3
P7	BT_COEX_OUT1
P8	OSCIN
P9	OSCOUT

Ball	Signal
P10	FM_VDDRF
P11	FM_RXP
P12	FM_RXN
P13	FM_VDDIF
P14	BT_VDDPLL

339-PIN WLCSP PINOUT

Note: The X- and Y-coordinate orientation is looking at the silicon face (i.e., looking up at the bottom of the die at the bumps, as opposed to top down). Refer to Figure 36 on page 116 for X- and Y-coordinate origin information.

Note: The WLCSP package was optimized and eight pins were removed (originally 347-pin WLCSP package). However, the CSP package pin out was not renumbered. The following pins were removed: Pin 1 WRF_PA_BYPGND_3P3, Pin 154 VOUT_LNLDO3, Pin 157 VIN_LNLDO3, Pin 258 usb20d_ulpi_stp, Pin 282 usb20d_ulpi_data_6, Pin 283 usb20d_ulpi_data_5, Pin 295 usb20d_ulpi_data_7, and Pin 307 usb20d_ulpi_nxt

Table 7: 339-Pin WLCSP Signal Assignments by Pin Number and X- and Y-Coordinates

Pin #	Signal Name	X-Coord	Y-Coord
2	WRF_RFOUTN_A	184.63	5538.005
3	WRF_VDDPAA_3P3	684.63	5538.005
4	WRF_VDDPAA_3P3	434.63	5538.005
5	WRF_RFOUTP_A	934.63	5538.005
6	WRF_RFOUTN_G	1184.63	5538.005
7	WRF_VDDPAG_3P3	1684.63	5538.005
8	WRF_VDDPAG_3P3	1434.63	5538.005
9	WRF_RFOUTP_G	1934.63	5538.005
10	WRF_AFE_pad_AVSS_RXADC	2186.84	5254.51
11	WRF_AFE_AVDD_RXADC	2523.96	5254.245
12	WRF_AFE_pad_AVSS_TXDAC	2773.96	5254.245
13	WRF_AFE_AVDD_TXDAC	3073.81	5254.245
14	WRF_GNDPAA_3P3	184.63	4933.17
15	WRF_GNDTX_1P2	419.98	4822.4
16	WRF_GNDPAA_3P3	934.63	4933.17
17	WRF_GNDPAG_3P3	1184.63	4902.645
18	WRF_GNDPAG_3P3	1934.63	4902.645
19	WRF_AFE_test_In	2182.26	4954.545
20	WRF_AFE_test_opI	2823.81	5004.235
21	WRF_AFE_test_onQ	3073.81	5004.235
22	WRF_AFE_test_Ip	2182.26	4704.5
23	WRF_AFE_TSSI_A	2573.81	4779.235
24	WRF_AFE_test_onI	2823.81	4754.235
25	WRF_AFE_test_opQ	3073.81	4754.235
26	WRF_RFINN_A2_XFMR	211.8	4663.165
27	WRF_VDDTX_1P2	1551.915	4506.545
28	WRF_AFE_iqadc_VREF	2182.26	4453.92
29	WRF_AFE_AVDD_AUX	2573.81	4529.235
30	WRF_AFE_TSSI_G	3073.81	4504.235
31	WRF_RFINP_A2	211.8	4384.17
32	WRF_EXTCOUPLE_AIN	2676.285	4301.17
33	WRF_BBPLL_VDD_1P2	2926.285	4301.17
34	WRF_AFE_test_Qp	2196.31	4202.195
35	WRF_AFE_test_Qn	2446.31	4202.195
36	WRF_RFINP_A1	211.8	4063.055
37	WRF_EXTCOUPLE_GIN	2676.285	4051.17
38	WRF_BBPLL_GND_1P2	2926.285	4036.35
39	WRF_GNDLO_1P2	1544.575	3877.305
40	WRF_RFINN_A1_XFMR	211.8	3784.06
41	WRF_VDDRX_1P2	461.8	3784.06
42	WRF_GNDRX_1P2	711.8	3605.83
43	WRF_VDDLO_1P2	1544.575	3627.305
44	WRF_GPIO_OUT1	1794.575	3627.305
45	WRF_GPIO_OUT2	2044.575	3627.305
46	WRF_RFINN_G2_XFMR	211.8	3534.045
47	WRF_PA_100UA	461.8	3534.045
48	WRF_RFINP_G2	211.8	3244.045
49	WRF_RFINP_G1	211.8	2956.455
50	WRF_VDDVCO_1P2	1305.455	2993.545
51	WRF_GNDVCO_1P2	1555.455	2993.545
52	WRF_RFINN_G1_XFMR	211.8	2666.455
53	WRF_GNDD_1P2	711.8	2655
54	WRF_VDDD_1P2	961.8	2655
55	WRF_GNDPFDCP_1P2	211.8	2405
56	WRF_VDDPFDCP_1P2	461.8	2405
57	WRF_GNDA_1P2	711.8	2405
58	WRF_VDDA_1P2	961.8	2405
59	WRF_VDDCAB_1P2	211.8	2155
60	WRF_GNDCAB_1P2	461.8	2155
61	WRF_EXTREFIN	1818.185	2155
62	WRF_RES_EXT	2068.185	2155
63	BT_RFION	202	1875
64	BT_VDDRF	452	1875
65	BT_VSSRF	893	1847
66	BT_RFIOP	202	1625
67	BT_VSSPA	452	1625
68	BT_VDDTF	202	1375
69	BT_VSSIF	452	1375
70	BT_VDDIF	202	1125

Pin #	Signal Name	X-Coord	Y-Coord
71	FM_ADVSS	2468	935
72	FM_ADVDD	2839	935
73	BT_VDDVCO	202	748
74	FM_VSSVCO	1492	744
75	FM_AUDIO_OUT2	2468	685
76	FM_AUDIO_OUT1	2839	685
77	BT_VDDPLL	150	435
78	BT_VSSVCO	400	435
79	BT_VSSPLL	650	435
80	No Connect (NC)	900	435
81	No Connect (NC)	1150	435
82	FM_VSSRX	1400	435
83	FM_CVAR	1650	435
84	FM_VSSPLL	1900	435
85	VSS_XTAL	2150	435
86	VDD_XTAL	2400	435
87	DUMMY_BUMP	150	185
88	FM_VSSIF	400	185
89	FM_VDDIF	650	185
90	FM_RXN	900	185
91	FM_RXP	1150	185
92	FM_VDDRX	1400	185
93	FM_VDDVCO	1650	185
94	FM_VDDPLL	1900	185
95	oscin	2150	185
96	oscout	2400	185
97	BT_RST_N	2650	150
98	SR_VFB2	4748	5548
99	SR_VLX2	4998	5548
100	SR_VBAT1A	5248	5548
101	SR_VLX1	5498	5548
102	SR_PVSS1	5748	5548
103	SR_VFB1	5998	5548
104	SR_VBAT1B	6248	5548
105	SR_PVSS2	4872.985	5331.4
106	SR_VLX2	5122.985	5331.4
107	SR_VBAT1A	5372.985	5331.4
108	SR_VLX1	5622.985	5331.4
109	SR_PVSS1	5872.985	5331.4
110	SR_VSSPLDO	6122.985	5331.4
111	SR_PVSS2	4998	5112
112	SR_VBAT1A	5248	5112
113	SR_VLX1	5498	5112
114	SR_PVSS1	5748	5112
115	SR_TESTSWG	5998	5112
116	SR_AVDD2P5	6248	5112
117	SR_AVSS	4872.985	4895.4
118	SR_VBAT1A	5122.985	4895.4
119	SR_AVSS	5622.985	4895.4
120	SR_VDDNLDO	6122.985	4895.4
121	BT_REG_ON	5498	4676
122	SR_VBATBB	5748	4676
123	SR_VBATBB	5998	4676
124	SR_VFBBB	6248	4676
125	WL_REG_ON	5372.985	4459.4
126	SR_VBATBB	5622.985	4459.4
127	SR_VBATBB	5872.985	4459.4
128	SR_VBATBB	6122.985	4459.4
129	SR_VLX1BB	5498	4240
130	SR_VLX1BB	5748	4240
131	SR_VLX1BB	5998	4240
132	SR_VLX1BB	6248	4240
133	SR_PVSSB	5372.985	4023.4
134	SR_PVSSB	5622.985	4023.4
135	SR_PVSSB	5872.985	4023.4
136	SR_PVSSB	6122.985	4023.4
137	SR_VLX2BB	5498	3804
138	SR_VLX2BB	5748	3804
139	SR_VLX2BB	5998	3804
140	SR_VLX2BB	6248	3804
141	SR_VOUTBB	5372.985	3587.4
142	SR_VOUTBB	5622.985	3587.4
143	SR_VOUTBB	5872.985	3587.4
144	SR_VOUTBB	6122.985	3587.4
145	VIN_CLDO	5497.96	1118.285
146	VIN_CLDO	5747.96	1118.285
147	VOUT_CLDO	5997.965	1118.285
148	VOUT_CLDO	6247.97	1118.285
149	VIN_LNLDO1	5497.96	868.285
150	VIN_LNLDO1	5747.96	868.285
151	VOUT_LNLDO1	5997.965	868.285
152	VOUT_LNLDO1	6247.97	868.285
153	AVSS1_LDO	5497.96	618.285
155	VIN_LNLDO2	5997.965	618.285
156	VOUT_LNLDO2	6247.97	618.285
158	VIN_LNLDO4	5997.965	368.285
159	VOUT_LNLDO4	6247.97	368.285
160	AVDD2P5_LDO	5747.96	118.285
161	AVSS2_LDO	5997.965	118.285
162	VREF_LDO	6247.97	118.285
163	packageoption_0	3325	5400
164	rf_sw_ctrl_n_0	3575	5400

Pin #	Signal Name	X-Coord	Y-Coord
165	VDDIO_RF	4075	5400
166	test_se	4325	5400
167	packageoption_1	3325	5150
168	rf_sw_ctrl_p_0	3575	5150
169	wrf_afe_digit_test1	3825	5150
170	rf_sw_ctrl_p_2	4075	5150
171	tdo	4325	5150
172	jtag_trst_n	4575	5150
173	packageoption_2	3325	4900
174	rf_sw_ctrl_n_1	3575	4900
175	gmode_ext_lna_gain	3825	4900
176	rf_sw_ctrl_n_2	4075	4900
177	tap_sel	4325	4900
178	WL_RST_N	4575	4900
179	packageoption_3	3325	4650
180	wrf_disable_n	3575	4650
181	rf_sw_ctrl_p_1	3825	4650
182	amode_tx_pu	4075	4650
183	lv_testmode	4325	4650
184	tck	4575	4650
185	VDDIO_RF	3275	4150
186	gmode_rx_pu	3525	4400
187	gmode_tx_pu	3775	4400
188	amode_ext_lna_gain	4025	4400
189	rf_sw_ctrl_n_3	4275	4400
190	tdi	4525	4400
191	tms	4775	4400
192	VSS	5025	4400
193	VDDIO_RF	3525	4150
194	VDDIO_RF	3775	4150
195	wrf_afe_digit_test2	4025	4150
196	amode_rx_pu	4275	4150
197	rf_sw_ctrl_p_3	4525	4150
198	VDDIO_RF	4775	4150
199	ercx_prisel	5025	4150
200	VDD	3275	3900
201	VDD	3525	3900
202	VDD	3775	3900
203	VDD	4025	3900
204	VSS	4275	3900
205	VDDIO_RF	4525	3900
206	sflash_q	4775	3900
207	ercx_status	5025	3900
208	VSS	3275	3650
209	VSS	3525	3650
210	VDDIO	3775	3650
211	VDD	4025	3650
212	VSS	4275	3650
213	WL_GPIO_0	4525	3650
214	sflash_d	4775	3650
215	ercx_rf_active	5025	3650
216	VDDIO	3775	3400
217	VDD	4025	3400
218	VSS	4275	3400
219	ercx_tx_freq	4525	3400
220	VDD	4775	3400
221	VDD	5025	3400
222	VSS	4025	3150
223	VDDIO	4275	3150
224	WL_GPIO_13	4525	3150
225	WL_GPIO_7	4775	3150
226	VDDIO	5025	3150
227	VDDIO	5275	3150
228	sflash_c	5525	3150
229	sflash_s	5775	3150
230	ercx_txconf	6025	3150
231	BT_VDDO	3025	2900
232	VDD	3775	2900
233	sprom_din	4275	2900
234	otp_vdd25	4525	2900
235	WL_GPIO_14	4775	2900
236	WL_GPIO_9	5025	2900
237	WL_GPIO_5	5275	2900
238	WL_GPIO_4	5525	2900
239	WL_GPIO_2	5775	2900
240	WL_GPIO_1	6025	2900
241	BT_VSSC_0	3025	2650
242	BT_VDDO	3275	2650
243	BT_VDDO	3525	2650
244	VDD	3775	2650
245	VSS	4025	2650
246	sprom_cs	4275	2650
247	wl_uart_rx0	5025	2650
248	WL_GPIO_12	5275	2650
249	WL_GPIO_10	5525	2650
250	WL_GPIO_8	5775	2650
251	WL_GPIO_6	6025	2650
252	BT_GPIO_1	3025	2400
253	BT_VSSC_0	3275	2400
254	BT_VSSC_0	3525	2400
255	BT_VSSC_0	3775	2400
256	VSS	4025	2400

Pin #	Signal Name	X-Coord	Y-Coord
257	VDDIO_SD	4525	2400
259	wl_uart_tx0	5275	2400
260	wl_uart_tx1	5525	2400
261	WL_GPIO_15	5775	2400
262	WL_GPIO_11	6025	2400
263	BT_XA_18	2525	2150
264	BT_GPIO_0	2775	2150
265	BT_XA_17	3025	2150
266	BT_VDDC	3275	2150
267	BT_VDDC	3525	2150
268	BT_PCM_CLK	3775	2150
269	BT_UART_RXD	4025	2150
270	SDIO_DATA_3	4275	2150
271	SDIO_DATA_2	4525	2150
272	SDIO_DATA_1	4775	2150
273	WRF_AFE_DIGIT_TEST0	5025	2150
274	xtal_pu	5775	2150
275	wl_uart_rx1	6025	2150
276	BT_XOE_N	3275	1900
277	BT_COEX_OUT0	3525	1900
278	BT_XA_7	3775	1900
279	BT_XA_15	4025	1900
280	BT_XD_3	4275	1900
281	SDIO_CMD	4525	1900
284	SDIO_DATA_0	5275	1900
285	SDIO_CLK	5525	1900
286	sprom_clk	5775	1900
287	sprom_dout	6025	1900
288	BT_TM1	3275	1650
289	BT_XA_3	3525	1650
290	BT_XA_8	3775	1650
291	BT_UART_RTS_N	4025	1650
292	BT_XD_2	4275	1650
293	BT_XD_4	4525	1650
294	BT_XD_9	4775	1650
296	VDDIO_SD	5275	1650
297	VDDIO_SD	5525	1650
298	BT_GPIO_2	3275	1400
299	BT_XA_1	3525	1400
300	BT_COEX_OUT1	3775	1400
301	BT_XA_12	4025	1400
302	BT_PCM_OUT	4275	1400
303	BT_SDA	4525	1400
304	BT_XD_8	4775	1400
305	BT_XD_10	5025	1400
306	VDD	6000	1400

Pin #	Signal Name	X-Coord	Y-Coord
308	BT_XCS_N	3255	1150
309	BT_TM0	3505	1150
310	BT_XA_5	3755	1150
311	BT_XA_9	4005	1150
312	BT_XA_13	4255	1150
313	BT_XD_1	4505	1150
314	BT_XD_7	4755	1150
315	BT_XD_13	5005	1150
316	BT_TM2	3255	900
317	BT_XA_2	3505	900
318	BT_GPIO_6	3755	900
319	BT_GPIO_3	4005	900
320	BT_VDDC	4255	900
321	BT_UART_TXD	4505	900
322	BT_VSSC_0	4755	900
323	BT_VSSC_0	5005	900
324	BT_XWE_N	3255	650
325	BT_TM6	3505	650
326	BT_XA_6	3755	650
327	BT_XA_10	4005	650
328	BT_PCM_SYNC	4255	650
329	BT_XA_16	4505	650
330	BT_VDDC	4755	650
331	BT_XD_12	5005	650
332	BT_XA_4	3525	400
333	BT_GPIO_5	3775	400
334	BT_XA_11	4025	400
335	BT_XA_14	4275	400
336	BT_SCL	4525	400
337	BT_XD_6	4775	400
338	BT_VDDO	5025	400
339	BT_GPIO_7	3525	150
340	BT_GPIO_4	3775	150
341	BT_PCM_IN	4025	150
342	BT_UART_CTS_N	4275	150
343	BT_XD_0	4525	150
344	BT_XD_5	4775	150
345	BT_XD_11	5025	150
346	BT_XD_14	5275	150
347	BT_XD_15	5525	240

Section 15: Signal Descriptions

196-BALL FBGA PACKAGE

Table 8: 196-Ball FBGA Signal Descriptions

Ball Number	Signal Name	Type	Description
WLAN RF			
A12	WRF_RFOUTP_G	O	WLAN 802.11g Internal Power Amplifier output (50Ω)
A14	WRF_RFOUTP_A	O	WLAN 802.11a Internal Power Amplifier output (50Ω)
F14	WRF_RFINP_G1	I	WLAN 802.11g Internal LNA RX input (50Ω)
D14	WRF_RFINP_A1	I	WLAN 802.11a Internal LNA RX Positive input (100Ω)
G14	WRF_RFINN_G1_XFMR	O	WLAN 802.11g RX transformer ground
E14	WRF_RFINN_A1_XFMR	I	WLAN 802.11a Internal LNA RX Negative input (100Ω)
L11	WRF_RES_EXT	I	Connect to external 15 kΩ resistor to ground
L12	WRF_EXTREFIN	I	32.768 kHz LPO clock input. Used for low-power mode timing
A10	WRF_EXTCOUPLE_GIN	I	WLAN directional coupler input for 802.11g (50Ω)
A9	WRF_EXTCOUPLE_AIN	I	WLAN directional coupler input for 802.11a (50Ω)
E9	WRF_AFE_TSSI_G	I	Transmit signal strength indicator for external 802.11g Power Amplifier
C10	WRF_AFE_TSSI_A	I	Transmit signal strength indicator for external 802.11a Power Amplifier
A8	WRF_DISABLE_N	I	Disables WLAN radio when low.
Integrated LDOs			
P1	VREF_LDO	O	Vref bypass. Connect to external capacitor.
M1	VOUT_LNLDO1	O	1.25V output for LNLDO1, 130 mA
P3	VOUT_LNLDO2	O	1.25V output for LNLDO2, 80 mA. It can be programmed to output 2.5V after reset (LNLDO2 is OFF by default. Software can program it to 1.25V or 2.5V before enabling it).
M3	VIN_LNLDO1	I	1.5V input for LNLDO1, 130 mA. ***Note:*** If LNLDO1 is not used, this pin **must** be connected to ground.
N1	VIN_LNLDO2	I	3.3V or 1.5V input (which could be the output of CBUCK), 80 mA current. ***Note:*** If LNLDO2 is not used, this pin **must** be connected to ground.
L1	VOUT_CLDO	O	1.25V output for CLDO, 200 mA
M2	VIN_CLDO	I	1.5V input for CLDO, 200 mA. ***Note:*** If CLDO is not used, this pin **must** be connected to ground.

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Integrated Switching Regulators			
G1	SR_VOUTBB	O	Buck Boost Regulator. 3.3V output
C1	SR_VNLDO	O	NLDO Output. 220 nF external compensating capacitor
F1	SR_VLX2BB	O	Buck Boost Regulator. Inductor –ve terminal
E1	SR_VLX1BB	O	Buck Boost Regulator. Inductor +ve terminal
A3	SR_VLX1	O	Core Buck Regulator. Output to inductor
D1	SR_VFBBB	I	Buck Boost Regulator. Voltage feedback. ***Note:*** If not used, this pin should be connected to ground.
A1	SR_VFB1	I	Core Buck Regulator. Output voltage feedback. ***Note:*** This pin should be connected to ground if CBUCK is not used.
E2	SR_VBATBB	I	Buck Boost Regulator. Battery voltage Input. ***Note:*** This pin **must** be connected to VBAT (or an external 3.3V supply even if the BBOOST and CBUCK regulators are not used.
A2	SR_VBAT1B	I	Clean VBAT supply for LDOs and Bandgap. ***Note:*** This pin **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
B3	SR_VBAT1A	I	Core Buck Regulator. Battery voltage input. ***Note:*** This pin **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
C2	SR_TESTSWG	I/O	Connect to 2.5V VDD (which could be SR_AVDD2P5) with or without 0Ω stuffing option.
F2	SR_PVSSB	I	Buck Boost Regulator. Power Switch Ground
C3	SR_PVSS	I	Core Buck Regulator. Power Switch Ground
D3	SR_AVSS	I	Analog Ground
B2	SR_PLDO	O	PLDO Output. 220 nF external compensating capacitor
B1	SR_AVDD2P5	O	2.5V LDO Output
N3	AVDD2P5_LDO	I	2.5V Supply for Internal LDO. Connect to SR_AVDD2P5
SDIO Bus Interface			
K4	SDIO_CMD	I/O	SDIO Command Line. See Table 18 on page 73 and Table 19 on page 74 for additional details.
L2	SDIO_DATA_0	I/O	SDIO Data Line 0. See Table 18 on page 73 and Table 19 on page 74 for additional details.
H2	SDIO_DATA_1	I/O	SDIO Data Line 1. See Table 18 on page 73 and Table 19 on page 74 for additional details.
J3	SDIO_DATA_2	I/O	SDIO Data Line 2. See Table 18 on page 73 and Table 19 on page 74 for additional details.
P6	SDIO_DATA_3	I/O	SDIO Data Line 3. See Table 18 on page 73 and Table 19 on page 74 for additional details.
K1	SDIO_CLK	I	SDIO Clock. This is an input pin driven by the SDIO clock signal. It remains high impedance when WL_RST_N is low. See Table 18 on page 73 and Table 19 on page 74 for additional details.

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
WLAN UART			
J4	WL_UART_TX0	I/O	Serial output for WLAN UART. Connect to RS-232 DTE for exchanging data with other serial devices. If not used, it may be left unconnected.
H3	WL_UART_RX0	I/O	Serial Input for WLAN UART. Connect to RS-232 DTE for exchanging data with other serial devices. If not used, it may be left unconnected.
JTAG Interface (test only)			
D4	TMS	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left unconnected (NC) as it has an internal pull-up resistor.
C4	TDO	O	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left NC.
E5	TDI	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left NC, as it has an internal pull-up resistor.
F5	TCK	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left NC, as it has an internal pull-up resistor.
E6	TAP_SEL	I	WLAN JTAG Tap Select. Drive low to connect the JTAG interface with the main tap controller; drive high to connect with the ARM tap controller. This pin has an internal pull-down. For normal operation, the pin can be left as a NC.
B4	JTAG_TRST_N	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left NC, as it has an internal pull-up resistor.
SPROM			
H1	SPROM_DOUT	I/O	SPROM Data Out. Must be connected to DIN signal of the SPROM.
H8	SPROM_DIN	I/O	SPROM Data In. Must be connected to DOUT signal of the SPROM.
J6	SPROM_CS	I/O	SPROM Chip Select. Must be connected to the chip select input of the SPROM (typically called CS). This pin has an internal pull-down.
K3	SPROM_CLK	I/O	SPROM Data Clock. Must be connected to the serial clock input of the SPROM (typically called SK).

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
RF Control Lines			
A7	RF_SW_CTRL_N_0	I/O	RF Switch Control Line. Connect to the BT TX port of the front-end switch.
B6	RF_SW_CTRL_N_1	I/O	RF Switch Control Line. Connect to the WLAN TX port of the front-end switch.
A5	RF_SW_CTRL_N_3	I/O	Programmable RF switch control line
B7	RF_SW_CTRL_P_0	I/O	RF Switch Control Line. Connect to the RX port (for both WLAN and BT) of the front-end switch.
E7	RF_SW_CTRL_P_1	I/O	Programmable RF switch control line
B5	RF_SW_CTRL_P_3	I/O	Programmable RF switch control line
A6	AMODE_TX_PU	I/O	802.11a external PA control
F6	AMODE_RX_PU	I/O	802.11a external LNA power supply control
B8	GMODE_TX_PU	I/O	802.11g external PA control
C7	WRF_AFE_DIGIT_TEST1	I/O	BT/WLAN external LNA power up control
D6	GMODE_EXT_LNA_GAIN	I/O	BT/WLAN external LNA gain control
WLAN GPIO			
G5	WL_GPIO_0	I/O	WLAN general purpose interface pins. These pins ae high impedance on power up and reset. Subsequently, they become an input or output under software control. These pins have a programmable pull-up/down. See Table 18 on page 73 and Table 19 on page 74 for additional details.
G3	WL_GPIO_1		
J2	WL_GPIO_2		
G2	WL_GPIO_6		
J5	WL_GPIO_7		
FM Receiver			
P11	FM_RXP	I	FM radio RF antenna port
P12	FM_RXN	I	FM radio RF antenna port
M11	FM_CVAR	I	Bypass node for FM VCO
M9	FM_AUDIO_OUT2	O	FM analog audio output channel 2
M7	FM_AUDIO_OUT1	O	FM analog audio output channel 1
External Coexistence			
H7	ERCX_TX_FREQ	I	Transmit frequency overlap signal from the external radio. Used to indicate that the external radio is about to transmit on a restricted channel defined by the coexistence mechanism.
F3	ERCX_STATUS	I	Coexistence Status from external radio. Used to signal external radio priority status and receive/transmit direction.
G4	ERCX_RF_ACTIVE	I	Indicates external radio is active. This pin is asserted prior to an external radio transaction and remains active for the duration of the transaction.

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Bluetooth UART			
P4	BT_UART_TXD	O	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
L7	BT_UART_RXD	I	Bluetooth UART Series Input. Serial data input for the HCI UART Interface.
N6	BT_UART_RTS_N	O	Bluetooth UART Request to Send. Active-low request to send signal for the HCI UART interface.
P5	BT_UART_CTS_N	I	Bluetooth UART Clear to Send. Active-low clear to send signal for the HCI UART interface.
Bluetooth Test Mode			
N8	BT_TM0	I	TM0 and TM1 are used for XTAL_PU polarity. Valid settings are TM[1:0] = 00 for high assertion and 01 for low assertion. See XTAL_PU signal description for more details.
K9	BT_TM1	I	
L8	BT_TM2	I	Bluetooth test mode pin
J8	BT_TM6	I	TM6 is pulled low for the 52-MHz Xtal or TCXO clock and pulled high for all other frequencies.
Bluetooth			
L4	BT_SDA	I/O	Bluetooth BSC data
N5	BT_SCL	I/O	Bluetooth BSC clock
N9	BT_RST_N	I	Low asserting reset for Bluetooth core. This pin **must** be driven high or low (not left floating). This pin needs 100 ms delay from BT_REG_ON or WL_REG_ON while the BCM4325 is powered up. See Section 22: "Power-Up Sequence and Timing" for more details.
K14	BT_RFIOP	O	RF I/O Tuning Port. For Class 2 operation, connect directly to ground. Trace lengths from the ball to ground must be kept short (parasitic inductance < 0.5 nH). If trace lengths need to be longer due to board constraints, add 1.8 pF capacitor to GND. For Class 1 operation, connect to external PA input.
J14	BT_RFION	O	RF I/O Antenna Port. For Class 2 operation, connect to antenna or BPF. For Class 1 operation, connect to T/R switch Receive pin.
E3	BT_REG_ON	I	Used by PMU (along with WL_REG_ON) to decide whether or not to power down internal BCM4325 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. BT_REG_ON needs about 70 µs delay (approx. two 32 kHz clock cycles) after VBAT and VDDIO is up. See Section 22: "Power-Up Sequence and Timing" for details.
Bluetooth PCM			
M5	BT_PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input)
L5	BT_PCM_OUT	I/O	PCM data output
K5	BT_PCM_IN	I/O	PCM data input
J7	BT_PCM_CLK	I/O	PCM clock, can be master (output) or slave (input)

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Bluetooth GPIO			
J9	BT_GPIO_0	I/O	Bluetooth general purpose interface pins. These pins are high-impedance on power up and reset. Subsequently, they become an input or output through software control. See Table 15 on page 68 and Table 17 on page 71 for more information.
H9	BT_GPIO_1		
K10	BT_GPIO_2		
M6	BT_GPIO_3		
K6	BT_GPIO_4		
K7	BT_GPIO_5		
L6	BT_GPIO_6		
K8	BT_GPIO_7		
Miscellaneous			
D2	WL_REG_ON	I	This signal is used by PMU (along with BT_REG_ON) to decide whether or not to power down the internal BCM4325 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. Also note that if WL_RST_N is low (regardless of BT_RST_N state), the WLAN core will be powered off. WL_REG_ON needs about 70 µs delay (approx. two 32 kHz clock cycles) after VBAT and VDDIO is up. See Section 22: "Power-Up Sequence and Timing" for more details.
A4	WL_RST_N	I	Low Asserting Reset for WLAN Core. This pin **must** be driven high or low (not left floating). See Section 22: "Power-Up Sequence and Timing" for more details.
P8	OSCIN	I	XTAL oscillator input
P9	OSCOUT	O	XTAL oscillator output
K2	XTAL_PU	O	The BCM4325 asserts this signal when it wants the host to turn on the crystal circuit/reference clock (e.g., TCXO). The XTAL_PU assertion polarity is programmable based on BT_TM0 and BT_TM1. If BT_TM0 and BT_TM1 connect to ground, XTAL_PU is high asserting (i.e., the BCM4325 drives XTAL_PU high when it wants the clock turned on). If TM0 connects to VDDIO and BT_TM1 connects to ground, XTAL_PU is low asserting.
Bluetooth Supplies			
M13	BT_VDDVCO	I	1.25V Bluetooth VCO power supply
L14	BT_VDDTF	I	Bluetooth internal PA power supply. For Class3 Pout < 0 dBm: Connect it to 1.25V. For Class2 0 dBm < Pout<3 dBm: Connect it to 1.5V. For Class1 Pout > 3 dBm: Connect it to 2.5V.
K12	BT_VDDRF	I	1.25V Bluetooth RF power supply
P14	BT_VDDPLL	I	1.25V Bluetooth PLL power supply
G8 N2	BT_VDDO	I	Bluetooth digital I/O supply (1.8V to 3.3V)
L13	BT_VDDIFIFP	I	1.25V Bluetooth IF and IF PLL power supply
J11 N4	BT_VDDC	I	1.25V Bluetooth baseband core supply

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
WLAN Supplies			
H12	WRF_VDDVCO_1P2	I	1.25V supply for WLAN PLL
D12	WRF_VDDTX_1P2	I	1.25V supply for WLAN transmitters
E13	WRF_VDDRX_1P2	I	1.25V supply tor WLAN receivers
H13	WRF_VDDPFDCP_1P2	I	1.25V supply for WLAN PLL
A11	WRF_VDDPAG_3P3	I	3.3V for the internal power amplifiers
B13	WRF_VDDPAA_3P3	I	3.3V for the internal power amplifiers
G12	WRF_VDDLO_1P2	I	1.25V supply for WLAN LO generator
J12	WRF_VDDD_1P2	I	1.25V supply for WLAN PLL
J13	WRF_VDDCAB_1P2	I	1.25V supply for WLAN CAB
K11	WRF_VDDA_1P2	I	1.25V supply for WLAN PLL
E10	WRF_BBPLL_VDD_1P2	I	1.25V supply for WLAN Baseband PLL
D7	WRF_AFE_AVDD_TXDAC	I	1.25V supply for DAC
B9	WRF_AFE_AVDD_RXADC	I	1.25V supply for ADC
D10	WRF_AFE_AVDD_AUX	I	1.25V supply for AUX ADC
Miscellaneous Supplies			
J1 L3	VDDIO_SD	I	SDIO I/O supply (1.8V to 3.3V)
C6 F10	VDDIO_RF	I	RF I/O supply (1.8V to 3.3V)
F9	VDDIO_RF	I	RF I/O supply (1.8V to 3.3V)
H6 F4 G6	VDDIO	I	Digital I/O supply (1.8V to 3.3V)
G9 H10 H4	VDDC	I	1.25V digital supply for core
L10	VDD_XTAL	I	1.25V XTAL Power Supply
H5	OTP_VDD25	I	2.5V OTP Power Supply
FM Receiver Supplies			
M8	FM_ADVDD	I	1.25V FM supply
M10	FM_VDDVCO	I	1.25V FM receiver VCO power supply
P10	FM_VDDRF	I	1.25V FM receiver RF power supply
N10	FM_VDDPLL	I	1.25V FM receiver PLL power supply
P13	FM_VDDIF	I	1.25V FM receiver IF block power supply

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
Ground			
E4	VSS	I	Ground
E8			
F8			
G7			
L9	FM_ADVSS	I	Ground
K13	BTFM_VSS	I	Ground
M12			
M14			
N11			
N14			
J10	BT_VSSC_0	I	Ground
M4			
P2	AVSS1_LDO	I	Ground
A13	AVSS	I	Ground
B11			
B12			
B14			
C11			
C12			
C13			
C14			
D13			
F12			
G13			
H14			
G10			
D5	LV_TESTMODE	I	Connect to Ground
C5	TEST_SE	I	Scan enable input. Connect to Ground

Table 8: 196-Ball FBGA Signal Descriptions (Cont.)

Ball Number	Signal Name	Type	Description
No Connect			
H11	WRF_GPIO_OUT2	O	No Connect
G11	WRF_GPIO_OUT1	O	No Connect
F13	WRF_PA_100UA	O	No Connect
E11	WRF_AFE_TEST_QP	I	No Connect
F11	WRF_AFE_TEST_QN	I	No Connect
D9	WRF_AFE_TEST_OPQ	O	No Connect
C8	WRF_AFE_TEST_OPI	O	No Connect
D8	WRF_AFE_TEST_ONQ	O	No Connect
C9	WRF_AFE_TEST_ONI	O	No Connect
D11	WRF_AFE_TEST_IP	I	No Connect
B10	WRF_AFE_TEST_IN	I	No Connect
E12	WRF_AFE_IQADC_VREF	O	No Connect
F7	GMODE_RX_PU	I/O	No connect
P7	BT_COEX_OUT1	I/O	No Connect
N7	BT_COEX_OUT0	I/O	No Connect
N12	N/C	O	No Connect
N13	N/C	O	No Connect

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Table 9: 339-Pin WLCSP Signal Descriptions

Pin #	Signal Name	Type	Description
WLAN RF			
14	WRF_GNDPAA_3P3	I	Internal power amplifier ground
16	WRF_GNDPAA_3P3	I	Internal power amplifier ground
17	WRF_GNDPAG_3P3	I	Internal power amplifier ground
18	WRF_GNDPAG_3P3	I	Internal power amplifier ground
15	WRF_GNDTX_1P2	I	Radio transmitter ground
2	WRF_RFOUTN_A	O	A-band PA transformer primary side ground (need short and solid ground).
5	WRF_RFOUTP_A	O	WLAN 802.11a Internal Power Amplifier output (50Ω)
6	WRF_RFOUTN_G	O	G-band PA transformer primary side ground (need short and solid ground).
9	WRF_RFOUTP_G	O	WLAN 802.11g Internal Power Amplifier output (50Ω)
10	WRF_AFE_PAD_AVSS_RXADC	I	ADC Ground
12	WRF_AFE_PAD_AVSS_TXDAC	I	DAC Ground
23	WRF_AFE_TSSI_A	I	Transmit signal strength indicator for external 802.11a Power Amplifier
26	WRF_RFINN_A2_XFMR	O	Ground of the primary side of the A-band RX transformer #2. Need short and solid ground
30	WRF_AFE_TSSI_G	I	Transmit signal strength indicator for external 802.11g Power Amplifier
31	WRF_RFINP_A2	I	WLAN 802.11a Internal LNA #2 RX input (50Ω)
32	WRF_EXTCOUPLE_AIN	I	WLAN directional coupler input for 802.11a (50Ω)
36	WRF_RFINP_A1	I	WLAN 802.11a Internal LNA RX Positive input (100Ω)
37	WRF_EXTCOUPLE_GIN	I	WLAN directional coupler input for 802.11g (50Ω)
38	WRF_BBPLL_GND_1P2	I	WLAN Baseband PLL Ground
39	WRF_GNDLO_1P2	I	WLAN LO Generator Ground
40	WRF_RFINN_A1_XFMR	I	WLAN 802.11a Internal LNA RX Negative input (100Ω)
42	WRF_GNDRX_1P2	I	WLAN RX Ground
46	WRF_RFINN_G2_XFMR	O	Ground of the primary side of the G-band RX transformer #2. Need short and solid ground
48	WRF_RFINP_G2	I	WLAN 802.11g Internal LNA #2 RX input (50Ω)
49	WRF_RFINP_G1	I	WLAN 802.11g and BT Shared LNA RX input (50Ω)
51	WRF_GNDVCO_1P2	I	WLAN PLL Ground
52	WRF_RFINN_G1_XFMR	O	Ground of the primary side of the Shared RX transformer. Need short and solid ground
53	WRF_GNDD_1P2	I	WLAN PLL Ground
55	WRF_GNDPFDCP_1P2	I	WLAN PLL Ground
57	WRF_GNDA_1P2	I	WLAN PLL Ground
60	WRF_GNDCAB_1P2	I	WLAN CAB Ground
61	WRF_EXTREFIN	I	32.768 kHz LPO clock input. Used for low-power mode timing. This pin needs be driven high or low (not left floating).
62	WRF_RES_EXT	I	Connect ~~to~~ external 15 kΩ (1% tolerance) resistor to ground.
180	WRF_DISABLE_N	I	Disables WLAN radio when low
178	WL_RST_N	I	Low asserting reset for WLAN core. This pin **must** be driven high or low (not left floating). See Section 22: “Power-Up Sequence and Timing”.

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
Integrated LDOs			
145 146	VIN_CLDO	I	1.5V input for CLDO, 200 mA ***Note:*** If CLDO is not used, these pins **must** be connected to ground.
147 148	VOUT_CLDO	O	1.25V output for CLDO, 200 mA
149 150	VIN_LNLDO1	I	1.5V input for LNLDO1, 130 mA ***Note:*** If LNLDO1 is not used, these pins **must** be connected to ground.
155	VIN_LNLDO2	I	3.3V or 1.5V input (which could be the output of CBUCK), 80 mA current. ***Note:*** If LNLDO2 is not used, this pin **must** be connected to ground.
158	VIN_LNLDO4	I	1.5V/3.3V Programmable input for LNLDO4 ***Note:*** If LNLDO4 is not used, this pin **must** be connected to ground.
151 152	VOUT_LNLDO1	O	1.25V output for LNLDO1, 130 mA
156	VOUT_LNLDO2	O	1.25V output for LNLDO2, 80 mA. It can be programmed to output 2.5V after reset (LNLDO2 is off by default. Software can program it to 1.25V or 2.5V before enabling it).
159	VOUT_LNLDO4	O	1.25V/2.5V programmable output for LNLDO4, 80 mA
160	AVDD2P5_LDO	I	2.5V supply for internal LDO. Connect to SR_AVDD2P5
162	VREF_LDO	O	Vref bypass. Connect to external capacitor.
153	AVSS1_LDO	I	Ground
161	AVSS2_LDO	I	Ground for band-gap reference
Integrated Switching Regulators			
101 108	SR_VLX1	O	Core buck regulator: Output to inductor
113	SR_VLX1	O	Core buck regulator: Output to inductor
100 107	SR_VBAT1A	I	Core buck regulator: Shared battery voltage input ***Note:*** These pins **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
102	SR_PVSS1	I	Core buck regulator: Power switch ground
103	SR_VFB1	I	Core buck regulator: Output voltage feedback ***Note:*** This pin should be connected to ground if CBUCK is not used.
104	SR_VBAT1B	I	Clean VBAT supply for LDOs and Bandgap ***Note:*** This pin **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
109	SR_PVSS1	I	Core buck regulator: Power switch ground
110	SR_VSSPLDO	I	Tracks battery voltage: Connect to 220 nF external capacitor to battery
112	SR_VBAT1A	I	Core buck regulator: Shared battery voltage input ***Note:*** This pin **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
114	SR_PVSS1	I	Core buck regulator: Power switch ground
115	SR_TESTSWG	I/O	Connect to 2.5V VDD (which could be SR_AVDD2P5) with or without 0Ω stuffing option.
116	SR_AVDD2P5	O	2.5V LDO output
117	SR_AVSS	I	Analog Ground

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
118	SR_VBAT1A	I	Core buck regulator: Shared battery voltage input ***Note:*** This pin **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
119	SR_AVSS	I	Analog Ground
120	SR_VDDNLDO	O	NLDO output: Connect to 220 nF external to capacitor to ground
122 123	SR_VBATBB	I	Buck boost regulator: Battery voltage Input ***Note:*** These pins **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
124	SR_VFBBB	I	Buck boost regulator: Voltage feedback ***Note:*** This pin should be connected to ground if BBOOST is not used.
126 127 128	SR_VBATBB	I	Buck boost regulator: Battery voltage input ***Note:*** These pins **must** be connected to VBAT (or an external 3.3V supply) even if the BBOOST and CBUCK regulators are not used.
129 130 131 132	SR_VLX1BB	O	Buck boost regulator: Inductor +ve terminal
133 134 135 136	SR_PVSSB	I	Buck boost regulator: Power switch ground
137 138 139 140	SR_VLX2BB	O	Buck boost regulator: Inductor –ve terminal
141 142 143 144	SR_VOUTBB	O	Buck boost regulator: 3.3V output
SDIO Bus Interface			
284	SDIO_DATA_0	I/O	SDIO Data Line 0. See Table 18 on page 73 and Table 19 on page 74 for more information.
272	SDIO_DATA_1	I/O	SDIO Data Line 1. See Table 18 on page 73 and Table 19 on page 74 for more information.
271	SDIO_DATA_2	I/O	SDIO Data Line 2. See Table 18 on page 73 and Table 19 on page 74 for more information.
270	SDIO_DATA_3	I/O	SDIO Data Line 3. See Table 18 on page 73 and Table 19 on page 74 for more information.
281	SDIO_CMD	I/O	SDIO Command Line. See Table 18 on page 73 and Table 19 on page 74 for more information.
285	SDIO_CLK	I	SDIO Clock. See Table 18 on page 73 and Table 19 on page 74 for more information.

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
WLAN UART			
247	WL_UART_RX0	I	Serial Input for WLAN UART. Connect to RS-232 DTE for exchanging data with other serial devices. If not used it may be left unconnected.
259	WL_UART_TX0	I/O	Serial Output for WLAN UART. Connect to RS-232 DTE for exchanging data with other serial devices. If not used it may be left unconnected.
260	WL_UART_TX1	I/O	Serial Output for second WLAN UART. Connect to RS-232 DTE for exchanging data with other serial devices. If not used it may be left unconnected.
275	WL_UART_RX1	I	Serial Input for second WLAN UART. Connect to RS-232 DTE for exchanging data with other serial devices. If not used it may be left unconnected.
JTAG Interface (test only)			
190	TDI	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left unconnected (NC) as they have internal pull-up resistors.
171	TDO	O	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, this pin can be left NC.
191	TMS	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left NC as they have internal pull-up resistors.
184	TCK	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left NC as they have internal pull-up resistors.
172	JTAG_TRST_N	I	For normal operation, connect as described in the JTAG specification (IEEE Std 1149.1). Otherwise, if JTAG is not used, these pins can be left NC as they have internal pull-up resistors.
177	TAP_SEL	I	WLAN JTAG tap select: Drive low to connect the JTAG interface with the main tap controller; drive high to connect with the ARM tap controller. This pin has an internal pull-down. For normal operation the pin can be left as NC.
SPROM			
233	SPROM_DIN	I	SPROM Data In. Must be connected to DOUT signal of the SPROM.
246	SPROM_CS	I/O	SPROM Chip Select. Must be connected to the chip select input of the SPROM (typically called CS). This pin has an internal pull-down.
286	SPROM_CLK	I/O	SPROM Data Clock. Must be connected to the serial clock input of the SPROM (typically called SK).
287	SPROM_DOUT	I/O	SPROM Data Out. Must be connected to DIN signal of the SPROM.
SFLASH			
206	SFLASH_Q	I	Data input from serial flash (active low)
214	SFLASH_D	O	Output data to serial flash
228	SFLASH_C	O	Serial flash clock
229	SFLASH_S	O	Serial flash chip select (active low)

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
RF Control Lines			
168	RF_SW_CTRL_P_0	O	RF Switch Control Line. Connect to the RX port (for both WLAN and BT) of the front-end switch.
181	RF_SW_CTRL_P_1	O	Programmable RF switch control line
170	RF_SW_CTRL_P_2	O	Programmable RF switch control line
197	RF_SW_CTRL_P_3	O	Programmable RF switch control line
164	RF_SW_CTRL_N_0	O	RF switch control line. Connect to the BT TX port of the front-end switch.
174	RF_SW_CTRL_N_1	O	RF switch control line. Connect to the WLAN TX port of the front-end switch.
176	RF_SW_CTRL_N_2	O	Programmable RF switch control line
189	RF_SW_CTRL_N_3	O	Programmable RF switch control line
169	WRF_AFE_DIGIT_TEST1	I/O	BT/WLAN external LNA power up control
182	AMODE_TX_PU	O	802.11a external PA control
196	AMODE_RX_PU	O	802.11a external LNA power supply control
188	AMODE_EXT_LNA_GAIN	O	802.11a external LNA gain control
187	GMODE_TX_PU	O	802.11g external PA control
175	GMODE_EXT_LNA_GAIN	O	BT/WLAN external LNA gain control
WLAN GPIO			
213	WL_GPIO_0	I/O	WLAN general purpose interface pins. These pins are high impedance on power up and reset. Subsequently, they become an input or output under software control. Each pin has a programmable pull-up/down, see Table 14 on page 67 and Table 18 on page 73 for more information.
240	WL_GPIO_1		
239	WL_GPIO_2		
238	WL_GPIO_4		
237	WL_GPIO_5		
251	WL_GPIO_6		
225	WL_GPIO_7		
250	WL_GPIO_8		
236	WL_GPIO_9		
249	WL_GPIO_10		
262	WL_GPIO_11		
248	WL_GPIO_12		
224	WL_GPIO_13		
235	WL_GPIO_14		
261	WL_GPIO_15		

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
FM Receiver			
76	FM_AUDIO_OUT1	O	FM analog audio output channel 1
75	FM_AUDIO_OUT2	O	FM analog audio output channel 2
83	FM_CVAR	I	Bypass node for FM VCO
90	FM_RXN	I	FM radio RF antenna port
91	FM_RXP	I	FM radio RF antenna port
External Coexistence			
199	ERCX_PRISEL	O	External Radio Coexistence. Priority Select.
207	ERCX_STATUS	I	Coexistence status from external radio. Used to signal external radio priority status and receive/transmit direction.
215	ERCX_RF_ACTIVE	I	Indicates external radio is active. This pin is asserted prior to an external radio transaction and remains active for the duration of the transaction.
219	ERCX_TX_FREQ	I	Transmit frequency overlap signal from the external radio. Used to indicate that the external radio is about to transmit on a restricted channel defined by the coexistence mechanism.
230	ERCX_TXCONF	O	External Radio Coexistence. Transmit Confirmation.
Bluetooth UART			
269	BT_UART_RXD	I	Bluetooth UART Serial Input. Serial data input for the HCI UART Interface.
321	BT_UART_TXD	O	Bluetooth UART Serial Output. Serial data output for the HCI UART Interface.
342	BT_UART_CTS_N	I	Bluetooth UART Clear to Send. Active-low clear to send signal for the HCI UART interface.
291	BT_UART_RTS_N	O	Bluetooth UART Request to Send. Active-low request to send signal for the HCI UART interface.
Bluetooth Test Mode			
309	BT_TM0	I	M0 and TM1 are used for XTAL_PU polarity. Valid settings are TM[1:0] = 00 for high assertion; and 01 for low assertion. See XTAL_PU signal description for more details.
288	BT_TM1	I	
316	BT_TM2	I	Bluetooth test mode pin
325	BT_TM6	I	TM6 is pulled low for the 52 MHz Xtal or TCXO clock and pulled high for all other frequencies.
Bluetooth			
63	BT_RFION	O	RF I/O antenna port. For Class 2 operation, connect to antenna or BPF.
66	BT_RFIOP	O	RF I/O tuning port. For Class 2 operation, connect directly to ground. Trace lengths from the ball to ground must be kept short (parasitic inductance < 0.5 nH). If trace lengths need to be longer due to board constraints, add a 0.9pF capacitor to GND.
97	BT_RST_N	I	Low asserting reset for Bluetooth core. This pin needs be driven high or low (not left floating). This pin needs 100 ms delay from BT_REG_ON or WL_REG_ON while BCM4325 is powered up. See Section 22: "Power-Up Sequence and Timing" for more details.
336	BT_SCL	I/O	Bluetooth BSC Clock
303	BT_SDA	I/O	Bluetooth BSC Data
308	BT_XCS_N	O	Active low chip select for external code space in Flash memory

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
276	BT_XOE_N	O	Active low output enable output for dataspace
324	BT_XWE_N	O	Active low write enable output for dataspace
299	BT_XA_1	O	Address bit 1 for Bluetooth Flash ROM/External SRAM
317	BT_XA_2	O	Address bit 2 for Bluetooth Flash ROM/External SRAM
289	BT_XA_3	O	Address bit 3 for Bluetooth Flash ROM/External SRAM
332	BT_XA_4	O	Address bit 4 for Bluetooth Flash ROM/External SRAM
310	BT_XA_5	O	Address bit 5 for Bluetooth Flash ROM/External SRAM
326	BT_XA_6	O	Address bit 6 for Bluetooth Flash ROM/External SRAM
278	BT_XA_7	O	Address bit 7 for Bluetooth Flash ROM/External SRAM
290	BT_XA_8	O	Address bit 8 for Bluetooth Flash ROM/External SRAM
311	BT_XA_9	O	Address bit 9 for Bluetooth Flash ROM/External SRAM
327	BT_XA_10	O	Address bit 10 for Bluetooth Flash ROM/External SRAM
334	BT_XA_11	O	Address bit 11 for Bluetooth Flash ROM/External SRAM
301	BT_XA_12	O	Address bit 12 for Bluetooth Flash ROM/External SRAM
312	BT_XA_13	O	Address bit 13 for Bluetooth Flash ROM/External SRAM
335	BT_XA_14	O	Address bit 14 for Bluetooth Flash ROM/External SRAM
279	BT_XA_15	O	Address bit 15 for Bluetooth Flash ROM/External SRAM
329	BT_XA_16	O	Address bit 16 for Bluetooth Flash ROM/External SRAM
265	BT_XA_17	O	Address bit 17 for Bluetooth Flash ROM/External SRAM
263	BT_XA_18	O	Address bit 18 for Bluetooth Flash ROM/External SRAM
343	BT_XD_0	I/O	Bidirectional data bus bit 0 for Flash ROM
313	BT_XD_1	I/O	Bidirectional data bus bit 1 for Flash ROM
292	BT_XD_2	I/O	Bidirectional data bus bit 2 for Flash ROM
280	BT_XD_3	I/O	Bidirectional data bus bit 3 for Flash ROM
293	BT_XD_4	I/O	Bidirectional data bus bit 4 for Flash ROM
344	BT_XD_5	I/O	Bidirectional data bus bit 5 for Flash ROM
337	BT_XD_6	I/O	Bidirectional data bus bit 6 for Flash ROM
314	BT_XD_7	I/O	Bidirectional data bus bit 7 for Flash ROM
304	BT_XD_8	I/O	Bidirectional data bus bit 8 for Flash ROM
294	BT_XD_9	I/O	Bidirectional data bus bit 9 for Flash ROM
305	BT_XD_10	I/O	Bidirectional data bus bit 10 for Flash ROM
345	BT_XD_11	I/O	Bidirectional data bus bit 11 for Flash ROM
331	BT_XD_12	I/O	Bidirectional data bus bit 12 for Flash ROM
315	BT_XD_13	I/O	Bidirectional data bus bit 13 for Flash ROM
346	BT_XD_14	I/O	Bidirectional data bus bit 14 for Flash ROM
347	BT_XD_15	I/O	Bidirectional data bus bit 15 for Flash ROM
322	BT_VSSC_0	I	Ground
323			

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
Bluetooth PCM			
268	BT_PCM_CLK	I/O	PCM clock, can be master (output) or slave (input).
302	BT_PCM_OUT	I/O	PCM data output
341	BT_PCM_IN	I/O	PCM data input
328	BT_PCM_SYNC	I/O	PCM sync signal, can be master (output) or slave (input).
Bluetooth GPIO			
264	BT_GPIO_0	I/O	Bluetooth general purpose interface pin.
252	BT_GPIO_1	I/O	These pins are high-impedance on power up and reset. Subsequently, they become an input or output through software control. See Table 15 on page 68 and Table 17 on page 71 for more information.
298	BT_GPIO_2	I/O	
319	BT_GPIO_3	I/O	
340	BT_GPIO_4	I/O	
333	BT_GPIO_5	I/O	
318	BT_GPIO_6	I/O	
339	BT_GPIO_7	I/O	
Miscellaneous			
95	OSCIN	I	XTAL oscillator input
96	OSCOUT	O	XTAL oscillator output
274	XTAL_PU	O	The BCM4325 asserts this signal when it wants the host to turn on the crystal circuit/ reference clock like TCXO. Note that the XTAL_PU assertion polarity is programmable based on BT_TM0 and BT_TM1. If BT_TM0 and BT_TM1 connect to ground, XTAL_PU is high asserting (i.e., the BCM4325 drives XTAL_PU high when it wants the clock turned on). If TM0 connects to VDDIO and BT_TM1 connects to ground, XTAL_PU is low asserting.
121	WL_REG_ON	I	Used by PMU (along with BT_REG_ON) to decide whether or not to power down internal BCM4325 regulators. If both BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. Also note that if WL_RST_N is low (regardless of BT_RST_N state) the WLAN core will be powered off. WL_REG_ON needs about 70 µs delay (approx. two 32-kHz clock cycles) after VBAT and VDDIO is up. See Section 22: “Power-Up Sequence and Timing”.
123	BT_REG_ON	I	Used by PMU (along with WL_REG_ON) to decide whether or not to power down internal BCM4325 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. BT_REG_ON needs about 70 µs delay (approx. two 32-kHz clock cycles) after VBAT and VDDIO is up. See Section 22: “Power-Up Sequence and Timing” for more details.

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
Bluetooth Supplies			
64	BT_VDDRF	I	1.25V Bluetooth RF power supply
68	BT_VDDTF	I	Bluetooth Internal PA power supply. For Class3 Pout < 0 dBm: Connect to 1.25V For Class2 0 dBm < Pout < 3 dBm: Connect to 1.5V For Class1 Pout > 3 dBm: Connect to 2.5V
70	BT_VDDIF	I	1.25V Bluetooth IF block power supply
73	BT_VDDVCO	I	1.25V Bluetooth VCO power supply
77	BT_VDDPLL	I	1.25V Bluetooth PLL power supply
231	BT_VDDO	I	Bluetooth Digital I/O supply (from 1.8V to 3.3V)
242 243	BT_VDDO	I	Bluetooth Digital I/O supply (1.8V to 3.3V)
266 267 320	BT_VDDC	I	1.25V Bluetooth baseband core supply
338	BT_VDDO	I	Bluetooth Digital I/O supply (1.8V to 3.3V)
330	BT_VDDC	I	1.25V Bluetooth baseband core supply
WLAN Supplies			
3 4	WRF_VDDPAA_3P3	I	3.3V for the internal power amplifiers
7 8	WRF_VDDPAG_3P3	I	3.3V for the internal power amplifiers
11	WRF_AFE_AVDD_RXADC	I	1.25V supply for ADC
13	WRF_AFE_AVDD_TXDAC	I	1.25V supply for DAC
27	WRF_VDDTX_1P2	I	1.25V supply for WLAN transmitters
29	WRF_AFE_AVDD_AUX	I	1.25V supply for AUX ADC
33	WRF_BBPLL_VDD_1P2	I	1.25V supply for WLAN baseband PLL
41	WRF_VDDRX_1P2	I	1.25V supply tor WLAN receivers
43	WRF_VDDLO_1P2	I	1.25V supply for WLAN LO generator
50	WRF_VDDVCO_1P2	I	1.25V supply for WLAN PLL
54	WRF_VDDD_1P2	I	1.25V supply for WLAN PLL
56	WRF_VDDPFDCP_1P2	I	1.25V supply for WLAN PLL
58	WRF_VDDA_1P2	I	1.25V supply for WLAN PLL
59	WRF_VDDCAB_1P2	I	1.25V supply for WLAN CAB
FM Receiver Supplies			
72	FM_ADVDD	I	1.25V FM supply
89	FM_VDDIF	I	1.25V FM receiver IF block power supply
92	FM_VDDRX	I	FM receiver power supply
93	FM_VDDVCO	I	1.25V FM receiver VCO power supply
94	FM_VDDPLL	I	1.25V FM receiver PLL power supply

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
Miscellaneous Supplies			
86	VDD_XTAL	I	1.25V XTAL power supply
200	VDD	I	1.25V digital supply
201			
202			
203			
217			
220			
221			
232			
211			
244			
306			
210	VDDIO	I	Digital I/O supply (1.8V to 3.3V)
216			
223			
226			
227			
257	VDDIO_SD	I	SDIO I/O supply (1.8V to 3.3V)
296			
297			
185	VDDIO_RF	I	RF I/O supply (1.8V to 3.3V)
165			
193			
194			
205			
198			
234	OTP_VDD25	I	2.5V OTP power supply
167	PACKAGEOPTION_1	I	Connect to VDDIO_RF (1.8V to 3.3V)

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
Ground			
65	BT_VSSRF	I	Bluetooth RF ground
67	BT_VSSPA	I	Bluetooth internal PA ground
69	BT_VSSIF	I	Bluetooth IF block ground
71	FM_ADVSS	I	Ground
74	FM_VSSVCO	I	FM receiver VCO ground
78	BT_VSSVCO	I	Bluetooth VCO ground
79	BT_VSSPLL	I	Bluetooth PLL ground
82	FM_VSSRX	I	FM receiver ground
84	FM_VSSPLL	I	FM receiver PLL ground
85	VSS_XTAL	I	XTAL ground
88	FM_VSSIF	I	FM IF block ground
98	SR_VFB2	I	Connect to ground
282	Ground	I	Connect to ground
204	VSS	I	Ground
245			
192			
179	PACKAGEOPTION_3	I	Connect to ground
173	PACKAGEOPTION_2	I	Connect to ground
208	VSS	I	Ground
209			
212			
218			
222			
253	BT_VSSC_0	I	Ground
254			
255			
256	VSS	I	Ground
241	BT_VSSC_0	I	Ground
163	PACKAGEOPTION_0	I	Connect to ground
183	LV_TESTMODE	I	Connect to ground
166	TEST_SE	I	Scan Enable Input. Connect to ground.

Table 9: 339-Pin WLCSP Signal Descriptions (Cont.)

Pin #	Signal Name	Type	Description
No Connect			
19	WRF_AFE_TEST_IN	I	No Connect
20	WRF_AFE_TEST_OPI	O	No Connect
21	WRF_AFE_TEST_ONQ	O	No Connect
22	WRF_AFE_TEST_IP	I	No Connect
24	WRF_AFE_TEST_ONI	O	No Connect
25	WRF_AFE_TEST_OPQ	O	No Connect
28	WRF_AFE_IQADC_VREF	O	No Connect
34	WRF_AFE_TEST_QP	I	No Connect
35	WRF_AFE_TEST_QN	I	No Connect
44	WRF_GPIO_OUT1	O	No Connect
45	WRF_GPIO_OUT2	O	No Connect
47	WRF_PA_100UA	O	No Connect
80	NO CONNECT (NC)	O	No Connect
81			
87	DUMMY_BUMP	N/A	No Connect
99	SR_VLX2	O	No Connect
106	SR_VLX2	O	No Connect
186	GMODE_RX_PU	O	No connect
273	WRF_AFE_DIGIT_TEST0	I/O	No Connect
195	WRF_AFE_DIGIT_TEST2	I/O	No Connect
300	BT_COEX_OUT1	I/O	No Connect
277	BT_COEX_OUT0	I/O	No Connect

PIN VOLTAGE DOMAINS

Table 10: BT_VDDO Domain (1.8V to 3.3V)

Signal	*FBGA Pin#*	*WLCSP Pin #*	*Type*
BT_REG_ON	E3	121	I
BT_GPIO_1	H9	252	I/O
BT_PCM_CLK	J7	268	I/O
BT_TM6	J8	325	I
BT_GPIO_0	J9	264	I/O
BT_GPIO_2	K10	298	I/O
BT_PCM_IN	K5	341	I/O
BT_GPIO_4	K6	340	I/O
BT_GPIO_5	K7	333	I/O
BT_GPIO_7	K8	339	I/O
BT_TM1	K9	288	I
BT_SDA	L4	303	I/O
BT_PCM_OUT	L5	302	I/O
BT_GPIO_6	L6	318	I/O
BT_TM0	N8	309	I
BT_TM2	L8	316	I
BT_PCM_SYNC	M5	328	I/O
BT_GPIO_3	M6	319	I/O
BT_SCL	N5	336	I/O
BT_UART_RTS_N	N6	291	I/O
BT_COEX_OUT0	N7	277	I/O
BT_UART_RXD	L7	269	I/O
BT_RST_N	N9	97	I
BT_UART_TXD	P4	321	I/O
BT_UART_CTS_N	P5	342	I/O
BT_COEX_OUT1	P7	300	I/O
BT_XCS_N	–	308	O
BT_XOE_N	–	276	O
BT_XWE_N	–	324	O
BT_XA[18:1]	–	Note	O
BT_XD[15:0]	–	Note	I/O

Note: For FBGA pin numbers see Table 8: “196-Ball FBGA Signal Descriptions,” on page 43.

Note: For WLCSP pin numbers, see Table 9: “339-Pin WLCSP Signal Descriptions,” on page 52.

Table 11: VDDIO Domain (1.8V to 3.3V)

Signal	*FBGA Pin#*	*WLCSP Pin#*	*Type*
WL_RST_N	A4	178	I
WL_REG_ON	D2	125	I
ERCX_STATUS	F3	207	I/O
WL_GPIO_6	G2	251	I/O
WL_GPIO_1	G3	240	I/O
ERCX_RF_ACTIVE	G4	215	I/O
WL_GPIO_0	G5	213	I/O
SPROM_DOUT	H1	287	I/O
WL_UART_RX0	H3	247	I/O
ERCX_TX_FREQ	H7	219	I/O
SPROM_DIN	H8	233	I/O
WL_GPIO_2	J2	239	I/O
WL_UART_TX0	J4	259	I/O
WL_GPIO_7	J5	225	I/O
SPROM_CS	J6	246	I/O
SPROM_CLK	K3	286	I/O
WRF_EXTREFIN	K12	61	I
XTAL_PU	K2	274	O
WL_UART_TX1	–	260	I/O
WL_UART_RX1	–	275	I
SFLASH_Q	–	206	I
SFLASH_D	–	214	O
SFLASH_C	–	228	O
SFLASH_S	–	229	O
WL_GPIO_4	–	238	I/O
WL_GPIO_5	–	237	I/O
WL_GPIO_8	–	250	I/O
WL_GPIO_9	–	236	I/O
WL_GPIO_10	–	249	I/O
WL_GPIO_11	–	262	I/O
WL_GPIO_12	–	248	I/O
WL_GPIO_13	–	224	I/O
WL_GPIO_14	–	235	I/O
WL_GPIO_15	–	261	I/O
ERCX_PRISEL	–	199	O
ERCX_TXCONF	–	230	O

Table 12: VDDIO_RF Domain (1.8V to 3.3V)

Signal	FBGA Pin#	WLCSP Pin#	Type
RF_SW_CTRL_N_3	A5	189	I/O
AMODE_TX_PU	A6	182	I/O
RF_SW_CTRL_N_0	A7	164	I/O
WRF_DISABLE_N	A8	180	I/O
JTAG_TRST_N	B4	172	I
RF_SW_CTRL_P_3	B5	197	I/O
RF_SW_CTRL_N_1	B6	174	I/O
RF_SW_CTRL_P_0	B7	168	I/O
GMODE_TX_PU	B8	187	I/O
TDO	C4	171	I/O
TEST_SE	C5	166	I
WRF_AFE_DIGIT_TEST1	C7	169	I/O
TMS	D4	191	I
LV_TESTMODE	D5	183	I
GMODE_EXT_LNA_GAIN	D6	175	I/O
TDI	E5	190	I
TAP_SEL	E6	177	I
RF_SW_CTRL_P_1	E7	181	I/O
TCK	F5	184	I
AMODE_RX_PU	F6	196	I/O
GMODE_RX_PU	F7	186	I/O
RF_SW_CTRL_P_2	–	170	O
RF_SW_CTRL_N_2	–	176	O
AMODE_EXT_LNA_GAIN	–	188	O

Table 13: VDDIO_SD Domain (1.8V to 3.3V)

Signal	FBGA Pin#	WLCSP Pin#	Type
SDIO_CMD	K4	281	I/O
SDIO_DATA_0	L2	284	I/O
SDIO_DATA_1	H2	272	I/O
SDIO_DATA_2	J3	271	I/O
SDIO_DATA_3	P6	270	I/O
SDIO_CLK	K1	285	I/O
WRF_AFE_DIGIT_TEST0	–	273	I/O

WLAN GPIO Signals and Strapping Options

The pins listed in Table 14 are sampled at Power-On Reset (POR) to determine the various operating modes. Sampling occurs within a few milliseconds following an internal POR or deassertion of the external POR. After POR, each pin assumes the GPIO or alternative function specified in the signal descriptions table. Each strapping option pin has an internal pull-up (PU) or pull-down (PD) resistor that determines the default mode.

To change the mode, connect an external PU resistor to VDDIO or a PD resistor to GND, using a 10 kΩ resistor or less.

Note: Refer to the reference board schematics for more information.

Table 14: WLAN GPIO Functions and Strapping Options

Pin Name	FBGA Pin #	WLCSP Pin #	Default	Function	Description
WL_GPIO_0	G5	213	–	GPIO	WL_GPIO[2:0] can be used to set out-of-band signals like WL_WAKE_N, WL_HOST_WAKE_N, and WL_STANDBY.
WL_GPIO_1	G3	240	–	GPIO	
WL_GPIO_2	J2	239	–	GPIO	
WL_GPIO_4	–	238	–	GPIO	
WL_GPIO_5	–	237	–	GPIO	
WL_GPIO_6	G2	251	High	GPIO[7:6][a]	[7:6] = 00: OTP powered ON, OTP source of Chip ID, CIS source: Default
WL_GPIO_7	J5	225	Low	–	[7:6] = 01: OTP powered ON, OTP source of Chip ID, CIS source: SROM
					[7:6] = 10: OTP powered ON, OTP source of Chip ID, CIS source: OTP
					[7:6] = 11: OTP powered OFF, default chip ID, CIS source: SROM
					[7:6] = ZZ: Same as 01: OTP powered, OTP source of Chip ID, CIS source SROM
WL_GPIO_8	–	250	High	Sets SDIO and ARM core status	0: SDIO in reset, ARM held in reset. Z: Same as 1: SDIO active and ARM in reset 1: SDIO active and ARM in reset
WL_GPIO_9	–	236	Low	Boot up status	[10:9] = 00: Default is set to boot from SRAM and ARM held in reset.
WL_GPIO_10	–	249	Low	–	[10:9] = 01: ARM running (out of reset), boot from ROM. [10:9] = 10: ARM running (out of reset), boot from flash. [10:9] = 11: invalid.
WL_GPIO_11	–	262	Low	Internal debug option	0: Pin must be kept at 0 or Z
WL_GPIO_12	–	248	Low	GPIO	–
WL_GPIO_13	–	224	Low	Sets clock that can be used for low power clock	0: External clock Z: Same as 0 1: Internal 32 kHz LPO clock (this is only available in the WLCSP package)

Table 14: WLAN GPIO Functions and Strapping Options (Cont.)

Pin Name	FBGA Pin #	WLCSP Pin #	Default	Function	Description
WL_GPIO_14	–	235	Low	Internal power up mode	[15:14] = 00: Chip powers up in the lowest power mode with all clock sources shut down except for the internal 32 kHz LPO clock that runs the PMU controller.
WL_GPIO_15	–	261	High	–	[15:14] = 01: Chip powers up to ILP request.
					[15:14] = 10: Chip powers up with the crystal oscillator turned on (default).
					[15:14] = 11: Chip powers up with PLL turned on by default.
					[15:14] = ZZ: Same as 10

a. These pins select the use of SPROM, OTP or the default CIS in the SDIO core.
b. WL_GPIO_3 does not exist.

BLUETOOTH GPIO SIGNALS

Table 15: BT GPIO Signals

Pin Name	FBGA Pin#	WLCSP Pin #	Type	Description
BT_GPIO_0	J9	264	I/O	Commonly set as BT_WAKEUP
BT_GPIO_1	H9	252	I/O	Commonly set as HOST_WAKEUP
BT_GPIO_2	K10	298	I/O	GPIO
BT_GPIO_3	M6	319	I/O	GPIO
BT_GPIO_4	K6	340	I/O	GPIO
BT_GPIO_5	K7	333	I/O	GPIO
BT_GPIO_6	L6	318	I/O	GPIO
BT_GPIO_7	K8	339	I/O	GPIO
BT_PCM_IN	K5	314	I	PCM data input
BT_PCM_OUT	L5	302	O	PCM data output
BT_PCM_SYNC	M5	328	I/O	PCM sync signal, can be master (output) or slave (input)
BT_PCM_CLK	J7	268	I/O	PCM clock, can be master (output) or slave (input)
BT_SCL	N5	336	I	BSC clock
BT_SDA	L4	303	I/O	BSC bidirectional data
BT_COEX_OUT0	N7	277	O	BT_ACTIVITY
BT_COEX_OUT1	P7	300	O	BT_PRIORITY_AND_STATUS

PIN DEFAULT PULL-UP/PULL-DOWN

Table 16: Pin Default Pull-Up/Pull-Down

Signal Name	*196-Ball FBGA Ball #*	*339-Pin WLCSP Pin #*	*Default Pin State*	*For No Connect*
RF_SW_CTRL_N_3	A5	189	No Pull Control	–
AMODE_TX_PU	A6	182	No Pull Control	–
RF_SW_CTRL_N_0	A7	164	No Pull Control	–
WRF_DISABLE_N	A8	180	High	IPU
JTAG_TRST_N	B4	172	High	IPU
RF_SW_CTRL_P_3	B5	197	No Pull Control	–
RF_SW_CTRL_N_1	B6	174	No Pull Control	–
RF_SW_CTRL_P_0	B7	168	No Pull Control	–
GMODE_TX_PU	B8	187	No Pull Control	–
SR_TESTSWG	C2	115	High	IPU
TDO	C4	171	No Pull Control	–
WRF_AFE_DIGIT_TEST1	C7	169	No Pull Control	–
TMS	D4	191	High	IPU
GMODE_EXT_LNA_GAIN	D6	175	No Pull Control	–
TDI	E5	190	High	IPU
TAP_SEL	E6	177	Low	IPD
RF_SW_CTRL_P_1	E7	181	No Pull Control	–
ERCX_STATUS	F3	207	No Pull Control	–
TCK	F5	184	High	IPU
AMODE_RX_PU	F6	196	No Pull Control	–
GMODE_RX_PU	F7	186	No Pull Control	–
WL_GPIO_6	G2	251	High	–
ERCX_RF_ACTIVE	G4	215	Low	IPD
SPROM_DOUT	H1	287	No Pull Control	–
WL_UART_RX0	H3	247	High	IPU
ERCX_TX_FREQ	H7	219	No Pull Control	–
SPROM_DIN	H8	233	No Pull Control	–
WL_UART_TX0	J4	259	No Pull Control	–
WL_GPIO_7	J5	225	Low	–
SPROM_CS	J6	246	Low	IPD
SDIO_CLK	K1	285	No Pull Control	–
SPROM_CLK	K3	286	No Pull Control	–
WL_UART_TX1	–	260	No Pull Control	–
WL_UART_RX1	–	275	High	IPU
SFLASH_Q	–	206	No Pull Control	–
SFLASH_C	–	228	No Pull Control	–
SFLASH_S	–	229	High	IPU
ERCX_TXCONF	–	230	No Pull Control	–
ERCX_PRISEL	–	199	No Pull Control	–

Table 16: Pin Default Pull-Up/Pull-Down (Cont.)

Signal Name	196-Ball FBGA Ball #	339-Pin WLCSP Pin #	Default Pin State	For No Connect
RF_SW_CTRL_P_2	–	170	No Pull Control	–
RF_SW_CTRL_N_2	–	176	No Pull Control	–
AMODE_EXT_LNA_GAIN	–	188	No Pull Control	–
PACKAGEOPTION_0	–	163	No Pull Control	–
PACKAGEOPTION_1	–	167	No Pull Control	–
PACKAGEOPTION_2	–	173	No Pull Control	–
PACKAGEOPTION_3	–	179	No Pull Control	–

Note: No Connect: Internal Pull Up/Down (IPU/IPD)

INTERFACE I/O STATUS

Table 17: BT/FM Interface I/O Status

Signal Name	I/O	On status	Low Power Status / Sleep (all supplies present)	REG_ON Held LOW (WL and BT RST_N held LOW) [a]	HW Default (REG_ON High, WL and BT_RST_N high; no SW loaded) [a]	Power rail	Internal Pull-Up Resistor Range (ohm)		Internal Pull-Down Resistor Range (ohm)		Comment
							3.3V	1.8V	3.3V	1.8V	
BT_GPIO_0, 1, 2, 3, 4, 6, 7	I/O	Programmable (In, Out, PD, PU)	Programmable (In, Out, PD, PU)	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	58K to 63K	58K to 63K	58K to 63K	58K to 63K	Internal pull-up/down are programmable and can be enabled/disabled by S/W.
BT_GPIO_5	I/O	Programmable (In, Out, PD, PU)	Programmable (In, Out, PD, PU)	No internal pull, disabled input	Output	BT_VDDO	58K to 63K	58K to 63K	58K to 63K	58K to 63K	Internal pull-up/down are programmable and can be enabled/disabled by S/W.
BT_UART_CTS	I	No internal pull	No internal pull, needs to be High Z	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	–	–	–	–	–
BT_UART_RTS	O	No internal pull	No internal pull, needs to be High Z	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	58K to 63K	58K to 63K	58K to 63K	58K to 63K	Pull-up required which can be internal or external. This can be programmed
BT_UART_RXD	I	No internal pull	No internal pull, needs to be driven low	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	–	–	–	–	–
BT_UART_TXD	O	No internal pull	No internal pull, needs to be High Z	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	58K to 63K	58K to 63K	58K to 63K	58K to 63K	Pull-up required which can be internal or external. This can be programmed
BT HOST_WAKE (BT_GPIO_0)	O	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	58K to 63K	58K to 63K	58K to 63K	58K to 63K	Pull-up required which can be internal or external. This can be programmed. Note: the level on HOST WAKE should be ignored by the host during power-up.
BT WAKE (BT_GPIO_1)	I	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	n/a	n/a	n/a	n/a	–
BT_PCM_CLK	I	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	n/a	n/a	n/a	n/a	–
BT_PCM_IN	I	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	n/a	n/a	n/a	n/a	–

Table 17: BT/FM Interface I/O Status (Cont.)

Signal Name	I/O	On status	Low Power Status / Sleep (all supplies present)	REG_ON Held LOW (WL and BT RST_N held LOW) [a]	HW Default (REG_ON High, WL and BT_RST_N high; no SW loaded) [a]	Power rail	Internal Pull-Up Resistor Range (ohm)		Internal Pull-Down Resistor Range (ohm)		Comment
							3.3V	1.8V	3.3V	1.8V	
BT_PCM_OUT	O	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	n/a	n/a	n/a	n/a	–
BT_PCM_SYNC	I	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	n/a	n/a	n/a	n/a	–
BT_SCL	I/O	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	n/a	n/a	n/a	n/a	–
BT_SDA	I/O	No internal pull	No internal pull	No internal pull, disabled input	No internal pull, disabled input	BT_VDDO	n/a	n/a	n/a	n/a	–
XTAL_PU	O	Programmable Default: BCM4325 drives to the asserted state when it needs the clock. Otherwise, the pin is pulled to the deasserted state. Polarity is set by the BT_TM0 pin	High-Z	Output Polarity set by the BT_TM0 pin.	VDDIO	58K to 63K	58K to 63K	58K to 63K	58K to 63K	–	

a. REG_ON Held LOW = Both WL_REG_ON and BT_REG_ON held low. REG_ON is WL_REG_ON OR'd internal to the 4325 with BT_REG_ON.

Table 18: WLAN Interface I/O Status

Signal Name	*I/O*	*On Status*	*Low Power Status / Sleep (all supplies present)*	*REG_ON Held LOW (WL and BT RST_N held LOW)* [b]	*HW Default (REG_ON High, WL and BT_RST_N high; no SW loaded)* [b]	*Power rail*	*Internal Pull-Up Resistor Range (ohm)*		*Internal Pull-Down Resistor Range (ohm)*		*Comment*
							3.3V	*1.8V*	*3.3V*	*1.8V*	
WRF_EXTREFIN	I	No internal pull. Must be driven.	No internal pull. Must be driven.	High-Z	No internal pull. Needs to be driven.	VDDIO	n/a	n/a	n/a	n/a	–
WL_REG_ON	I	No internal pull. Must be driven.	No internal pull. Must be driven.	No internal pull, must be driven Low	No internal pull. Needs to be driven.	VDDIO/ BT_VDDO	n/a	n/a	n/a	n/a	–
WL_RST_N	I	No internal pull. Must be driven.	No internal pull. Must be driven.	No internal pull, must be driven Low	No internal pull. Needs to be driven.	VDDIO	n/a	n/a	n/a	n/a	–
BT_RST_N	I	No internal pull. Must be driven.	No internal pull. Must be driven.	No internal pull, must be driven Low	No internal pull. Needs to be driven.	BT_VDDO	n/a	n/a	n/a	n/a	–
BT_REG_ON	I	No internal pull. Must be driven.	No internal pull. Must be driven.	No internal pull, must be driven Low	No internal pull. Needs to be driven.	VDDIO/ BT_VDDO	n/a	n/a	n/a	n/a	–
WL_GPIO	I/O	Programmable (In, Out, PD, PU)	Programmable (In, Out, PD, PU)	High-Z, No pull	High-Z No pull	VDDIO	58K to 63K	58K to 63K	58K to 63K	58K to 63K	Internal pull-up/down are programmable and can be enabled/disabled by S/W.
SDIO Data [3:0] [a]	I/O	Pull-up	Pull-up	High-Z, No pull	Pull-up	VDDIO_SD	15K to 35K	30K to 82K	n/a	n/a	PD not available, PU by default, can be disabled by SW.
SDIO CMD [a]	I/O	Pull-up	Pull-up	High-Z, No pull	Pull-up	VDDIO_SD	15K to 35K	30K to 82K	n/a	n/a	PD not available, PU by default, can be disabled by SW.
SDIO_CLK	I	No internal pull. Must be driven.	No internal pull. Must be driven.	High-Z	High-Z	VDDIO_SD	n/a	n/a	n/a	n/a	–

a. Section 6 of the SDIO physical layer specification states that the SDIO host must provide a 10k to 100k ohm pull-up resistor on each CMD and DAT(3:0) signal line. To properly operate the BCM4325, this requirement must be met by either programming internal PU resistors on the host or device side or adding discrete resistors.
b. REG_ON Held LOW = Both WL_REG_ON and BT_REG_ON held low. REG_ON is WL_REG_ON OR'd with BT_REG_ON in the BCM4325.

SDIO PIN DESCRIPTION

Table 19: SDIO Pin Description

SD 4-Bit Mode		*SD 1-Bit Mode*		*SPI Mode*	
SDIO_DATA_0	Data line 0	DATA	Data line	DO	Data output
SDIO_DATA_1	Data line 1 or Interrupt	IRQ	Interrupt	IRQ	Interrupt
SDIO_DATA_2	Data line 2 or Read Wait	RW	Read Wait	NC	Not used
SDIO_DATA_3	Data line 3	N/C	Not used	CS	Card select
SDIO_CLK	Clock	CLK	Clock	SCLK	Clock
SDIO_CMD	Command line	CMD	Command line	DI	Data input

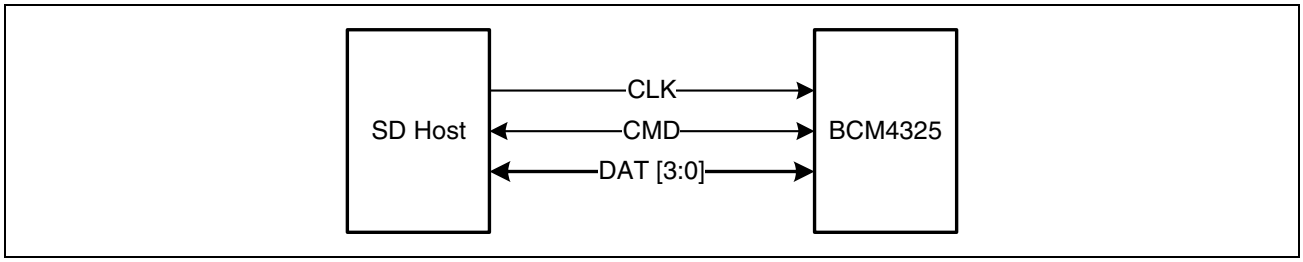


Figure 13: Signal Connections to SDIO Card (SD 4-Bit Mode)

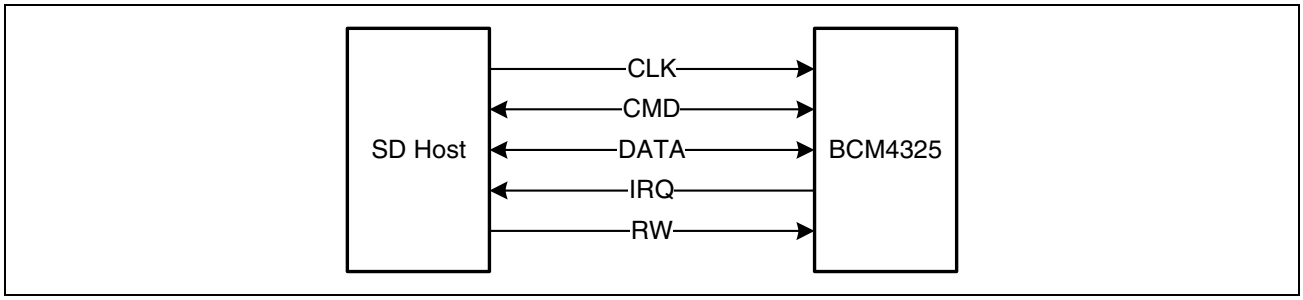


Figure 14: Signal Connections to SDIO Card (SD 1-Bit Mode)

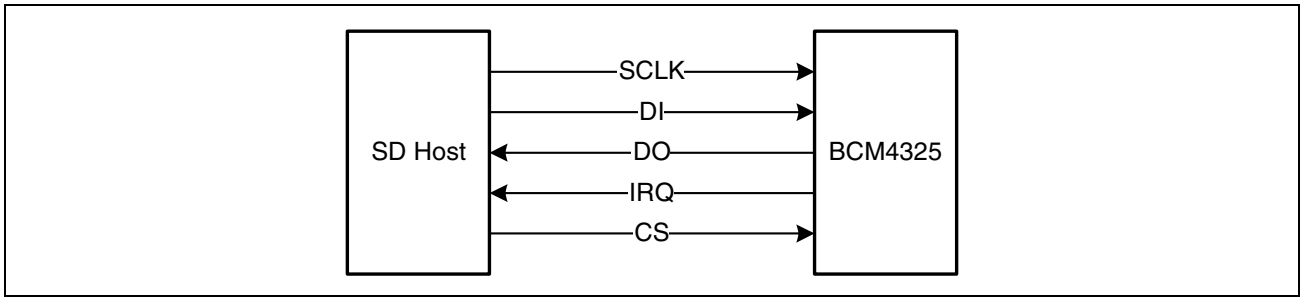


Figure 15: Signal Connections to SDIO Card (SPI Mode)

Section 16: Operating Conditions and DC Characteristics

Absolute Maximum Ratings

Caution! These specifications indicate levels where permanent damage to the device can occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 20: Absolute Maximum Ratings

Rating	Symbol	Value	Unit
DC supply voltage for VBATT	VBATT	–0.5 to 6.5	V
DC supply voltage for I/O	VDDIO	–0.5 to 4.1	V
DC supply voltage for WLAN PAs	VDDPAG VDDPAA	–0.5 to 4.1	V
DC supply voltage for BT PA	VDDTF	–0.5 to 2.9	V
DC supply voltage for RF	All 1.25V analog	–0.5 to 1.32	V
DC supply voltage for core	VDDC	–0.5 to 1.32	V
Maximum undershoot voltage for I/O	Vundershoot	–0.5	V
Maximum junction temperature	T_j	125	°C

Electrostatic Discharge Specifications

Use extreme caution to avoid damage due to electrostatic discharge (ESD). Proper use of wrist and heel grounding straps to discharge static electricity is required when handling microprocessor devices. When storing a device, place it in antistatic packaging.

Table 21: ESD Specifications

Pin Type	Symbol	Condition	ESD Rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human Body Model Contact Discharge per JEDEC EID/ JESD22-A114	±1500	V
Either HBM or MM to be tested.	ESD_HAND_MM	Machine Model Contact	±50	V
CDM to be tested	ESD_HAND_CDM	Charged Device Model Contact Discharge per JEDEC EIA/ JESD22-C101	±200	V

ENVIRONMENTAL RATINGS

Table 22: Environmental Ratings

Characteristic	Value	Units	Conditions/Comments
Ambient Temperature (T_A)	–30 to 85	°C	Operation
Storage Temperature	–40 to 125	°C	–
Relative Humidity	Less than 60	%	Storage
	Less than 85	%	Operation

RECOMMENDED OPERATING CONDITIONS

Table 23: Recommended Operating Conditions and DC Characteristics

Element	Symbol	Value			Unit
		Minimum	Typical	Maximum	
DC supply voltage for VBATT [a]	VDDBATT	2.3	3.3	5.5	V
DC supply voltage for I/O [a]	VDDIO	1.62	3.3 or 1.8	3.63	V
DC supply voltage for WLAN PAs[a]	WRF_VDDPAG WRF_VDDPAA	2.97	3.3	3.63	V
DC Supply for BT PA[a]:	VDDTF				
Class1		2.38	2.5	2.63	V
Class2		1.4	1.5	1.6	V
Class3		1.19	1.25	1.31	V
DC supply voltage for core [a]	VDDC	1.19	1.25	1.31	V
Input low voltage (VDDIO = 3.3V)	V_{IL}	–	–	0.8	V
Input high voltage (VDDIO = 3.3V)	V_{IH}	2.0	–	VDDIO	V
Input low voltage (VDDIO = 1.8V)	V_{IL}	–	–	0.6	V
Input high voltage (VDDIO = 1.8V)	V_{IH}	1.1	–	VDDIO	V
Output low voltage	V_{OL}	–	–	0.4	V
Output high voltage	V_{OH}	VDDIO – 0.4V		–	V
Input low current	I_{IL}	–	0.3	–	µA
Input high current	I_{IH}	–	0.3	–	µA
Output low current (VDDIO = 3.3V, V_{OL} = 0.4V)	I_{OL}	–	–	3.0	mA
Output high current (VDDIO = 3.3V, V_{OH} = 2.9V)	I_{OH}	–	–	3.0	mA
SDIO input/output current	I_{sdio}	–	–	12	mA

a. **Caution:** Functional operation is not guaranteed outside specified limits. Operation outside these limits for extended periods may adversely affect the long-term reliability of the device.

BLUETOOTH AND FM CURRENT CONSUMPTION

Note: WLAN_RST_N is low for all measurements.

Note: For Class 1, VDDTF is supplied 2.5V externally separate from VBATT. For FM, the Bluetooth is in reset. The current consumption numbers are measured based on typical output power specified in the Table 27: "Bluetooth Transmitter RF Specifications," on page 81.

Table 24: Bluetooth and FM Current Consumption

Test Item	Operating Mode	Class 1			Class 2		Unit
		Vbat=3.6V and Vddio=3.3V			Vbat=3.6V and Vddio=3.3V		
		VBAT	VDDTF =2.5V	VDDIO	VBAT	VDDIO	
1	Sleep	0.18	0.001	0.005	–	–	mA
2	Standard 1.28s Inquiry Scan	0.41	0.004	–	–	–	mA
3	Standard 2.56s Inquiry Scan	0.30	0.002	–	–	–	mA
4	R1 Standard Page Scan	0.41	0.004	–	–	–	mA
5	Standard page and 1.28s Inquiry Scan	0.61	0.01	–	–	–	mA
6	Standard page and 2.56s Inquiry Scan	0.50	0.005	–	–	–	mA
7	500 ms Sniff Master	0.41	0.06	–	–	–	mA
8	500 ms Sniff Slave	0.41	0.06	–	–	–	mA
13	500 ms Sniff Master Page and 1.28s Inquiry Scan	1.01	0.06	–	–	–	mA
17	DM1/DH1 Master	18.10	22.24	–	23.26	–	mA
18	DM3/DH3 Master	19.20	26.84	–	25.10	–	mA
19	DM5/DH5 Master	19.28	25.08	–	24.78	–	mA
22	HV3 Master [a]	10.54	7.42	–	12.31	–	mA
23	FM I^2S Audio	9.50	–	–	–	–	mA
24	FM Analog Audio	11.00	–	–	–	–	mA
25	BT_Reset + WL_Reset	0.02	0.001	0.005	–	0.005	mA

a. Includes sniff.

WLAN CURRENT CONSUMPTION

Note: BT_RST_N is low for all measurements.

Table 25: WLAN Current Consumption using Power Topology #1 (Vbatt with Buck-Boost) [a]

Operational State	*VBATT = 3.6V, VDDIO = 3.3V*	
	Typical	*Units*
Leakage (WLAN and BT/FM in reset) [b, c, d]	20	uA
Sleep with Buck-Boost in burst mode (driver controlled)	250	uA
Sleep with Buck-Boost shutdown (driver controlled)	160	uA
Idle between beacons	152	uA
IEEE PS@DTIM = 100 ms	1.3	mA
IEEE PS@DTIM = 300 ms	553	uA
Beacon reception	78	mA
Rx 1 Mbps	79	mA
Rx 11 Mbps	79	mA
Rx 6 Mbps	81	mA
Rx 54 Mbps	83	mA
TX 1 Mbps, 18 dBm at chip Tx output [e]	245	mA
TX 1 Mbps, 21 dBm at chip Tx output [e]	288	mA
TX 11 Mbps, 18 dBm at chip Tx output [e]	249	mA
TX 11 Mbps, 21 dBm at chip Tx output [e]	295	mA
TX 6 Mbps, 17 dBm at chip Tx output [e]	240	mA
TX 6 Mbps, 20 dBm at chip Tx output [e]	276	mA
TX 54 Mbps, 17 dBm at chip Tx output [e]	241	mA
TX 54 Mbps, 20 dBm at chip Tx output [e]	277	mA

a. For details, refer to the *BCM4325 Power Supply Topologies* application note (document number 4325-AN60X-R).
b. Additional leakage current may occur at the board level, depending on factors such as the power topology and external PU/PD resistors, etc.
c. All measurements include VDDIO current with VDDIO = 3.3V.
d. All measurements exclude current drawn by the external 32.768 KHz oscillator, which is required for operation.
e. Chip Tx output power is based on Broadcom reference board measurements and backward calculation from antenna test port.

Section 17: Bluetooth RF Specifications

Note: Unless otherwise stated, all specifications in this section apply to the operating temperature and voltage ranges specified in Table 20 and Table 22 on page 76 and Table 23 on page 76. Functional operation outside these limits is not guaranteed.

Table 26: Bluetooth Receiver RF Specifications

Parameter	Conditions	Minimum	Typical [d]	Maximum	Unit
General					
Frequency range	–	2402	–	2480	MHz
RX sensitivity [a]	GFSK, 0.1% BER, 1 Mbps	–	–88.0	–84.0	dBm
	π/4-DQPSK, 0.01% BER, 2 Mbps	–	–90.0	–84.0	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–85.0	–80.0	dBm
Input IP3	–	–16	–	–	dBm
Maximum input	–	–	–	–20.0	dBm
Interference Performance					
C/I cochannel	GFSK, 0.1% BER	–	–	11.0	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3-MHz adjacent channel	GFSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–	–20.0	dB
C/I co-channel	π/4-DQPSK, 0.1% BER	–	–	13.0	dB
C/I 1 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	0.0	dB
C/I 2 MHz adjacent channel	π/4-DQPSK, 0.1% BER	–	–	–30.0	dB
C/I ≥ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–40.0	dB
C/I image channel	π/4-DQPSK, 0.1% BER	–	–	–7.0	dB
C/I 1 MHz adjacent to image channel	π/4-DQPSK, 0.1% BER	–	–	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	–	21.0	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	5.0	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–25.0	dB
C/I > = 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–	0.0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–	–13.0	dB
Out-of-Band Blocking Performance (CW)					
30 MHz – 2000 MHz	0.1% BER	–	–10.0	–	dBm
2000 – 2399 MHz	0.1% BER	–	–27	–	dBm
2498 – 3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz – 12.75 GHz	0.1% BER	–	–10.0	–	dBm

Table 26: Bluetooth Receiver RF Specifications (Cont.)

Parameter	Conditions	Minimum	Typical [d]	Maximum	Unit
Out-of-Band Blocking Performance, Modulated Interferer [b]					
824 – 849 MHz, CDMA	–	–	–10	–	dBm
824 – 849 MHz, EDGE/GSM	–	–	–2	–	dBm
880 – 915 MHz, EDGE/GSM	–	–	–2	–	dBm
1710 – 1785 MHz, EDGE/GSM	–	–	–5	–	dBm
1850 – 1910 MHz, EDGE/GSM	–	–	–5	–	dBm
1850 – 1910 MHz, CDMA	–	–	–15	–	dBm
1850 – 1910 MHz, WCDMA	–	–	–20	–	dBm
1920 – 1980 MHz, WCDMA	–	–	–20	–	dBm
776 – 794 MHz, CDMA	–	–	–10	–	dBm
Spurious Emissions [c]					
30 MHz – 1 GHz	–	–	–80	–57	dBm
1 GHz – 12.75 GHz	–	–	–51	–47	dBm
Cell-band Noise Floor					
824 – 850 MHz, EDGE/GSM	–	–	–145	–	dBm/Hz
880 – 915 MHz, EDGE/GSM	–	–	–145	–	dBm/Hz
1710 – 1785 MHz, EDGE/GSM	–	–	–145	–	dBm/Hz
1850 – 1910 MHz, EDGE/GSM	–	–	–145	–	dBm/Hz
1920 – 1980 MHz, WCDMA	–	–	–145	–	dBm/Hz

a. The receiver sensitivity is measured at a BER of 0.1% on the device interface.
b. Bluetooth reference level of –82 dBm.
c. Includes baseband-radiated emissions.
d. Typical operating conditions are 1.25V operating voltage and 25°C ambient temperature.

Note: The maximum value represents the actual Bluetooth specification required for Bluetooth qualification as defined in the version 2.1 specification.

Table 27: Bluetooth Transmitter RF Specifications [a]

Parameter	Minimum	Typical	Maximum	Unit
General				
Frequency range	2402	–	2480	MHz
Class1, TX max powerBT_VDDTF = 2.5V (max. up to 3.1V)	4.5	7.5	–	dBm
Class2, TX max powerBT_VDDTF = 1.5V	0	4[b]	–	dBm
Class1, TX min powerBT_VDDTF = 2.5V (max. up to 3.1V)	–	–18	–	dBm
Class2, TX min powerBT_VDDTF = 1.5V	–	–20	–	dBm
Gain step	2	4	6	dB
In-Band Spurious Emissions				
±500 kHz	–	–	–20.0	dBc
1.0 MHz < |M – N| < 1.5 MHz	–	–	–26.0	dBc
1.5 MHz < |M – N| < 2.5 MHz	–	–	–40.0	dBm
|M – N| ≥ 2.5 MHz	–	–	–60.0	dBm
Out-of-Band Spurious Emissions				
30 MHz to 1 GHz	–	–	–36.0 [c, d]	dBm
1 GHz to 12.75 GHz	–	–	–30.0 [a]	dBm
1.8 GHz to 1.9 GHz	–	–	–37.0	dBm
5.15 GHz to 5.3 GHz	–	–	–37.0	dBm
GPS Band Spurious Emissions				
Without SAW filter	–	–150	–	dBm/Hz
Out-of-Band Noise Floor				
746 MHz to 764 MHz	–	–145	–	dBm/Hz
851 MHz to 894 MHz	–	–145	–	dBm/Hz
925 MHz to 960 MHz	–	–145	–	dBm/Hz
1805 MHz to 1880 MHz	–	–145	–	dBm/Hz
1930 MHz to 1990 MHz	–	–145	–	dBm/Hz
2110 MHz to 2170 MHz	–	–145	–	dBm/Hz

a. The RF characteristics are measured at the device interface.
b. Actual output power can be adjusted to a lower level based on product requirements.
c. The maximum value represents the value required for Bluetooth qualification as defined in the version 2.1 specification.
d. The spurious emissions during Idle mode are the same as specified in Table 26 on page 79.

Section 18: FM Receiver Specifications

Note: Unless otherwise stated, all specifications in this section apply to the operating temperature and voltage ranges specified in Table 20 and Table 22 on page 76 and Table 23 on page 76. Functional operation outside these limits is not guaranteed.

Table 28: FM Receiver Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
RF Parameters					
Operating frequency	Frequencies inclusive	76	–	108	MHz
Sensitivity, V_{RF}	FM only, fmod = 1kHz Δf = 22.5 kHz (S+N)/N=26 dB BAF = 300 Hz to 15 kHz A-weighted de-emphasis = 50 µs, f_{IN} = 76 to 108 MHz	–	–105	–102	dBm
	RDS. For an RDS deviation of 1.2 kHz. 95% of blocks decoded with no errors, over a sample of 5000 blocks. [b]	–	23	28	dBuV
	RDS. For an RDS deviation of 2 kHz. 95% of blocks decoded with no errors, over a sample of 5000 blocks. [b]	–	19	24	dBuV
Receiver adjacent channel selectivity	At ±200 kHz. f_{IN} = 76 to 108 MHz, Measured for 40 dB SNR at the audio output.	16	–	–	dB
	At ±300 kHz (as above)	25	–	–	dB
Image response (assuming image frequency ≥ ±300 kHz), mono	At f_{wanted} ±2f IF depending on LO injection relative to F_{wanted}. Should be 40 dB SNR at the audio output	25	–	–	dB
Image response (assuming image frequency ≥ ±300 kHz), stereo		0	–	–	dB
Min S/N for in band blocking for offsets ≥ 400 KHz and ≤ 1 MHz, mono	Wanted level set to –90 dBm, Δf = 75 kHz, Interferer level set to –55 dBm, Δf = 40 kHz, 1-kHz tone, AGC on	35	–	–	dB
Min S/N for in band blocking for offsets ≥ 400 KHz and ≤ 1 MHz, stereo	Wanted level set to –72 dBm, Δf = 75 kHz, 1-kHz tone. Interferer level set to –37 dBm	35	–	–	dB
Intermediate S/N in the presence of intermodulation	Overall third-order intercept point, for tones ±400 and ±800 kHz, ±4 and ±8 MHz. Reference level is –82 dBm, tone levels set at –50 dBm. f_{IN} = 76 to 108 MHz. AGC enabled	40	–	–	dB
AM suppression, mono	Vin = –90 dBm, fmod = 1 kHz, Δf = 22.5 kHz, m = 0.3, BAF = 300 Hz to 15 kHz, L = R, de-emphasis = 75 µs	40	–	–	dB
AM suppression, stereo	Vin = –47 dBm, fmod = 1 kHz, Δf = 22.5 kHz, m = 0.3, BAF = 300 Hz to 15 kHz, L = R, de-emphasis = 75 µs	40	–	–	dB

Table 28: FM Receiver Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Intermediate S/N	Vin = –90 dBm, fmod = 1 kHz, Δf = 22.5 kHz, m = 0.3, BAF = 300 Hz to 15 kHz A-weighted, MONO, de-emphasis = 50 µs	45	–	–	dB
RF Input					
RF input impedance	Single-ended input with optional external matching circuitry	–	50	–	Ω
RF input level	Maximum on-channel input level 76–108 MHz.	–	–	–10	dBm
RF input impedance return loss	With external matching circuitry	–	–	–6	dB
RF conducted emissions	Local oscillator breakthrough measured on the reference port	–	–	–55	dBm
	925–960 MHz, 1805 –1880 MHz and 1930–1990 MHz	–	–	–90	dBm
RF blocking levels at the FM antenna input. (Assumes presence of an external matching circuit.)	824–915 MHz, GSM 200 kHz BW, CDMA 1.2 MHz BW	–	–	0	dBm
	1710–1980 MHz, GSM 200 kHz BW, CDMA 1.2 MHz BW, WCDMA 4 MHz BW	–	–	–5	dBm
	2.4–2.4835 GHz, BT 1 MHz BW, WLAN 20 MHz BW	–	–	–20	dBm
PLL					
Frequency step	Channel offset	–	–	50	kHz
Settling time	Single frequency switch in any direction to a frequency within the bands 88–108 MHz or 76–90 MHz. Time measured to within 5 kHz of the final frequency.	–	5	–	ms
Sweep time	Total time for an automatic search to sweep from 88–108 MHz or 76–90 MHz (and reverse direction) assuming no channels found.	–	8	–	sec
Soft Mute					
Soft mute start level [a]	Mute attenuation = 3 dB	3	5	10	uV
Soft mute attenuation	Vin = 1 µV, Δf = 22.5 kHz, L = R fmod = 1 kHz, BAF = 300 Hz to 15 kHz, de-emphasis = 75 µs	10	20	30	dB
General Audio					
Audio output level	Vin = 1 mV, Δf = 22.5 kHz_p fmod = 1 kHz, L = R, de-emphasis = 75 µs. Δf Pilot = 6.75 kHz_p, Rload > 30 kΩ	60	75	90	mV, rms
Maximum audio output level	Vin = 1 mV, Δf = 100 kHz_p fmod = 1 kHz, L = R, de-emphasis = 75 µs. Δf Pilot = 6.75 kHz_p, Rload > 30 kΩ	–	–	360	mV, rms
Audio output level difference	Vin = 1 mV, Δf = 22.5 kHz, fmod = 1 kHz, L = R, de-emphasis = 75 µs	–1	–	1	dB
Max signal plus noise to noise ratio (S+N)/N, mono	Vin = 1 mV, Δf = 22.5 kHz, fmod = 1 kHz, de-emphasis = 50 µs, L = R, BAF = 300 Hz to 15 kHz (A-Weighted) f_{IN} = 76 to 108 MHz	53	57	–	dB
Max signal plus noise to noise ratio (S+N)/N, stereo		48	53	–	dB

Table 28: FM Receiver Specifications (Cont.)

Parameter	Conditions	Minimum	Typical	Maximum	Units
Total harmonic distortion, mono	Vin = 1 mV, Δf = 75 kHz, L = R, fmod = 400 Hz, de-emphasis = 50 µs.	–	0.4	0.8	%
	Vin = 1 mV, Δf = 75 kHz, L = R, fmod = 1 kHz, de-emphasis = 50 µs.	–	0.4	0.8	%
	Vin = 1 mV, Δf = 100 kHz, L = R, fmod = 1 kHz, de-emphasis = 50 µs.	–	0.5	1.0	%
Total harmonic distortion, stereo	Vin = 1 mV, Δf = 75 kHz, L = R, fmod = 3 kHz, de-emphasis = 50 µs.	–	0.9	1.5	%
Audio spurious products	Vin = 1 mV, Δf = 22.5 kHz, fmod = 1 kHz, de-emphasis = 50 µs, L = R, BAF = 300 Hz to 15 kHz (A-Weighted), f_{IN} = 76 to 108 MHz, With respect to 1 kHz tone.	–	–	–60	dBc
Audio bandwidth, upper (–3 dB point)	Vin = 1 mV, Δf = 22.5 kHz, for both 50 and 75 µs de-emphasis, pre-emphasis applied.	15	–	–	KHz
Audio bandwidth, lower (–3 dB point)		–	–	20	Hz
Deviation of the audio response from an ideal de-emphasis curve	100 Hz to 13 kHz, Vin = 1 mV, Δf = 22.5 kHz, for both 50 and 75 µs de-emphasis, pre-emphasis applied.	–	–	±0.5	dB
De-emphasis time constant tolerance	With respect to 50 and 75 µs.	–	–	±5	%
Audio output impedance	When FM function is disabled, or when left or right channels are hard-muted via the bus.	50	–	–	KΩ
Audio output impedance	When FM function is enabled and in any of the following modes: autosearch, AC-muted by software, or RF soft-mute is active.	–	50	–	Ω
Left and right AC_mute		60	–	–	dB
Right audio output hard muting attenuation		80	–	–	dB
Left audio output hard muting attenuation		80	–	–	dB
Pause Detection					
Audio level at which a pause is detected	Relative to 1 kHz tone, 22.5 kHz deviation, 50 µs de-emphasis	–	–	–	–
	Four values in 3 dB steps	–21	–	–12	dB
Audio pause duration	Four values	20	–	40	ms
Stereo Decoder					
Stereo channel separation	SNC OFF, increasing RF input, switched from mono to stereo Δf = 75 kHz, fmod = 1 kHz, 30 µV input level, R = 0, L = 1 including 9% pilot	27	30	–	dB
Pilot suppression	Measured at audio outputs. Δf = 75 kHz, fmod = 1 kHz, de-emphasis = 75 µs	46	–	–	dB

a. Start level is configurable.
b. RDS sensitivity range is only from 87.5 MHz to 108 MHz.

Section 19: WLAN RF Specifications

INTRODUCTION

The BCM4325 includes an integrated dual-band direct conversion radio that supports either the 2.4 GHz IEEE 802.11g band or the 5 GHz IEEE 802.11a band. The BCM4325 does not provide simultaneous 2.4 GHz and 5 GHz operation. This section describes the RF characteristics of the 2.4 GHz and 5 GHz portions of the radio.

Note: Unless otherwise stated, all specifications in this section apply to the operating temperature and voltage ranges specified in Table 20 and Table 22 on page 76 and Table 23 on page 76. Functional operation outside these limits is not guaranteed.

CELLULAR BLOCKING

WLAN and cellular transceivers have separate antennas. The isolation between the antennas is 20 dB in all cases (for example, the maximum EGSM900 signal power at the WLAN RF port is +13 dBm).

Table 29: Blocking Signals from Embedded Cellular Transmitter at Cellular Antenna Port

System	*Frequency (MHz)*	*Maximum Power Output*	*Modulation*
GSM	824–849	+33 dBm	GMSK
		+27	EDGE
CDMA	824–849	+25	QPSK
EGSM900	880–915	+33	GMSK
		+27	EDGE
DCS1800	1710–1785	+30	GMSK
		+26	EDGE
PCS1900	1850–1910	+30	GMSK
		+26	EDGE
CDMA	1850–1910	+24	QPSK
WDCMA FDD	1920–1980	+21	QPSK
Wideband noise from cellular TX	2400–2500	–150 dBm/Hz	–

Note: GMSK and EDGE transmissions have duty cycle of 1/8 or 1/4. Nominal repetition rate of transmission is about 217 Hz. QPSK transmissions for (W)CDMA have a duty cycle of 1.

WLAN Receiver Blocking Performance

The total contribution of out-of-band signals from a cellular band transmitter and wideband noise falling on the WLAN band does not reduce the sensitivity of the WLAN receiver more than 1 dB compared to the performance without interference. Only one cellular transmitter is active at a time.

The cited specifications assume the use of an external cellular blocking filter that has the following characteristics:

- (NdBa) TiO_3 ($E_r = 88/T_{Cf} = 0 \pm 10$ ppm/K) with a coating of copper (10 μm thick) and tin (>5 μm thick)
- Operating temperature = –30°C to +85°C
- Center frequency = 2.450 GHz
- Insertion loss = 0.7 dB (typical), 1.0 dB (maximum)
- Pass band (2400–2500) = 100 MHz (minimum)
- Amplitude ripple (peak-to-peak) = 0.4 dB (typical), 0.8 dB (maximum)
- SWR = 1.5 (typical), 2.0 (maximum)
- Impedance = 50Ω (typical)
- Attenuation:
  - @ DC to 880 MHz — 50 dB (minimum), 55 dB (typical)
  - @ 880 to 960 MHz — 45 dB (minimum), 50 dB (typical)
  - @ 960 to 1990 MHz — 40 dB (minimum), 45 dB (typical)
  - @ 1990 to 2100 MHz — 25 dB (minimum), 30 dB (typical)

2.4 GHz Band General RF Specifications

Table 30: 2.4 GHz Band General RF Specifications

Item	Condition	Minimum	Typical	Maximum	Unit
TX/RX Switch Time	Including TX ramp down	–	5	10	μs
RX/TX Switch Time	Including TX ramp up	–	5	5	μs

2.4 GHz Band Local Oscillator Specifications

Table 31: 2.4 GHz Band Local Oscillator Specifications

Characteristic	Condition	Minimum	Typical	Maximum	Unit
VCO Frequency Range	–	2412	–	2484	MHz
Reference Input Frequency Range	–	–	Various [a]	–	MHz
Reference Spurs	–	–	–	–34	dBc
Local Oscillator Phase Noise, single-sided from 1 to 300 kHz offset	–	–	–	–86.5	dBc/Hz
Clock Frequency Tolerance	–	–	–	±20	ppm

a. Reference supported frequencies range from 13 MHz to 52 MHz.

2.4 GHz Band Receiver RF Specifications

Table 32: 2.4 GHz Band Receiver RF Specifications

Characteristic	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
Cascaded Noise Figure	–	–	4	–	dB
Maximum Receive Level (when using a suitable external switch)	@ 1, 2 Mbps	–4	–	–	dBm
	@ 5.5, 11 Mbps	–10	–	–	dBm
	@ 54 Mbps	–10	–	–	dBm
PGA DC Rejection Servo Loop Bandwidth	WB mode	–	1	–	MHz
	NB mode	120 Hz	–	230 kHz	–
LPF DC Rejection Servo Loop Bandwidth	WB mode	–	500	–	kHz
	NB mode	120 Hz	–	230 kHz	–
Adjacent Channel Power Rejection (DSSS at 11Mbps [a])	Rx = –70 dBm [b]	35	–	–	dB
Maximum Receiver Gain	–	–	>100	–	dB

a. The difference between the interfering and desired signal (> 25 MHz apart) at 8% PER for 1024 octet PSDU with desired signal level, as specified.
b. Values are measured at the input to the BCM4325. Accordingly, they include insertion losses from the integrated baluns, but these values do not include the insertion loss of the external RF path. Reference sensitivity (10% PER for OFDM and 8% PER for DSSS for 1000-octet PSDU) at chip input.

2.4 GHz Receiver Performance Specifications

Table 33: 2.4 GHz Receiver Performance Specifications

Rate/Modulation	*Typical Receive Sensitivity [a]*
1 Mbps DSSS	–96.0 dBm
2 Mbps DSSS	–95.0 dBm
5.5 Mbps DSSS	–93.0 dBm
11 Mbps DSSS	–90.5 dBm
6 Mbps OFDM	–91.5 dBm
9 Mbps OFDM	–91.0 dBm
12 Mbps OFDM	–90.5 dBm
18 Mbps OFDM	–89.0 dBm
24 Mbps OFDM	–85.5 dBm
36 Mbps OFDM	–82.5 dBm
48 Mbps OFDM	–77.0 dBm
54 Mbps OFDM	–75.5 dBm

a. Values are measured at the input to the BCM4325. Accordingly, they include insertion losses from the integrated baluns, but these values do not include the insertion loss of the external RF path. Reference sensitivity (10% PER for OFDM and 8% PER for DSSS for 1000-octet PSDU) at chip input.

2.4 GHz Band Transmitter RF Specifications

Table 34: 2.4 GHz Band Transmitter RF Specifications

Characteristic	Condition	Minimum	Typical	Maximum	Unit
RF Output Frequency Range	–	2400	–	2500	MHz
Output Power (EVM Compliant)	Maximum gain	–	–	+22 [c]	dBm
Gain Flatness	Maximum gain	–	–	2	dB
Output IP3	Maximum gain	–	37	–	dBm
Output P1dB	–	–	27	–	dBm
Carrier Suppression	–	15	–	–	dBr
TX Spectrum mask @ maximum gain CCK	fc – 22 MHz < f < fc – 11 MHz	–	–	–30	dBr
	fc + 11 MHz < f< fc + 22 MHz	–	–	–30	dBr
	f < fc – 22 MHz; and f > fc + 22 MHz	–	–	–50	dBr
TX Spectrum mask (chip output power = 16 dBm) OFDM	f < fc – 11 MHz and f > fc + 11 MHz	–	–	–26	dBc
	f < fc – 20 MHz and f > fc + 20 MHz	–	–	–35	dBr
	f < fc – 30 MHz and f > fc + 30 MHz	–	–	–40	dBr
TX Modulation Accuracy (EVM) at maximum gain	IEEE 802.11b mode	–	–	35%	–
	IEEE 802.11g mode QAM64 54 Mbps	–	–	5%	–
Gain Control Step Size	NA	–	0.25 dB	–	dB/step
Amplitude Balance [a]	DC input	–1	–	1	dB
Phase Balance [a]	DC input	–1.5	–	1.5	° (degrees)
Baseband Differential Input Voltage	Shaped pulse	–	0.6	–	Vpp
TX Power Ramp Up	90% of final power	–	–	2	µsec
TX Power Ramp Down	10% of final power	–	–	2	µsec
Out-of-Band Noise and Spurious Emissions					
100 kHz to 1930 MHz	21 dBm at Chip Tx output [b]	–	–145	–	dBm/Hz
1930 to 2170 MHz	21 dBm at Chip Tx output [b]	–	–135	–	dBm/Hz
2170 to 2300 MHz	21 dBm at Chip Tx output [b]	–	–125	–	dBm/Hz
2300 to 2390 MHz	21 dBm at Chip Tx output [b]	–	–115	–	dBm/Hz
2484 to 2655 MHz	21 dBm at Chip Tx output [b]	–	–115	–	dBm/Hz
2655 to 4700 MHz	21 dBm at Chip Tx output [b]	–	–125	–	dBm/Hz
4700 to 12750 MHz	21 dBm at Chip Tx output [b]	–	–135	–	dBm/Hz

a. At a 3 MHz offset from the carrier frequency.
b. +21 dBm Chip Tx output power is based on Broadcom reference board level measurements and backward calculation from antenna test port.
c. Referred to the chip output. The maximum output power at the antenna test port depends on board layout and output matching.

5 GHz Band Receiver RF Specifications

Table 35: 5 GHz Band Receiver RF Specifications [a]

Characteristic	*Condition*	*Minimum*	*Typical*	*Maximum*	*Unit*
Cascaded Noise Figure	Maximum RX gain	–	4.5	–	dB
Maximum Receive Level [a](5.24 GHz)	@ 6 Mbps	–10	–	–	dBm
	@ 54 Mbps	–15	–	–	dBm
DC Rejection Servo Loop Bandwidth (normal operation)	WB mode	–	500	–	kHz
	NB mode	120 Hz	–	230 kHz	NA
Adjacent Channel Power Rejection (OFDM at 54 Mbps [b])	Rx at –62 dBm [d]	–1	–	–	dB
Alternate Adjacent Channel Power Rejection (OFDM at 54Mbps [c])	Rx at –61.5 dBm [d]	15	–	–	dB
Minimum RX Gain	–	–	15	–	dB
Maximum RX Gain	–	–	>100	–	dB
IQ Amplitude Balance	–	–	0.5	–	dB
IQ Phase Balance	–	–	1.5	–	Degree
Out-of-Band Blocking Performance without RF Band-Pass Filter (–1dB desensitization)					
CW	30 – 4300 MHz	–10	–	–	dBm
CW	4300 – 4800 MHz	–25	–	–	dBm
CW	5900 – 6400 MHz	–25	–	–	dBm

a. With minimum RF gain.
b. The difference between the interfering and tehe desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with the desired signal level, as specified.
c. The difference between the interfering and the desired signal (40 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level, as specified.
d. Values are measured at the input pin of the BCM4325. Accordingly, they include insertion losses from the integrated baluns but do not include the insertion loss of the external RF path.

5 GHz Band Transmitter RF Specifications

Table 36: 5 GHz Band Transmitter RF Specifications

Characteristic	Condition	Minimum	Typical	Maximum	Unit
RF Output Frequency Range	NA	4920	–	5805	MHz
Gain Flatness	Maximum gain	–	–	1	dB
Output IP3	Maximum gain	–	35	–	dBm
Output P1dB	Maximum gain	–	25	–	dBm
Output Power (EVM Compliant)	Minimum gain	–	–	–	dBm
Carrier Suppression	–	–15	–	–	dBr
TX Spectrum mask (chip output power = 16 dBm) OFDM	f < fc – 11 MHz and f > fc + 11 MHz	–	–	–26	dBc
	f < fc – 20 MHz and f > fc + 20 MHz	–	–	–35	dBr
	f < fc – 30 MHz and f > fc + 30 MHz	–	–	–40	dBr
Gain Control Step Size	NA	–	0.25	–	dB/step
I/Q Baseband 3 dB Bandwidth	NA	–	12	–	MHz
Amplitude Balance	DC Input	–0.5	–	0.5	dB
Phase Balance	DC Input	–1.5	–	1.5	° (degree)
Baseband Differential Input Voltage	NA	–	0.7	–	Vpp
TX Power Ramp Up	90% of final power	–	–	2	µsec
TX Power Ramp Down	10% of final power	–	–	2	µsec

5 GHz Band Local Oscillator Frequency Generator Specifications

Table 37: 5 GHz Band Local Oscillator Frequency Generator Specifications

Characteristic	Condition	Minimum	Typical	Maximum	Unit
VCO Frequency Range	–	4920	–	5805	MHz
Reference Input Frequency Range	–	–	various [a]	–	MHz
Reference Spurs	–	–	–	–30	dBc
Local Oscillator Integrated Phase Noise (1–300 kHz)	4.920–5.700 GHz	–	0.7	–	degree
	5.725–5.805 GHz	–	1.4	–	degree
Clock Frequency Tolerance	–	–	–	±20	ppm

a. Reference supported frequencies range from 13 MHz to 52 MHz.

5 GHz Receiver Performance Specifications

Table 38: 5 GHz Receiver Performance Specifications

Rate/Modulation	*Typical Receive Sensitivity* [a]
6 Mbps OFDM	–89.5 dBm
9 Mbps OFDM	–89.0 dBm
12 Mbps OFDM	–89.0 dBm
18 Mbps OFDM	–88.5 dBm
24 Mbps OFDM	–84.5 dBm
36 Mbps OFDM	–81.5 dBm
48 Mbps OFDM	–76.5 dBm
54 Mbps OFDM	–74.5 dBm

a. Values are measured at the BCM4325 input pin. Accordingly, they include insertion losses from the integrated baluns, but do not include the insertion loss of the external RF path. Reference sensitivity (10% PER for 1000-octet PSDU) at chip input.

Section 20: Internal Regulator Electrical Specifications

Note: Functional operation is not guaranteed outside specified limits. Operation outside these limits for extended periods may adversely affect the long-term reliability of the device.

CLDO

Table 39: CLDO

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
Input supply voltage [a]	–	–	1.5	1.98	Volt
Output voltage	Programmable in 25 mV steps	1.10	1.25	1.35	Volt
Absolute accuracy	–	–	–	±4	%
Output current	–	–	–	200	mA
LDO quiescent current	–	–	10	15	uA
Leakage current through output transistor	CLDO_pu=0	–	0.1	10	uA
Output noise	@30 kHz, 200 mA load	–	80	–	nV/rt Hz
Power supply rejection (PSR)	@1 kHz, 150 mV dropout	–	40	–	dB
Dropout voltage	–	150	–	–	mV
Start-up time	–	–	–	0.5	ms

a. For good PSRR performance, the input supply should be at least 200 mV higher than the output.

LNLDOi (i = 1, 2, or 4)

LNLDO4 is only available in the 339-pin CSP package.

Table 40: LNLDOi

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
Input supply voltage [a]	LNLDOi_vo_sel=0	–	1.5	1.98	Volts
	LNLDOi_vo_sel=1	–	3.3	3.6	
Output voltage	LNLDOi_vo_sel=0	1.10	1.25	1.35	Volts
	LNLDOi_vo_sel=1	2.5	2.5	3.1	
Absolute accuracy	–	–	–	±4	%
Output current for LNLDO1	–	–	–	130	mA
Output current for LNLDO2	–	–	–	80	mA
Output current for LNLDO4	–	–	–	80	mA
Quiescent current for LNLDO1	LNLDOi_vo_sel=0	–	31	44	uA
	LNLDOi_vo_sel=1	–	110	206	
Quiescent current for LNLDO2 and 4	LNLDOi_vo_sel=0	–	29	42	uA
	LNLDOi_vo_sel=1	–	108	202	
Leakage current for LNLDO1	LNLDO1_pu=0	–	–	–	
	LNLDOi_vo_sel=0	–	0.1	5	uA
	LNLDOi_vo_sel=1	–	0.1	9	
Leakage current for LNLDO2 and 4	LNLDO1_pu=0	–	–	–	
	LNLDOi_vo_sel=0	–	0.1	2	uA
	LNLDOi_vo_sel=1	–	0.1	4	
Output noise	@30 kHz, 50 mA load	–	–	–	
	LNLDOi_vo_sel=0	–	20	–	nV/rt Hz
	LNLDOi_vo_sel=1	–	31	–	
PSRR	@1 kHz, 150 mV dropout	–	50	–	dB
Dropout voltage	–	150	–	–	mV
Start-up time	–	–	–	0.5	ms

a. For good PSRR performance, the input supply should be at least 200 mV higher than the output.

CORE BUCK REGULATOR

Table 41: Core Buck Regulator

Specification	Notes	Minimum	Typical	Maximum	Units
Input supply voltage	–	2.3	–	5.5	Volts
PWM mode switching frequency	–	2.24	2.8	3.36	MHz
PWM output current	–	–	–	300	mA
Output voltage range	Programmable, 25 mV steps	1	1.5	1.75	Volts
PWM ripple voltage, static load	–	–	–	20	mVp-p
PWM ripple voltage, dynamic load	200 mA, 1 µs rise/fall current step	–	–	85	mVp-p
Burst mode ripple voltage, static	–	–	–	80	mVp-p
PWM mode efficiency	200 mA load current	80	90 [b]	–	%
Burst mode efficiency	10 mA load current	70	80 [b]	–	%
Quiescent current	Burst Mode	–	25	–	µA
	Low Power Burst Mode	–	20	–	µA
	Power Down	–	1	–	µA
Start-up time from power down	–		500	1000	µs
Settling time: burst to PWM mode	Ensure light-load (<30 mA) during mode-change	–	200	400	µs
Settling time: PWM to burst mode	Ensure light-load (<30 mA) during mode-change	–	–	100	µs
Input supply voltage ramp-up time 1 [a]	0 to 4.3V	44	–	–	µs
Input supply voltage ramp-up time 2 [a]	4.3 to 5.5V	100	–	–	µs

a. The 0 to 4.3V and 4.3 to 5Vramp up assumes a Li-ion insertion causing a max ramp slope
b. VBAT=3.3V, Vout=1.5V, fsw=2.76 MHz, inductor DCR=160 mOhms.

BUCK-BOOST REGULATOR

Table 42: Buck-Boost Regulator

Specification	*Notes*	*Minimum*	*Typical*	*Maximum*	*Unit*
Input supply voltage	–	2.3	–	5.5	Volts
PWM mode switching frequency	–	–	1.4		MHz
PWM output current	–	–	–	300	mA
Output voltage range	Programmable, 50 mV steps	2.25	3.3	3.5	Volts
PWM ripple voltage, static	–	–	–	40	mV_{p-p}
PWM ripple voltage, dynamic load	100 mA, 1 µs rise/fall current step	–	–	85	mV_{p-p}
Burst mode ripple voltage, static	–	–	–	80	mV_{p-p}
PWM mode efficiency	200 mA load current	70	86 [b]	–	%
Quiescent current	Burst mode No load	–	30	–	µA
Start-up time from power down	–	–	500	1000	µs
Settling time: Burst-to-PWM mode	Ensure light-load (<30 mA) during mode change	–	200	400	µs
Settling time: PWM-to-Burst mode	Ensure light-load (<30 mA) during mode change	–	–	100	µs
Input supply voltage ramp-up time 1	0 to 4.3V [a]	44	–	–	µs
Input supply voltage ramp up time 2	4.3 to 5.5V [a]	100	–	–	µs

a. The 0 to 4.3V and 4.3 to 5V ramp up assumes a Li-ion insertion causing a max ramp slope.
b. VBAT=3.65V, Vout=3.3V, fsw=1.38 MHz, inductor DCR=156 mOhms.

Section 21: Interface Timing and AC Characteristics

Note: Unless otherwise stated, all specifications in this section apply to the operating temperature and voltage ranges specified in Table 20 and Table 22 on page 76 and Table 23 on page 76. Functional operation outside these limits is not guaranteed.

Bluetooth Peripheral Transport Unit Timing Specifications

This section describes the Peripheral Transport Unit (PTU) timing.

The following conditions apply:

V_{DD} = 3.3V, V_{SS} = 0V, T_A = 0 to 85 °C

Bluetooth UART Timing

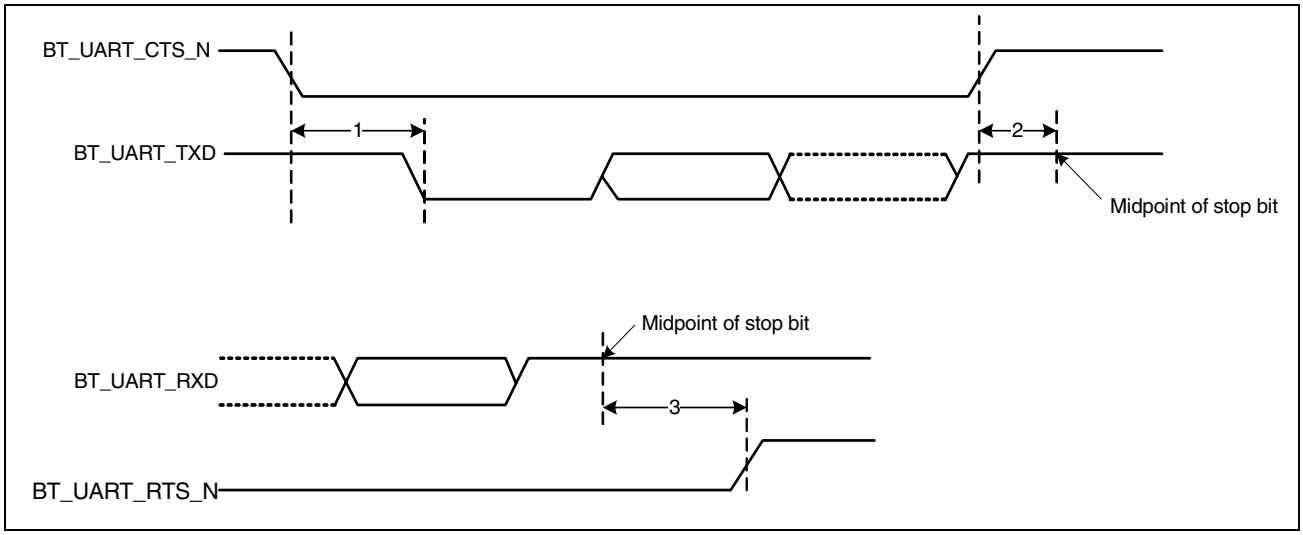


Figure 16: UART Timing

Table 43: UART Timing Speicifications

Reference	Description	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to UART_TXD valid	–	–	24	Baudout cycles
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	10	ns
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	2	Baudout cycles

PCM INTERFACE TIMING

Short Frame Sync, Master Mode

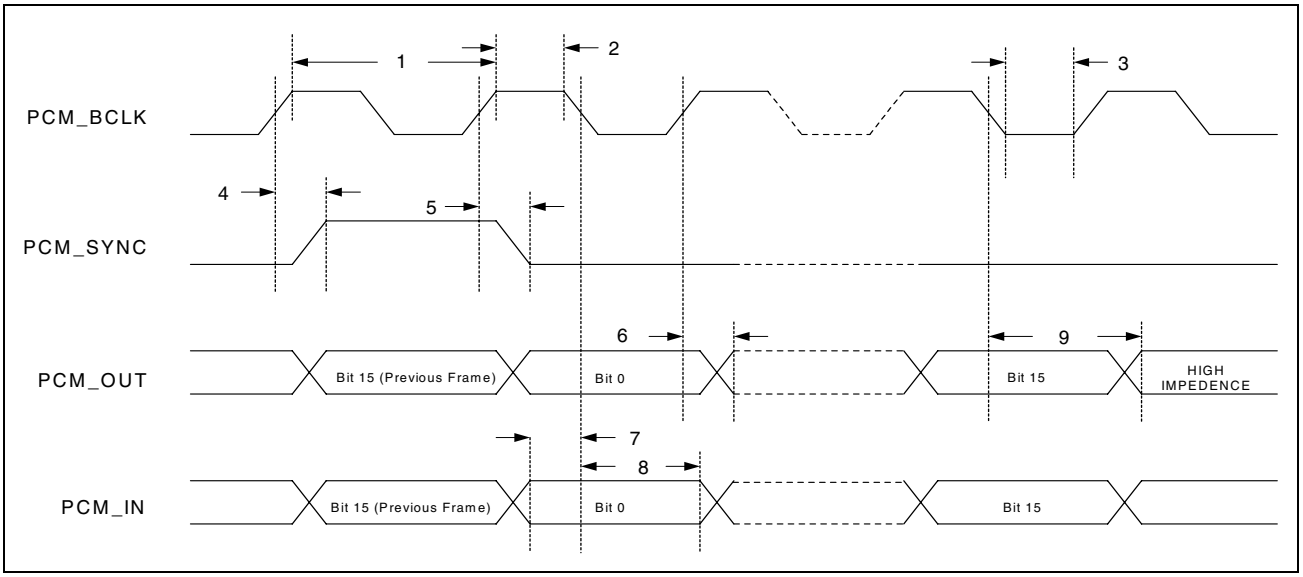


Figure 17: PCM (Short Frame Sync, Master Mode) Timing

Table 44: PCM (Short Frame Sync, Master Mode) Timing Specifications

Reference	*Description*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	128	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC high	–	–	50	ns
5	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC low	–	–	50	ns
6	Delay from BT_PCM_CLK rising edge to data valid on BT_PCM_OUT	–	–	50	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	–	–	50	ns

Short Frame Sync, Slave Mode

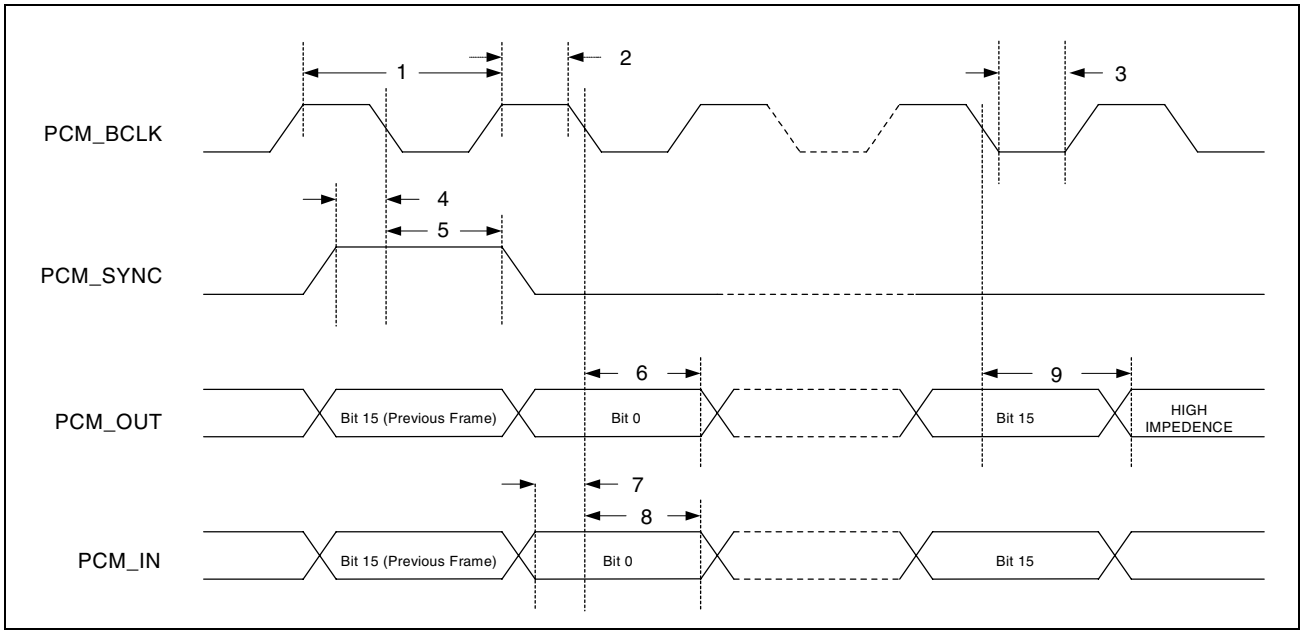


Figure 18: PCM (Short Frame Sync, Slave Mode) Timing

Table 45: PCM (Short Frame Sync, Slave Mode) Timing Specifications

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	209	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Setup time for BT_PCM_SYNC before falling edge of BT_PCM_BCLK	50	–	–	ns
5	Hold time for BT_PCM_SYNC after falling edge of BT_PCM_CLK	10	–	–	ns
6	Hold time of BT_PCM_OUT after BT_PCM_CLK falling edge	–	–	175	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	–	–	100	ns

Long Frame Sync, Master Mode

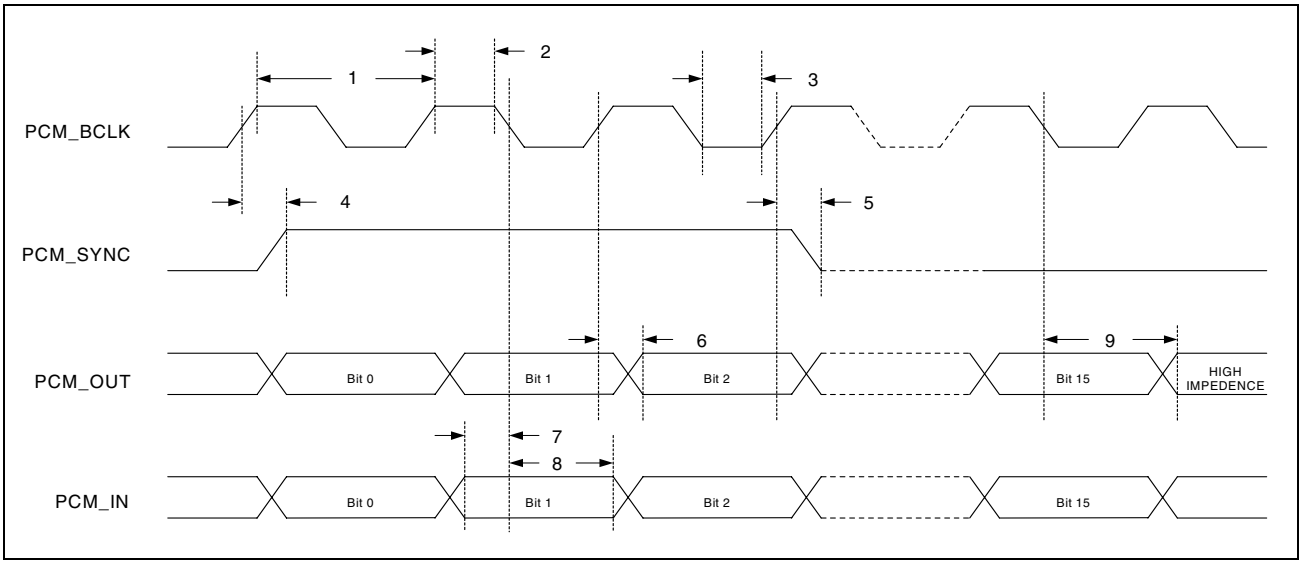


Figure 19: PCM (Long Frame Sync, Master Mode) Timing

Table 46: TPCM (Long Frame Sync, Master Mode) Timing Specifications

Reference	*Description*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	209	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC high during first bit time	–	–	50	ns
5	Delay from BT_PCM_CLK rising edge to BT_PCM_SYNC low during third bit time	–	–	50	ns
6	Delay from BT_PCM_CLK rising edge to data valid on BT_PCM_OUT	–	–	50	ns
7	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns
8	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
9	Delay from falling edge of BT_PCM_CLK during last bit period to BT_PCM_OUT becoming high impedance	–	–	50	ns

Long Frame Sync, Slave Mode

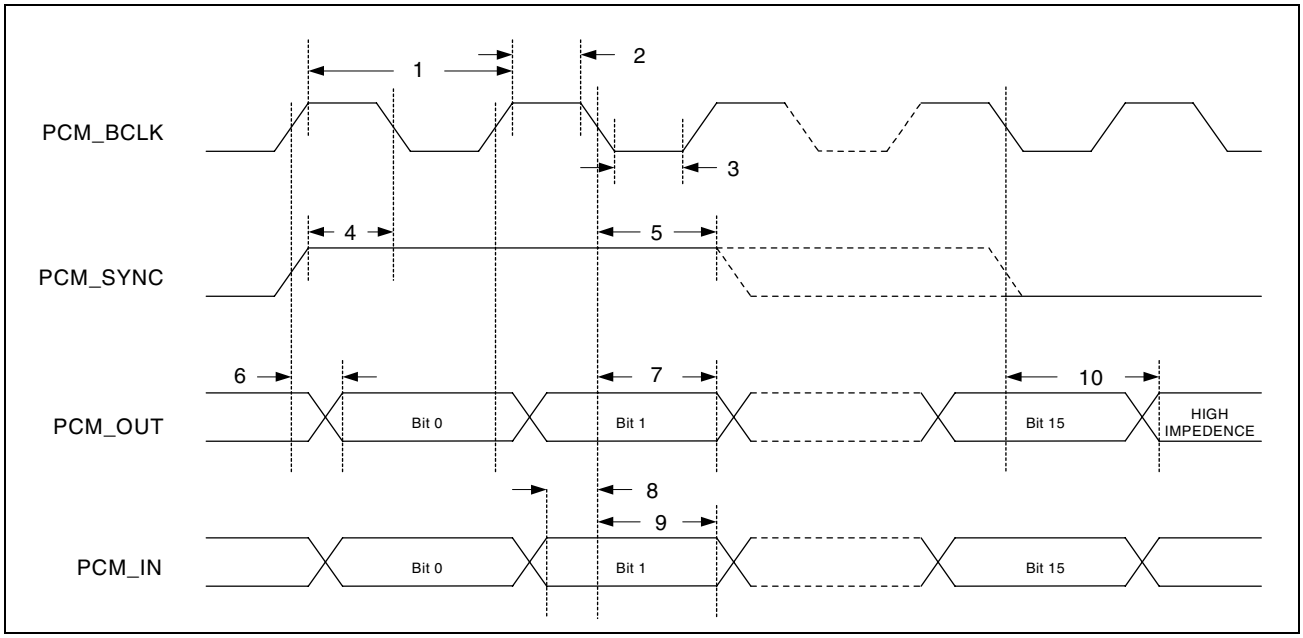


Figure 20: PCM (Long Frame Sync, Slave Mode) Timing

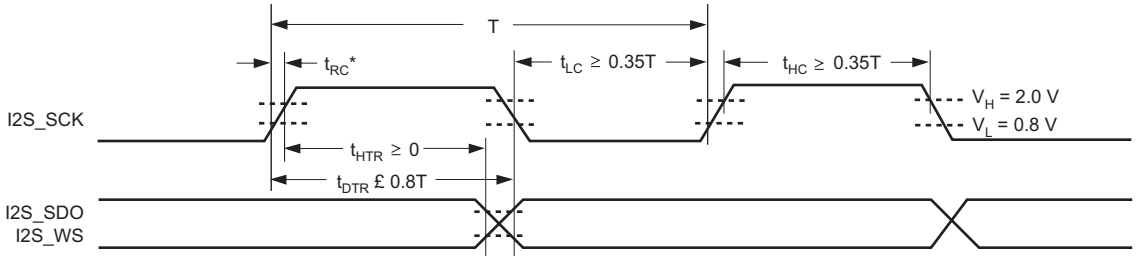
Table 47: PCM (Long Frame Sync, Slave Mode) Timing Specifications

Reference	Description	Min	Typ	Max	Unit
1	PCM bit clock frequency	128	–	2048	kHz
2	PCM bit clock high time	209	–	–	ns
3	PCM bit clock low time	209	–	–	ns
4	Setup time for BT_PCM_SYNC before falling edge of BT_PCM_CLK during first bit time	50	–	–	ns
5	Hold time for BT_PCM_SYNC after falling edge of BT_PCM_CLK during second bit period. (BT_PCM_SYNC may go low any time from second bit period to last bit period)	10	–	–	ns
6	Delay from rising edge of BT_PCM_CLK or BT_PCM_SYNC (whichever is later) to data valid for first bit on BT_PCM_OUT	–	–	50	ns
7	Hold time of BT_PCM_OUT after BT_PCM_CLK falling edge	–	–	175	ns
8	Setup time for BT_PCM_IN before BT_PCM_CLK falling edge	50	–	–	ns
9	Hold time for BT_PCM_IN after BT_PCM_CLK falling edge	10	–	–	ns
10	Delay from falling edge of BT_PCM_CLK or BT_PCM_SYNC (whichever is later) during last bit in slot to BT_PCM_OUT becoming high impedance	–	–	100	ns

FM I²S TIMING

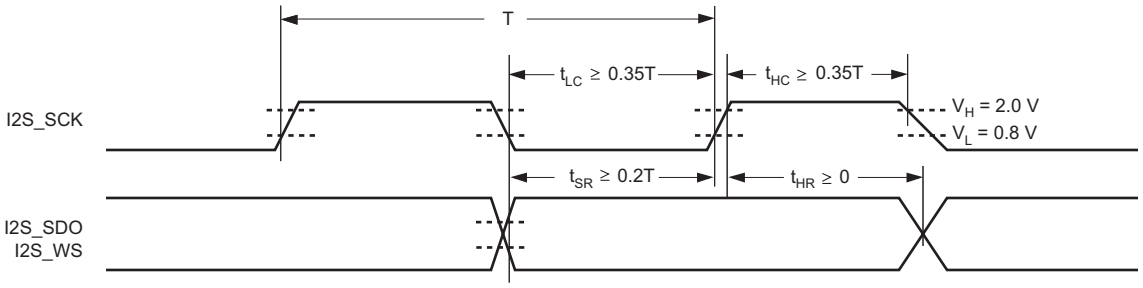
The timing illustrated in Figure 21 and Figure 22 are described in Table 48 on page 102.

Note: The times given in Figure 21 and Figure 22 are determined by the transmitter speed. The specification of the receiver must be capable of matching the performance of the transmitter.



Notes:
T = clock period
T_{TR} = minimum allowed clock period for transmitter
$T > T_{TR}$
* t_{RC} is only relevant for transmitters in slave mode.

Figure 21: I²S Transmitter Timing



Notes:
T= Clock period
T_R = Minimum allowed clock period for transmitter
$T > T_R$

Figure 22: I²S Receiver Timing

Table 48: Timing for I²S Transmitters and Receivers[a]

Parameter	Transmitter				Receiver				Notes
	Lower LImit		Upper Limit		Lower Limit		Upper Limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T[b]	T_{TR}	–	–	–	T_r	–	–	–	a
Master Mode: Clock generated by transmitter or receiver[c]									
High t_{HC}	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	–	b
Low t_{LC}	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	–	b
Slave Mode: Clock accepted by transmitter or receiver[d]									
High t_{HC}	–	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	c
Low t_{LC}	–	$0.35T_{TR}$	–	–	–	$0.35T_{TR}$	–	–	c
Rise-time t_{RC}	–	–	$0.15T_{TR}$	–	–	–		–	d
Transmitter									
Delay t_{DTR}[e]	–	–	–	0.8T	–	–	–	–	e
Hold time t_{HTR}	0	–	–	–	–	–	–	–	d
Receiver[f]									
Setup time t_{SR}	–	–	–	–	–	$0.2T_R$	–	–	f
Hold time t_{HR}	–	–	–	–	–	0	–	–	f

a. All timing values are specified with respect to high and low threshold levels.
b. The system clock period T must be greater than T_{TR} and T_r because both the transmitter and receiver must be able to handle the data transfer rate.
c. The transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason t_{HC} and t_{LC} are specified with respect to T.
d. The transmitter and receiver need a clock signal with minimum high and low periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_R$, any clock that meets the requirements can be used.
e. Because the delay (t_{DTR}) and the maximum transmitter speed (defined by T_{TR}) are related, a fast transmitter driven by a slow clock edge can result in t_{DTR} not exceeding t_{RC} which means t_{HTR} becomes zero or negative. Therefore, the transmitter has to guarantee that t_{HTR} is greater than or equal to zero, provided the clock rise-time t_{RC} is not more than t_{RCmax}, where t_{RCmax} is not less than $0.15T_{TR}$. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
f. The data setup and hold time must not be less than the specified receiver setup and hold time.

FM I²C-COMPATIBLE TIMING

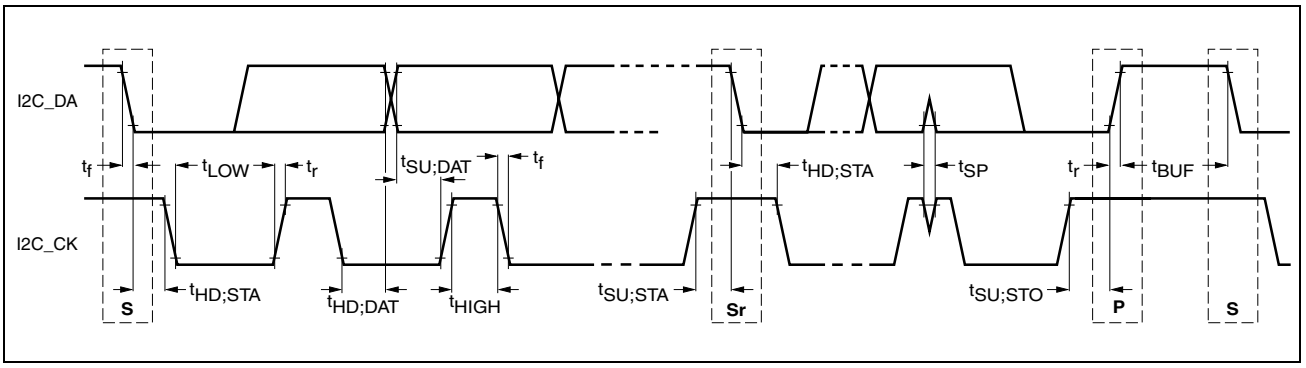


Table 49: FM I2C-Compatible Interface Timing

Parameter	*Symbol*	*Minimum*	*Maximum*	*Unit*
I2C_CK clock frequency	f_{I2C_CK}	0	400	kHz
Bus-free times between a stop and start condition	t_{BUF}	1.3	–	µs
Hold time (repeated) start condition. After this period, the first clock pulse is generated.	$t_{HD,STA}$	0.6	–	µs
Low period of the I2C_CK clock	t_{LOW}	1.3	–	µs
High period of the I2C_CK clock	t_{HIGH}	0.6	–	µs
Setup time for a repeater start condition	$t_{SU,STA}$	0.6	–	µs
Data hold time	$t_{HD,DAT}$	0	0.9	µs
Data setup time	$t_{SU,DAT}$	–	–	µs
Rise time of both I2C_DA and I2C_CK signals	t_r	$20 + 0.1C_b$[a]	300	ns
Fall time of both I2C_DA and I2C_CK signals	t_r	$20 + 0.1C_b$[a]	300	ns
Setup time for stop condition	$t_{SU,STO}$	0.6	–	µs

a. C_b = Total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.

SPROM TIMING

Table 50: SPROM Timing Characteristics

Signal Name	*Period*	*Output Max*	*Output Min*	*Setup*	*Hold*
SPROM_CLK	1.92 µs	–	–	–	–
SPROM_CLK falling edge to SPROM_DOUT	–	0.5 µs	0.3 µs	–	–
SPROM_CLK falling edge to SPROM_CS	–	0.5 µs	0.3 µs	–	–
SPROM_CLK rising edge to SPROM_DIN	–	–	–	0.5 µs	–0.3 µs

JTAG TIMING

Table 51: JTAG Timing Characteristics

Signal Name	Period	Output Max	Output Min	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–	–	–	20 ns	0 ns
TMS	–	–	–	20 ns	0 ns
TDO	–	100 ns	0 ns	–	–
JTAG_TRST	250 ns	–	–	–	–

SDIO TIMING

This section describes the SDIO timing in both default and high-speed modes.

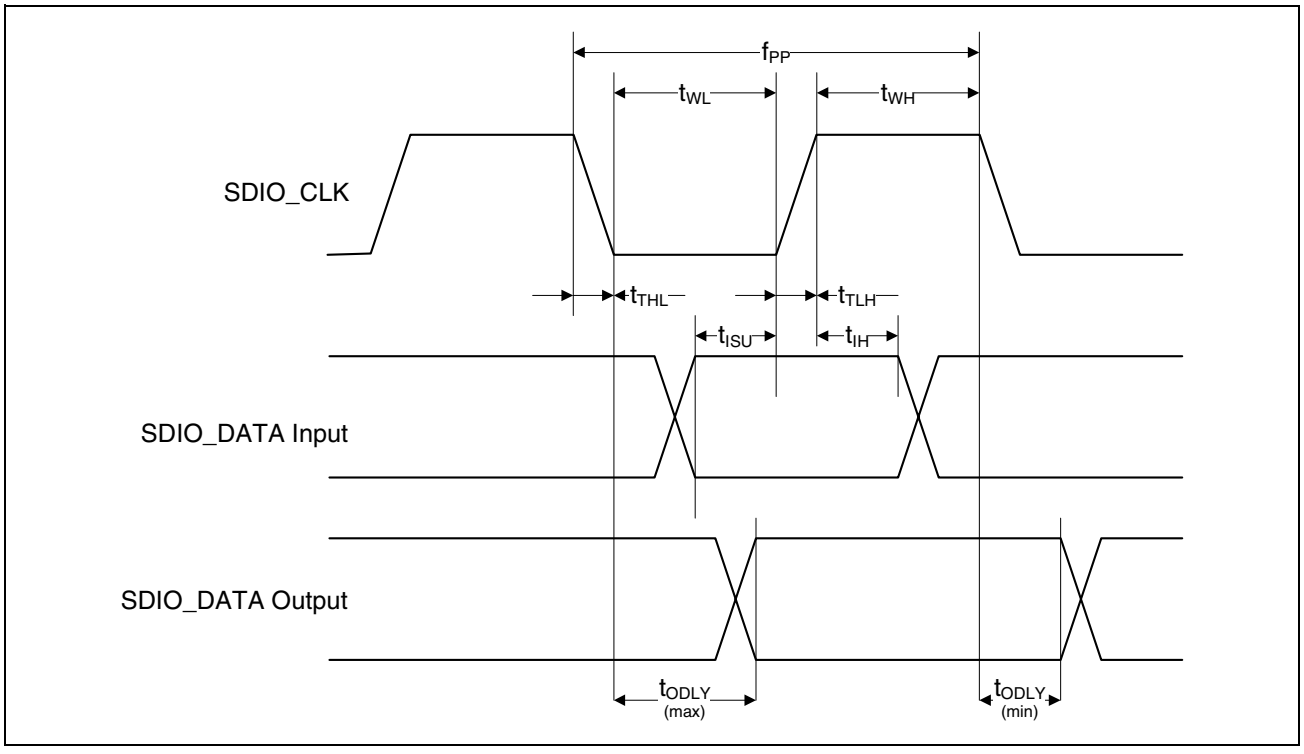


Figure 23: SDIO Bus Timing (Default Mode)

Table 52: SDIO Bus Timing [a] Parameters (Default Mode)

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
Clock: SDIO_CLK (All values are referred to min. VIH and max. VIL[b])					
Frequency—Data Transfer Mode	fPP	0	–	25	MHz
Frequency—Identification Mode	fOD	0	–	400	kHz
Clock Low Time	tWL	10	–	–	ns
Clock High Time	tWH	10	–	–	ns
Clock Rise time	tTLH	–	–	10	ns
Clock Low Time	tTHL	–	–	10	ns
Inputs: CMD, DATA (referenced to SDIO_CLK)					
Input Setup Time	tISU	5	–	–	ns
Input Hold Time	tIH	5	–	–	ns
Outputs: CMD, DATA (referenced to SDIO_CLK)					
Output Delay time—Data Transfer Mode	tODLY	0	–	14	ns
Output Delay time—Identification Mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min (Vih) = 0.7*Vdd and max (Vil) = 0.2*Vdd

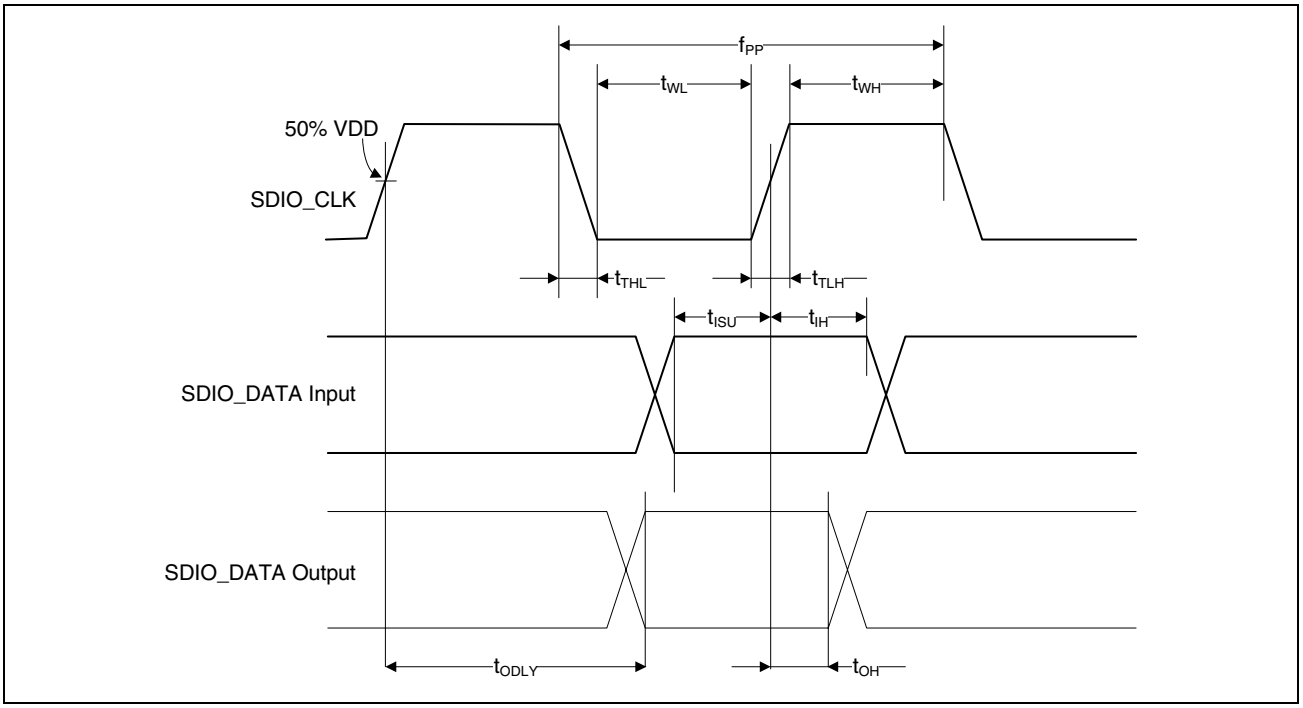


Figure 24: SDIO Bus Timing (High-Speed Mode)

Table 53: SDIO Bus Timing [a] Parameters (High-Speed Mode)

Parameter	*Symbol*	*Min*	*Typical*	*Max*	*Unit*
Clock: SDIO_CLK (all values are referred to min. VIH and max. VIL [b])					
Frequency—Data Transfer Mode	fPP	0	–	50	MHz
Frequency—Identification Mode	fOD	0	–	400	kHz
Clock Low Time	tWL	7	–	–	ns
Clock High Time	tWH	7	–	–	ns
Clock Rise time	tTLH	–	–	3	ns
Clock Low Time	tTHL	–	–	3	ns
Inputs: CMD, DATA (referenced to SDIO_CLK)					
Input Setup Time	tISU	6	–	–	ns
Input Hold Time	tIH	2	–	–	ns
Outputs: CMD, DATA (referenced to SDIO_CLK)					
Output Delay time—Data Transfer Mode	tODLY	–	–	14	ns
Output Hold time	tOH	2.5	–	–	ns
Total System Capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. Minimum (Vih) = 0.7*Vdd and maximum (Vil) = 0.2*Vdd

Section 22: Power-Up Sequence and Timing

SDIO Host Timing Requirement

The SDIO host must wait a minimum of 150 ms before initiating access to the BCM4325 after the VDDC (1.25V DC supply for core) ramps up and settles. The specifics of this requirement depend on the power supply topology being used. For example, if the topology shown in Figure 5 on page 4 is being used, reset and host access timing depends on the CLDO and CBUCK outputs and the VDDC's bypass network. For an additional safety margin, a longer delay should be used.

Reset and Regulator Control Signal Sequencing

The BCM4325 has four signals (see Table 54) that enable or disable the Bluetooth, WLAN, and internal regulator blocks, allowing the host to control power consumption. This section contains detailed timing diagrams of these signals and the required power-up sequences. These timing diagrams are provided to illustrate proper sequencing of the signals in various operational states. The timing values indicated in the diagrams are the minimum requirements. Longer delays are also acceptable.

Table 54: Control Signal Descriptions

Signal	*Description*
WL_REG_ON	This signal is used by the PMU (along with BT_REG_ON) to decide whether or not to power down the internal BCM4325 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled. If WL_RST_N is low (regardless of BT_RST_N state), the WLAN core will be powered off.
BT_REG_ON	This signal is used by the PMU (along with WL_REG_ON) to decide whether or not to power down the internal BCM4325 regulators. If BT_REG_ON and WL_REG_ON are low, the regulators will be disabled.
WL_RST_N	Low Asserting Reset for WLAN Core This pin must be driven high or low (not left floating).
BT_RST_N	Low asserting reset for Bluetooth core. This pin must be driven high or low (not left floating)

Note: WL_REG_ON and BT_REG_ON are OR gated together in the BCM4325.

SIGNAL AND POWER-UP SEQUENCE TIMING DIAGRAMS

Note: The timing diagrams presented in this section are not to scale and are for illustrative purposes only.

The timing diagrams show the signals going high at the same time (which is true when both REG signals are controlled by a single host GPIO). However, if two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), only one signal has to be high in order to enable the BCM4325's regulators. Additionally, the reset requirements for the Bluetooth core also apply to the FM core. Therefore, if FM is to be used, the Bluetooth core must be enabled.

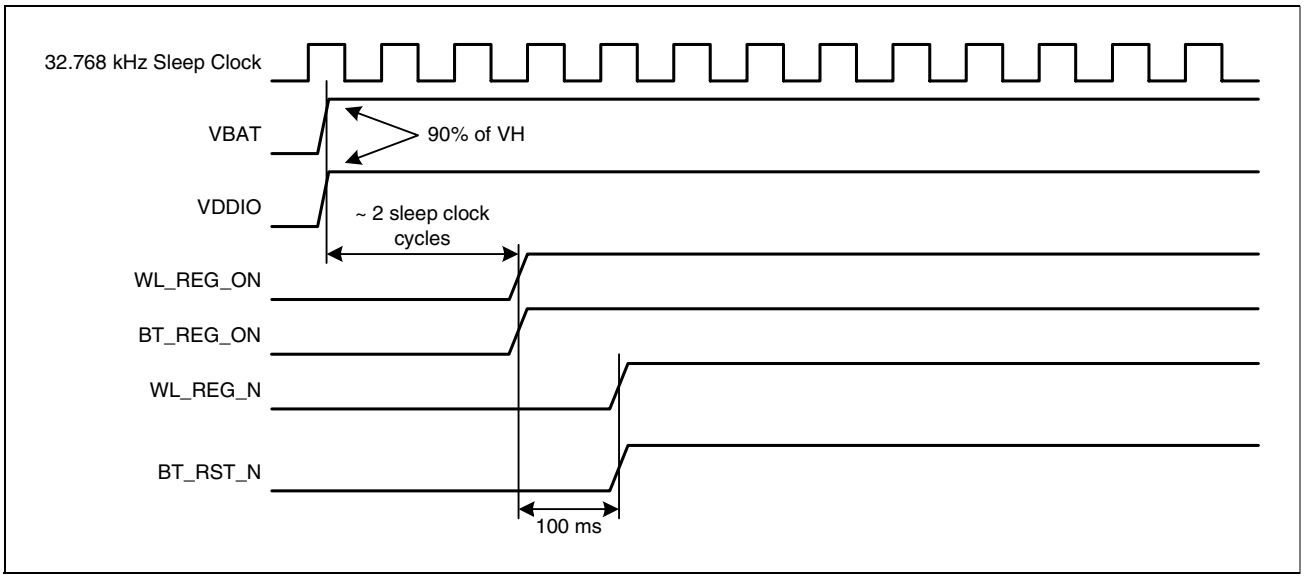


Figure 25: Power-Up Timing for WL On and BT On

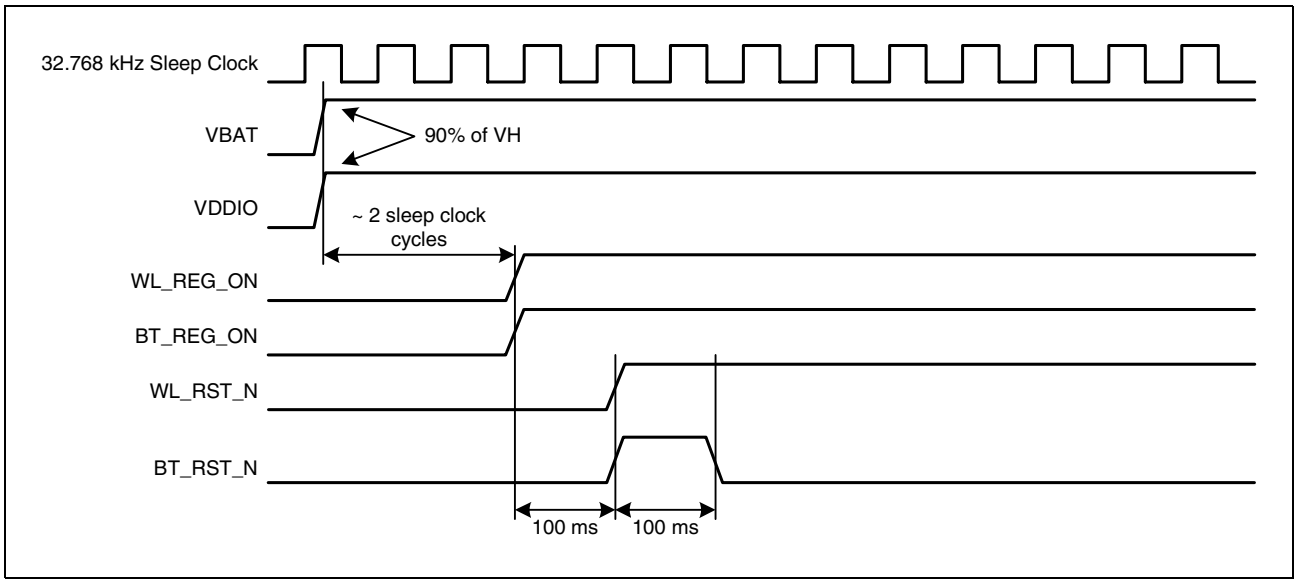


Figure 26: Power-Up Timing for WL On and BT Off

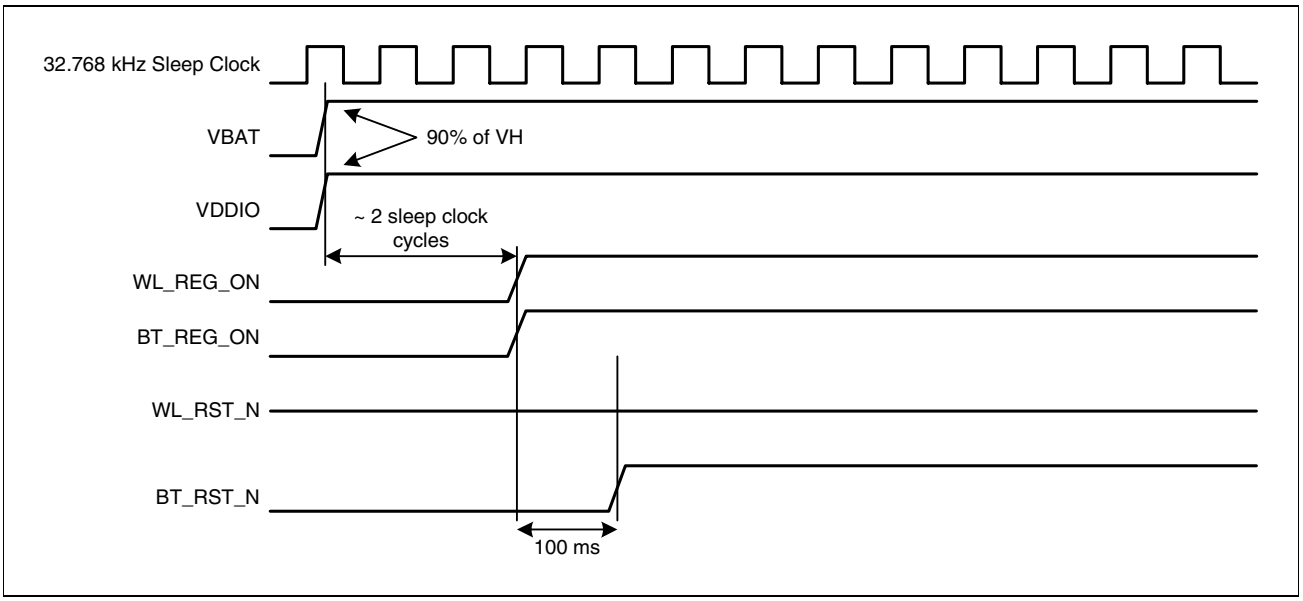


Figure 27: Power-Up Timing for WL Off and BT On

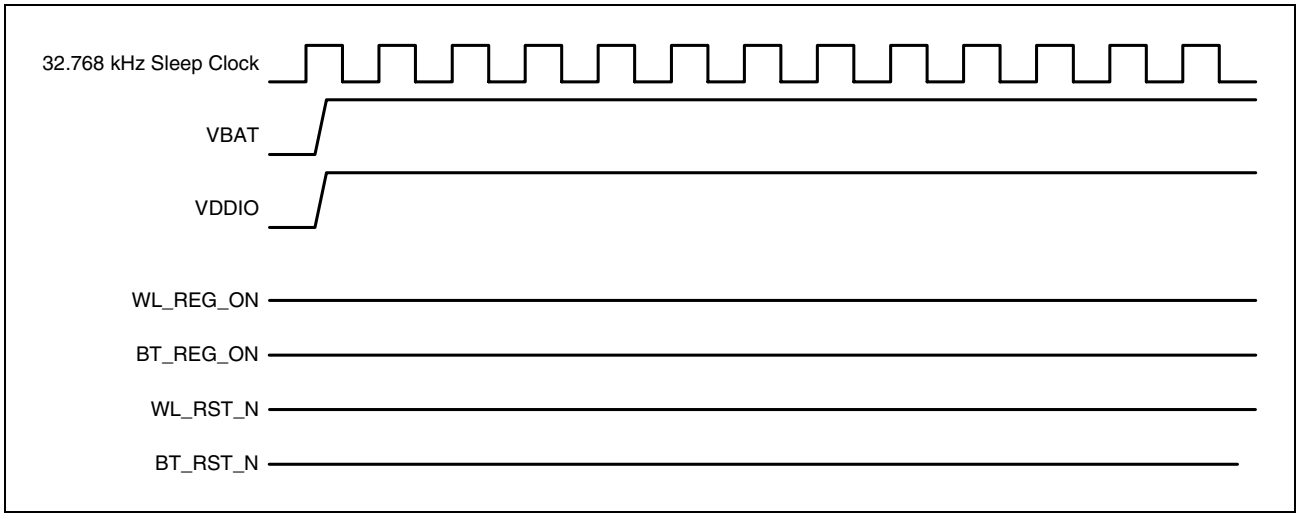


Figure 28: Power-Up Timing for WL Off and BT Off (VDDC Provided by BCM4325)

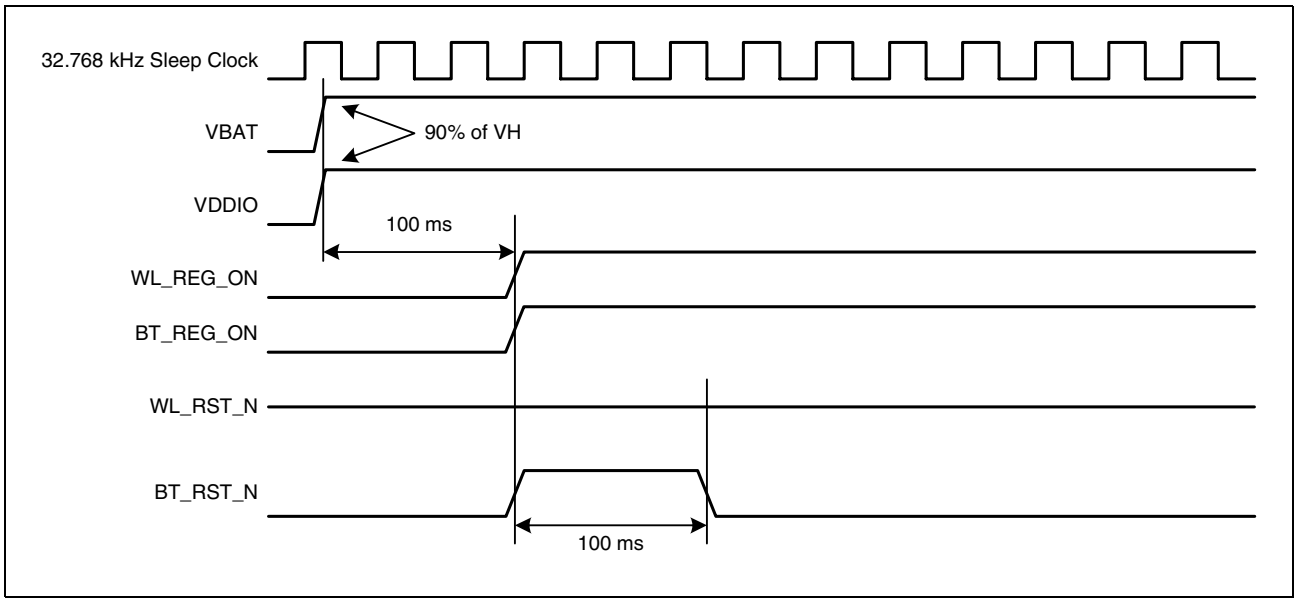


Figure 29: Power-Up Timing for WL Off and BT Off (VDDC Provided Externally)

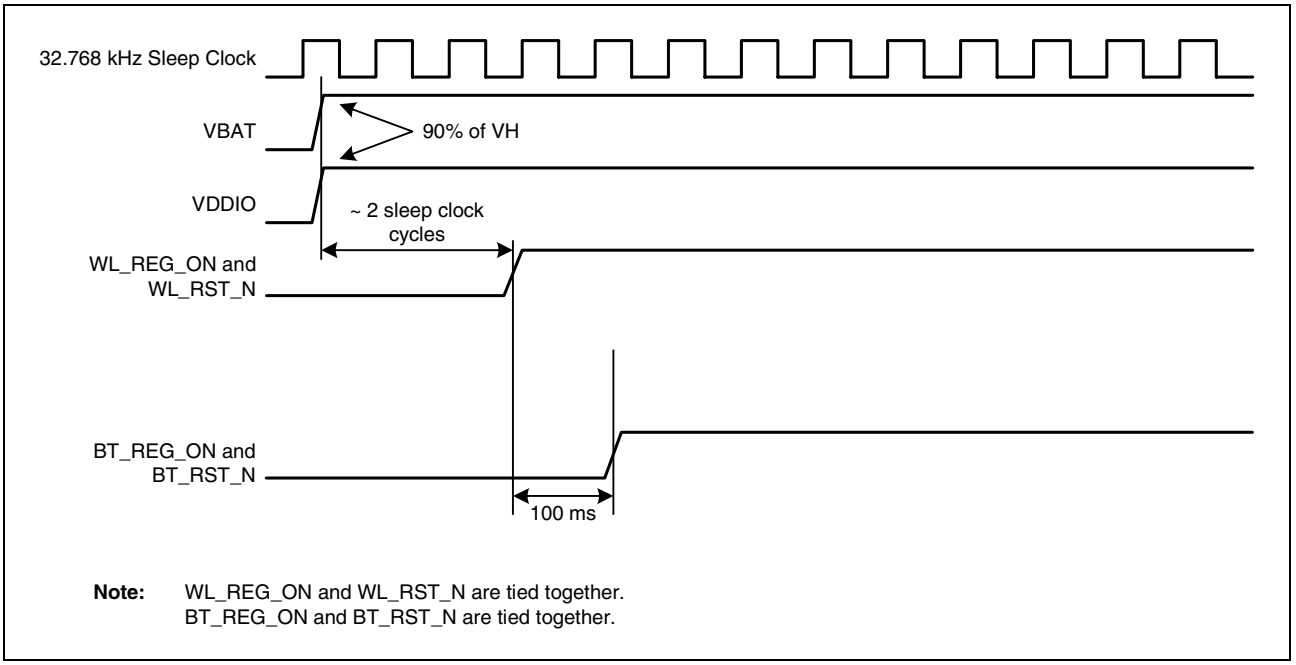
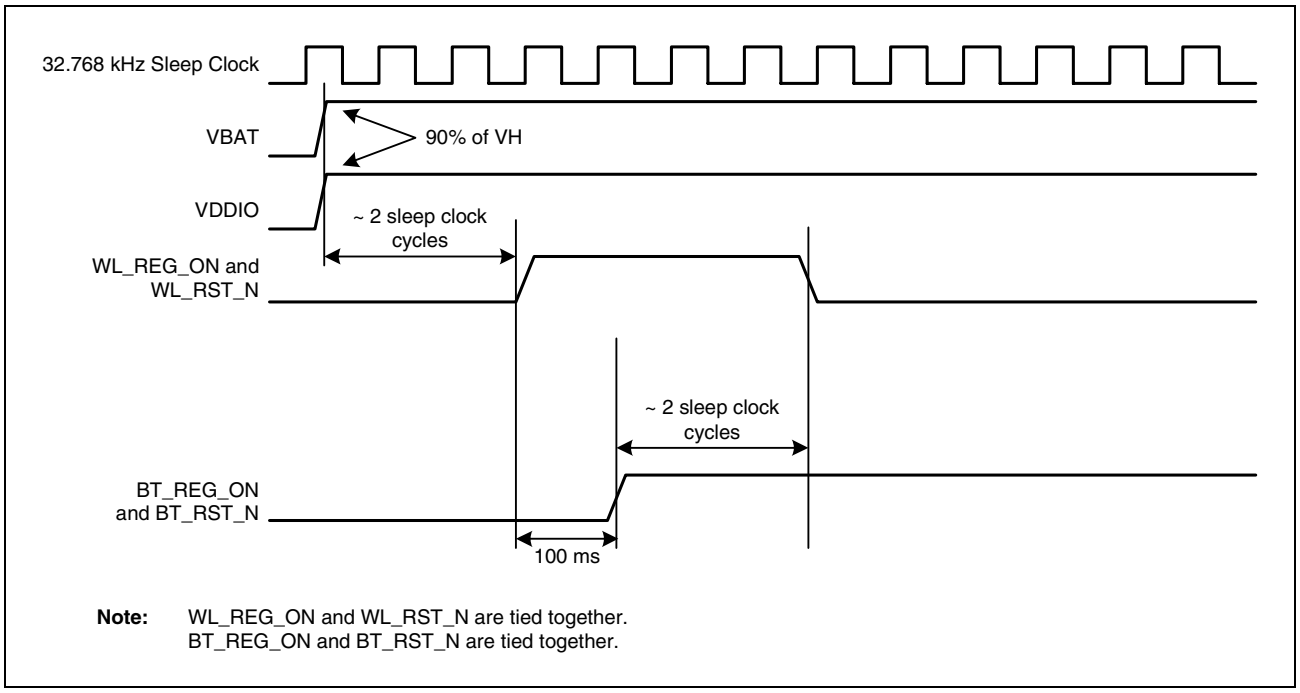
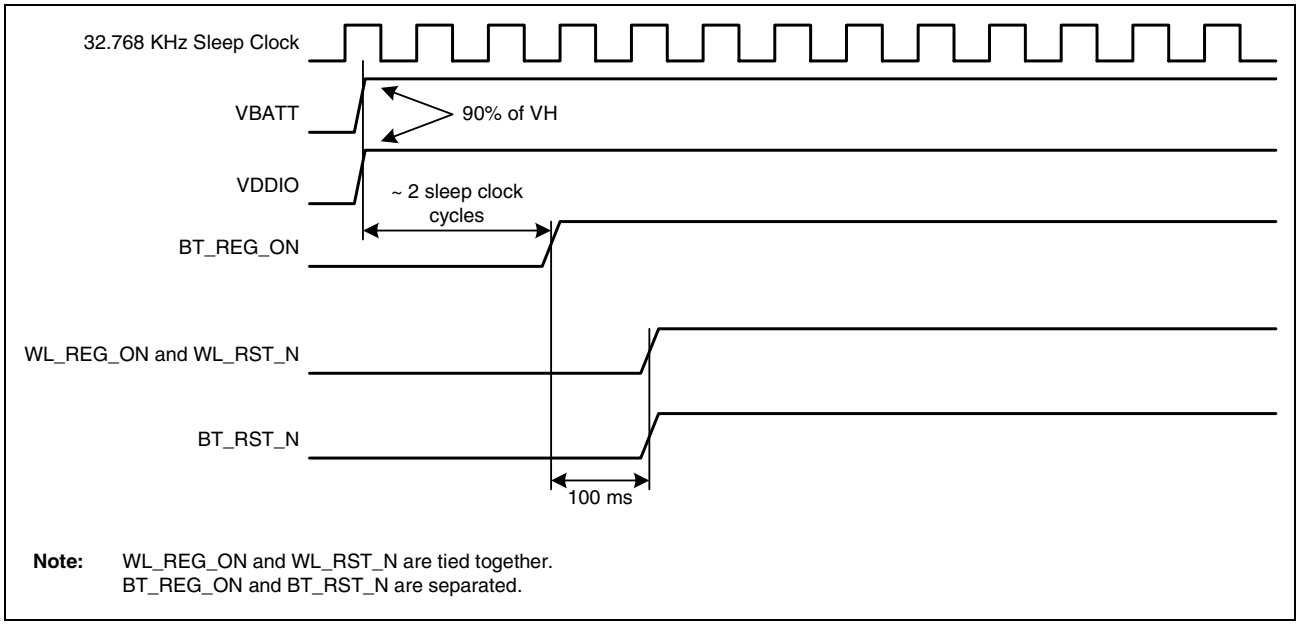


Figure 30: Power-Up Timing for WL On and BT On (REG_ON signals are connected to RST_N signals)



Note: WL_REG_ON and WL_RST_N are tied together.
BT_REG_ON and BT_RST_N are tied together.

Figure 31: Power-Up Timing for WL Off and BT On (REG_ON signals are connected to RST_N signals)



Note: WL_REG_ON and WL_RST_N are tied together.
BT_REG_ON and BT_RST_N are separated.

Figure 32: Power-Up Timing for WL ON and BT ON (WL REG_ON signal connected to WL_RST_N, BT separated)

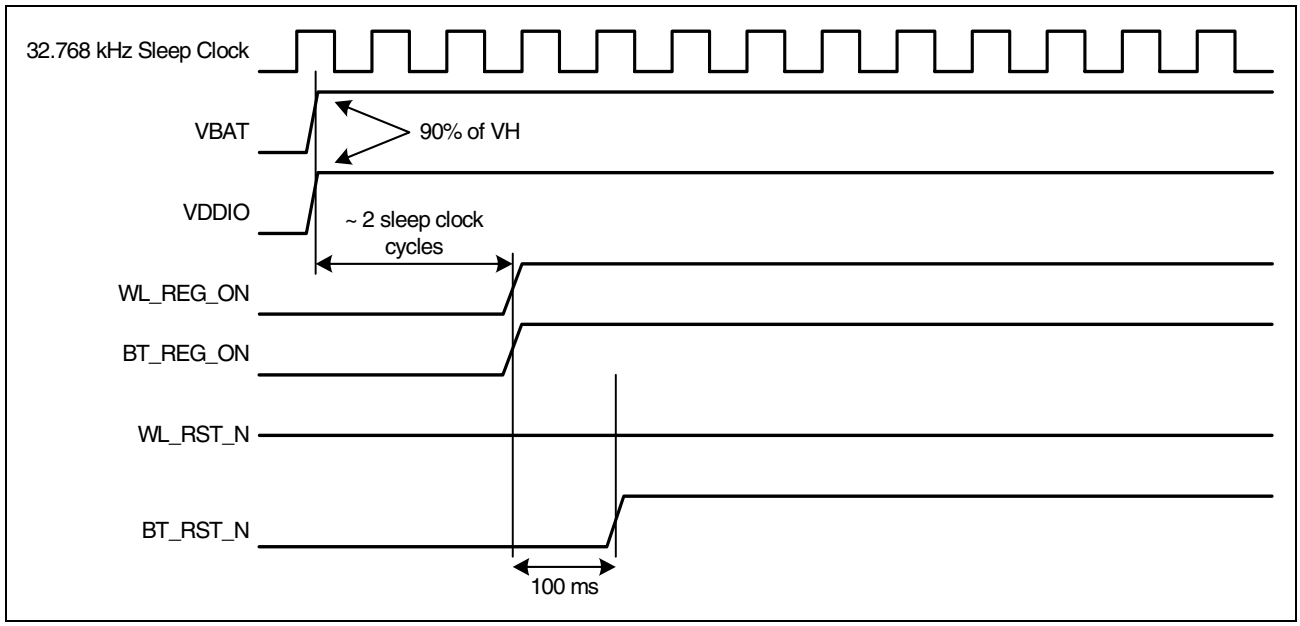


Figure 33: Power-Up Timing for WL OFF and BT ON (WL REG_ON signal connected to WL_RST_N, BT separated)

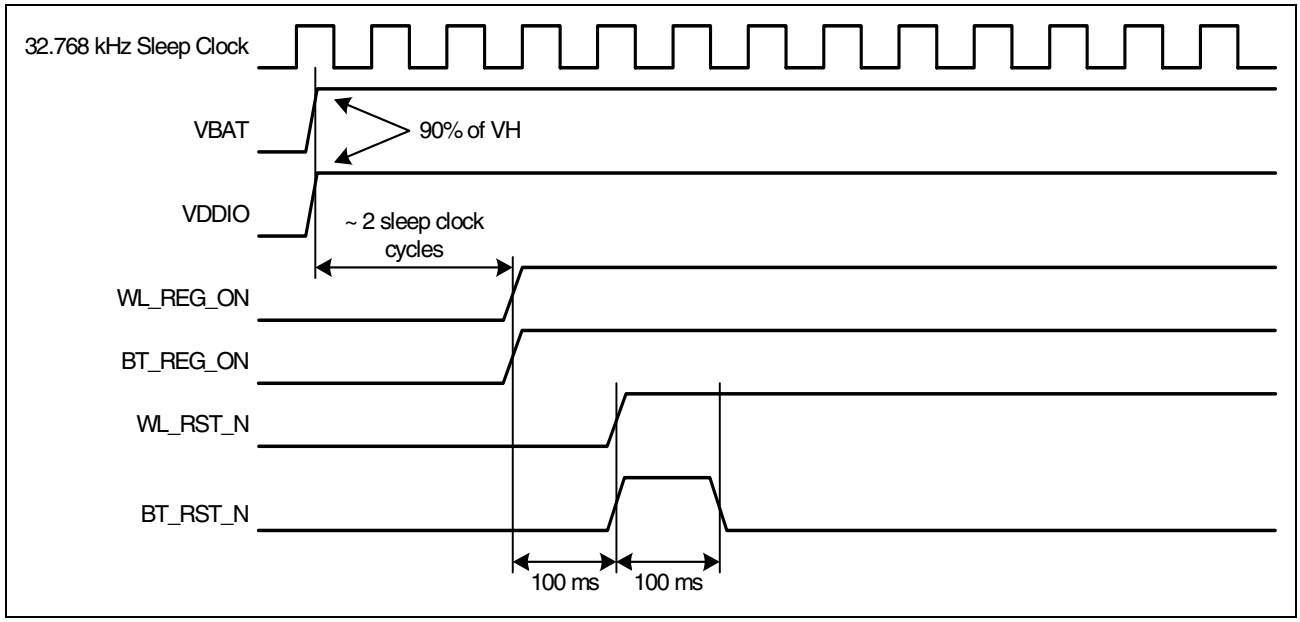


Figure 34: Power-Up Timing for WL ON and BT OFF (WL REG_ON signal connected to WL_RST_N, BT separated)

Section 23: Package Information

Package Thermal Characteristics

Table 55: Thermal Characteristics (Values in Still Air) [a]

Characteristic	*196-Ball FBGA Package*	*339-WLCSP Package*
θ_{JA} (°C/W)	36.3	36.7
θ_{JB} (°C/W)	4.9	1.23
θ_{JC} (°C/W)	10.9	0.06
Ψ_{JT} (°C/W)	0.27	0.27
Maximum Junction Temperature T_j (°C)	125	125

a. No heat sink, TA = 70° C. This is an estimate based on a 2-layer PCB and P = 1.2W continuous dissipation.

Junction Temperature Estimation and PSI_{JT} Versus $THETA_{JC}$

Package thermal characterization parameter PSI-J_T (Ψ_{JT}) yields a better estimation of actual junction temperature (T_J) versus using the junction-to-case thermal resistance parameter Theta-J_C (θ_{JC}). The reason for this is θ_{JC} assumes that all the power is dissipated through the top surface of the package case. In actual applications, some of the power is dissipated through the bottom and sides of the package. Ψ_{JT} takes into account power dissipated through the top, bottom. and sides of the package. The equation for calculating the device junction temperature is as follows:

$$T_J = T_T + P \times \Psi_{JT}$$

Where:

- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

Environmental Characteristics

For environmental characteristics data, see "Environmental Ratings" on page 76.

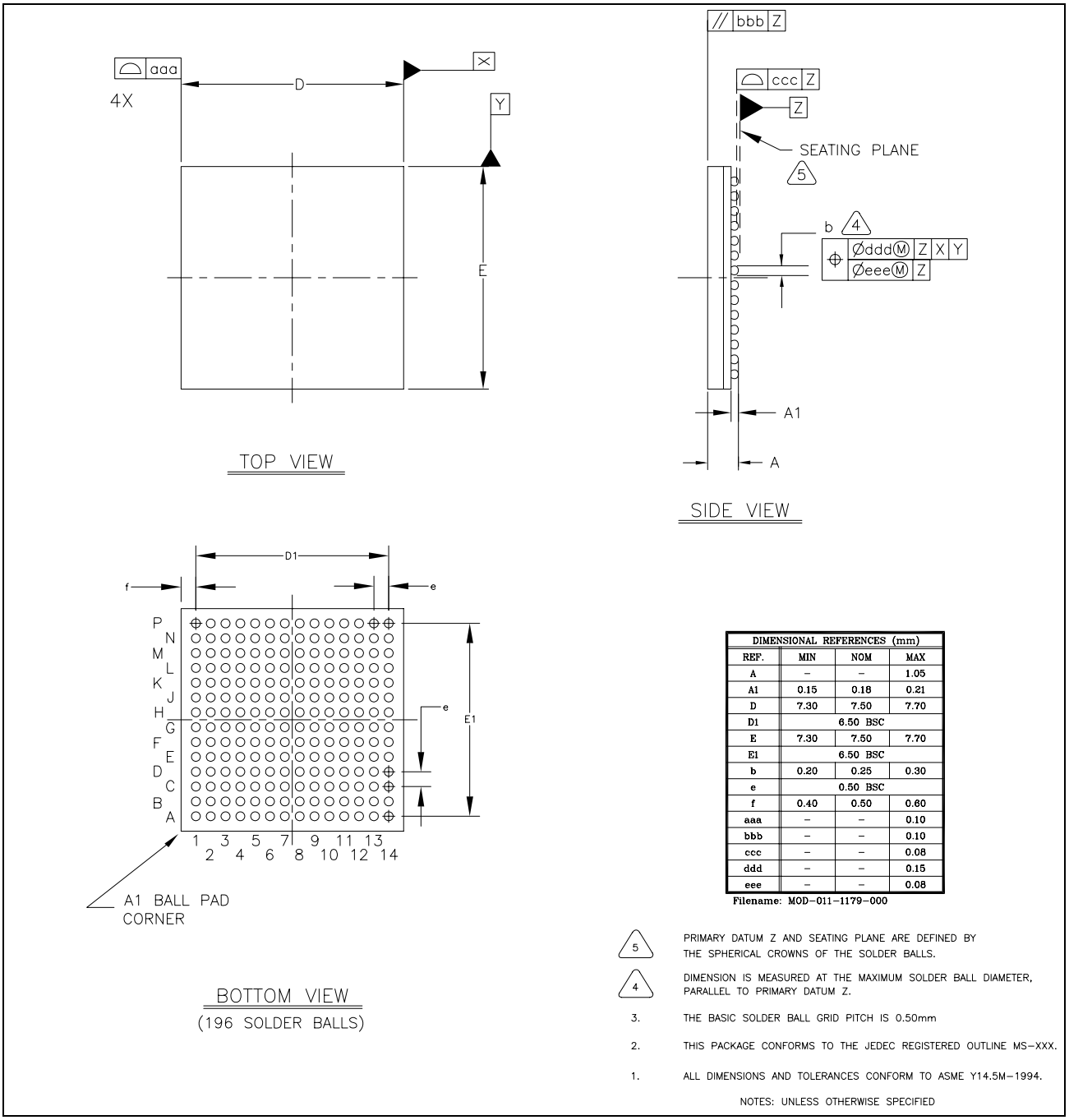
MISCELLANEOUS CHARACTERISTICS

Table 56: Miscellaneous Characteristics

Characteristics	Value	Units	Conditions/Comments
Moisture Sensitivity Level (MSL)	3	–	–
Ball Metallurgy	SnAg1.0Cu0.5	–	–
Under bump Metallurgy	E'lytic Ti/Cu/Ni	–	–
With bump Metallurgy	SnCu2.5	–	–
FBGA peak reflow temperature	260	^{o}C	–

Section 24: Mechanical Information

196-BALL FBGA PACKAGE



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	1.05
A1	0.15	0.18	0.21
D	7.30	7.50	7.70
D1		6.50 BSC	
E	7.30	7.50	7.70
E1		6.50 BSC	
b	0.20	0.25	0.30
e		0.50 BSC	
f	0.40	0.50	0.60
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.15
eee	–	–	0.08

Filename: MOD-011-1179-000

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BALL GRID PITCH IS 0.50mm

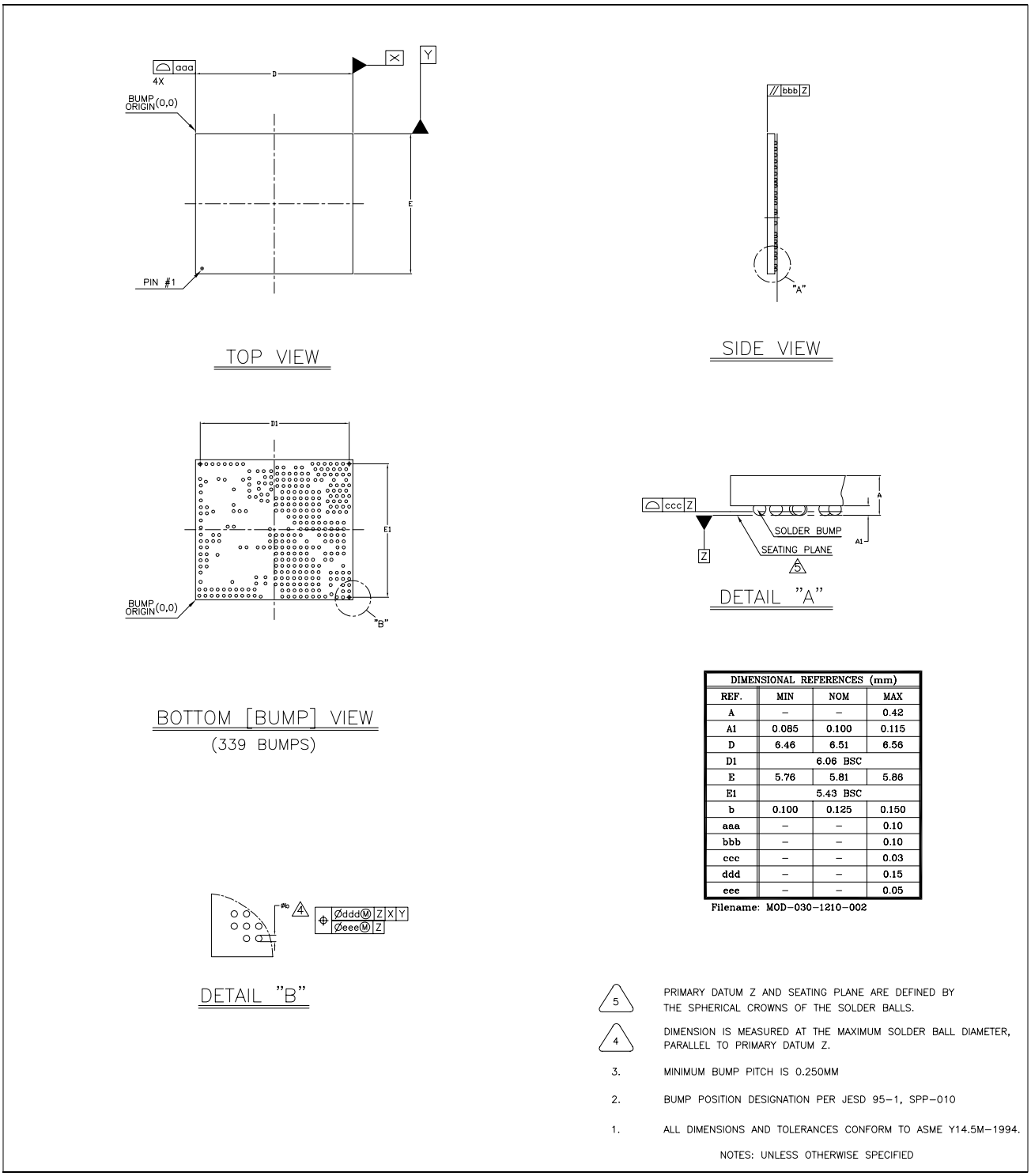
2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MS-XXX.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 35: 196-Ball FBGA Mechanical Information

339-PIN WLCSP PACKAGE



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	–	–	0.42
A1	0.085	0.100	0.115
D	6.46	6.51	6.56
D1		6.06 BSC	
E	5.76	5.81	5.86
E1		5.43 BSC	
b	0.100	0.125	0.150
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.03
ddd	–	–	0.15
eee	–	–	0.05

Filename: MOD-030-1210-002

Figure 36: 339-Pin WLCSP Mechanical Information

Section 25: WLCSP Keepout Area

This section shows the PCB keepout areas of theBCM4325 WLCSP package; there should not be any metal on these layers.

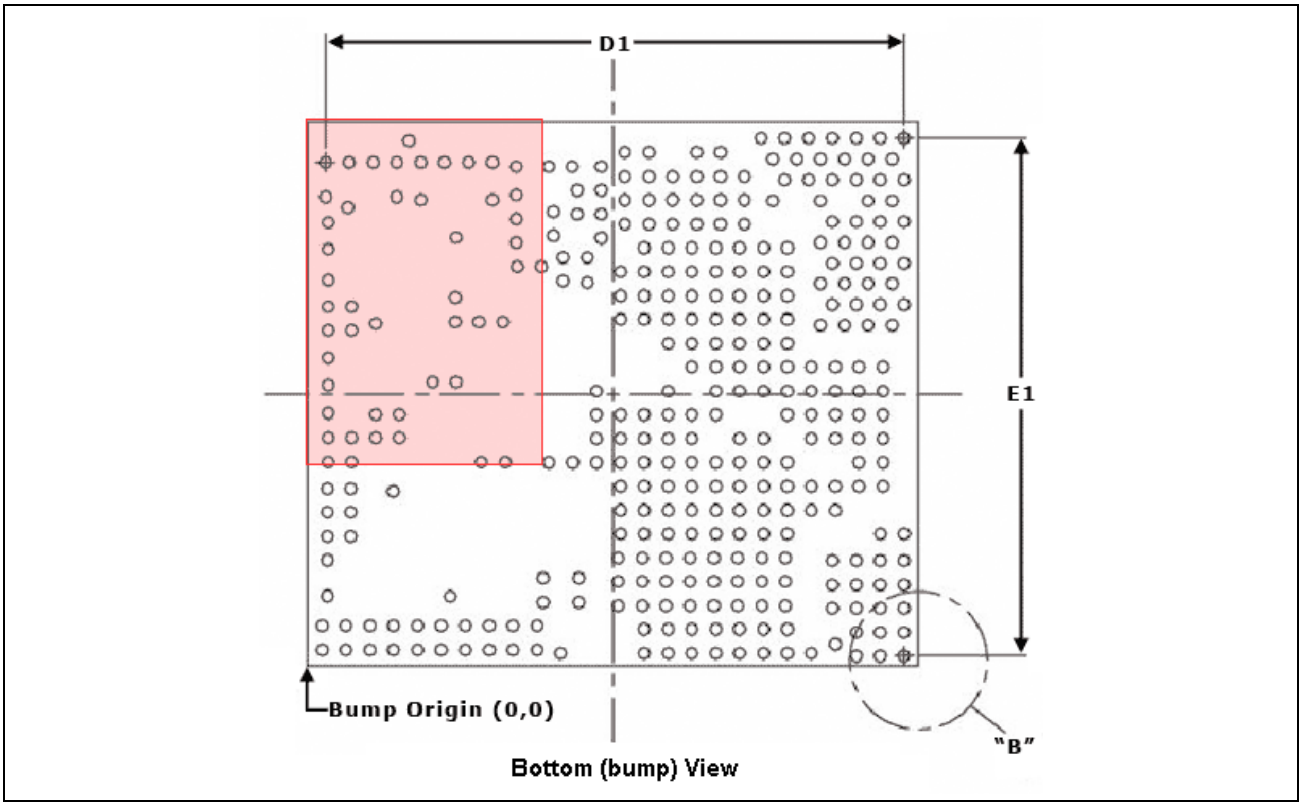


Figure 37: WLAN Section Top Metal Keepout Area

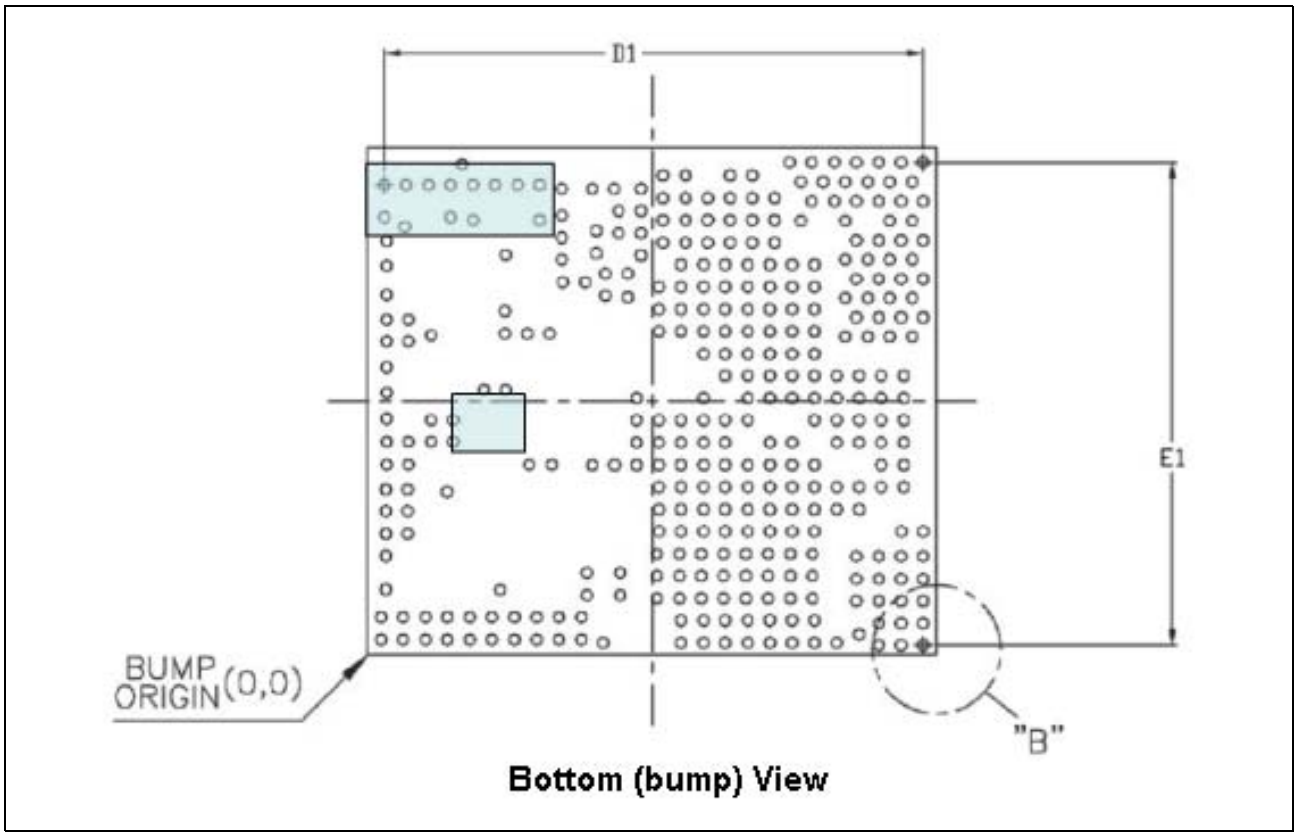


Figure 38: WLAN Section Second Metal Keepout Area

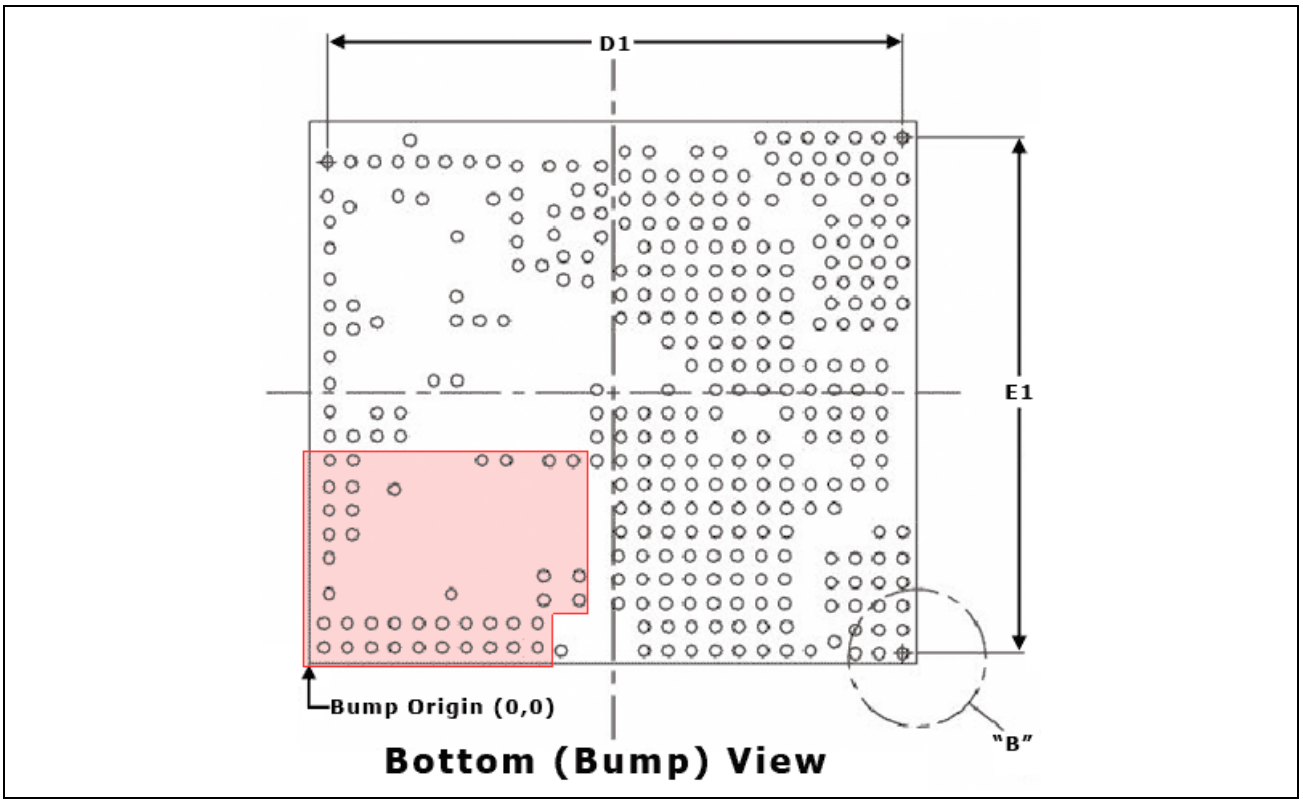


Figure 39: BT and FM Keepout Area

Note: The shaded area in Figure 39 is enlarged in Figure 40 on page 119.

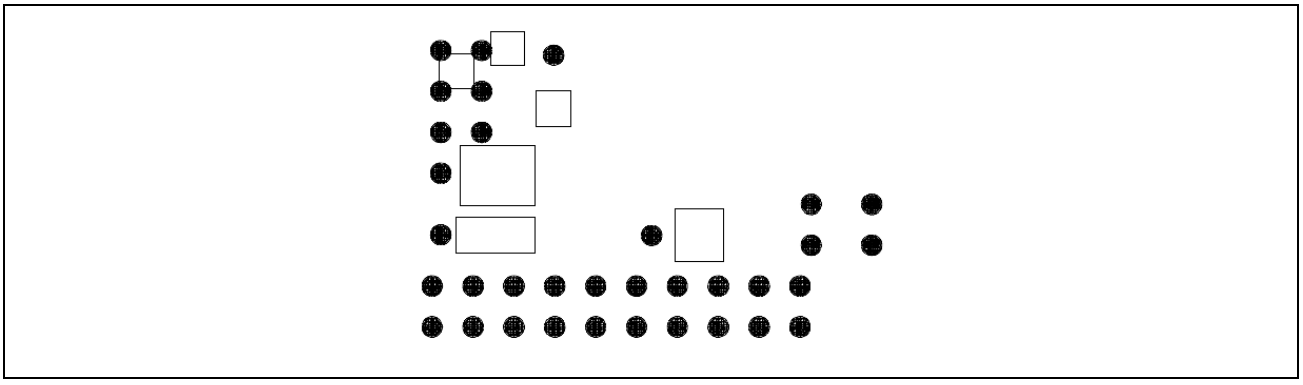


Figure 40: BT and FM first and Second Keepout Area Enlargement

Note: Figure 40 above is an enlargement of the BT and FM keepout area; see Figure 39 on page 119 to view the entire layer.

Section 26: Ordering Information

Table 57: Ordering Information

Part Number	Package	Ambient Temperature
BCM4325GKFBG	Single-band 2.4 GHz WLAN, Bluetooth 3.0 + HS, 196-ball flip-chip FBGA (7.5 mm x 7.5 mm x 1.05 mm, 0.50 mm pitch)	–30°C to +85°C
BCM4325FKFBG	Single-band 2.4 GHz WLAN, Bluetooth 3.0 + HS, FM Rx, 196-ball flip-chip FBGA (7.5 mm x 7.5 mm x 1.05 mm, 0.50 mm pitch)	–30°C to +85°C
BCM4325GKWBG	Single-band 2.4 GHz WLAN, Bluetooth 3.0 + HS, 339-pin WLCSP (6.51 mm X 5.8 mm X 0.4 mm, 0.250 mm pitch)	–30°C to +85°C
BCM4325FKWBG	Single-band 2.4 GHz WLAN, Bluetooth 3.0 + HS, FM Rx, 339-pin WLCSP (6.51 mm X 5.8 mm X 0.4 mm, 0.250 mm pitch)	–30°C to +85°C

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