Integrated Circuit Systems, Inc.

M2004-02/-12

FREQUENCY TRANSLATION PLL

GENERAL DESCRIPTION

The M2004 variants -02 and -12 are VCSO (Voltage Controlled SAW Oscillator) based clock generator PLLs designed for clock frequency translation and jitter attenuation in a high-speed data communications system. The clock multiplication ratio and output divider ratio are pin selectable.

External loop components allow the tailoring of PLL loop response. The M2004-12 adds Hitless Switching with Phase Build-out (HS/PBO) to ensure that reference clock reselection does not disrupt the output clock.

Also read about device variants -22, -32, -42, and -52 in the M2004-x2 Preliminary Information sheet.

FEATURES

◆ **Ideal for OC-48/192 data clock**

◆ **Integrated SAW (surface acoustic wave) delay line**

◆ **VCSO frequency from 300 to 700MHz (Specify VCSO center frequency at time of order)**

◆ **Low phase jitter of < 0.5ps rms, typical (12kHz to 20MHz or 50kHz to 80MHz)**

◆ **Pin-selectable configuration**

◆ **The M2004-12 adds Hitless Switching with Phase Build-out (HS/PBO) to ensure SONET/SDH MTIE and TDEV compliance during reference clock reselection**

◆ **Reference clock inputs support differential LVDS, LVPECL, as well as single-ended LVCMOS, LVTTL**

◆ **Industrial temperature available**

◆ **Single 3.3V power supply**

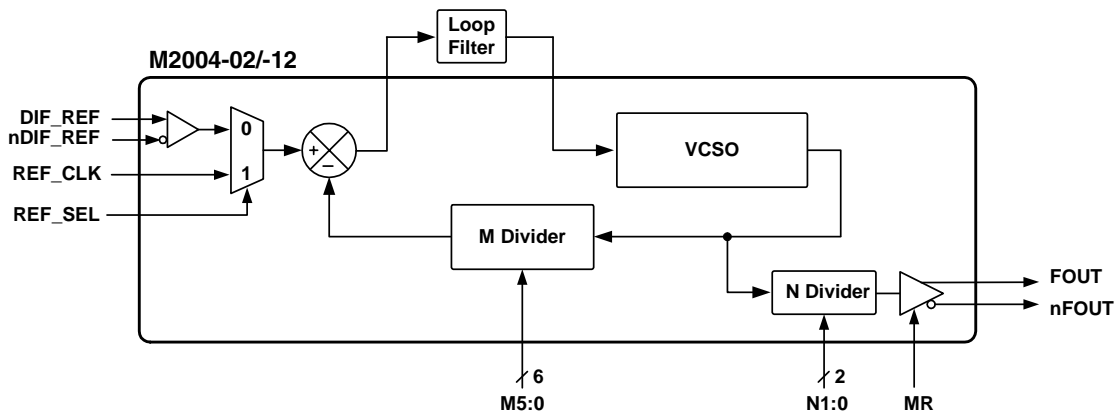◆ **Small 9 x 9 mm SMT (surface mount) package**

SIMPLIFIED BLOCK DIAGRAM

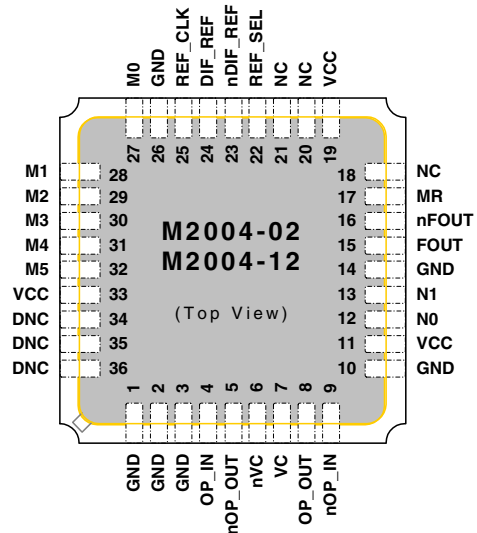## PIN ASSIGNMENT (9 x 9 mm SMT)

Figure 1: Pin Assignment

Example Input / Output Frequency Combinations

Input Clock (MHz)	VCSO [1] Freq (MHz)	Output Freq (MHz)	Application
19.44	622.08	77.76	OC-12 / 48 /192
38.80		155.52	
77.76		311.04	
155.52		622.08	
25.00	625.00	156.25	Gigabit Ethernet

Table 1: Example Input / Output Frequency Combinations

Note 1: Specify VCSO center frequency at time of order

Figure 2: Simplified Block Diagram

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PIN DESCRIPTIONS

Number	Name	I/O	Configuration	Description
1, 2, 3, 10, 14, 26	GND	Ground		Power supply ground connections.
4 9	OP_IN nOP_IN	Input		External loop filter connections. See Figure 4, External Loop Filter, on pg. 5.
5 8	nOP_OUT OP_OUT	Output		
6 7	nVC VC	Input		
11, 19, 33	VCC	Power		Power supply connection, connect to +3.3V.
12 13	N0 N1	Input	Internal pull-down resistor[1]	N divider (output divider) inputs N1:N0. LVCMOS/LVTTL. See Table 5, N Divider Pin Selection, on pg. 3.
15 16	FOUT nFOUT	Output	No internal terminator	Clock output pair. Differential LVPECL.

17	MR	Input	Internal pull-down resistor[1]	Reset:
				    Logic 1 resets M and N dividers and forces FOUT to LOW and nFOUT to HIGH.
				    Logic 0 enables the outputs.
				LVCMOS/LVTTL.

18 20 21	NC NC NC			No connection.
22	REF_SEL	Input	Internal pull-down resistor[1]	Reference clock input selection. LVCMOS/LVTTL. See Table 3, Reference Clock Input Selection, on pg. 3. For the M2004-12, REF_SEL triggers Hitless Switching (HS/PBO) when toggled.
23	nDIF_REF	Input	Internal pull-UP resistor[1]	Reference clock input pair.
24	DIF_REF		Internal pull-down resistor[1]	Differential LVPECL or LVDS.
25	REF_CLK	Input	Internal pull-down resistor[1]	Reference clock input. LVCMOS/LVTTL.
27 28 29 30 31	M0 M1 M2 M3 M4	Input	Internal pull-down resistor[1]	M divider (feedback divider) inputs M5:M0. See Table 4, M Divider Pin Selection, on pg. 3.
32	M5		Internal pull-UP resistor[1]	
34, 35, 36	DNC			Do Not Connect.

Table 2: Pin Descriptions

Note 1: For typical values of internal pull-down and pull-up resistors, see **DC Characteristics** on pg. 6.
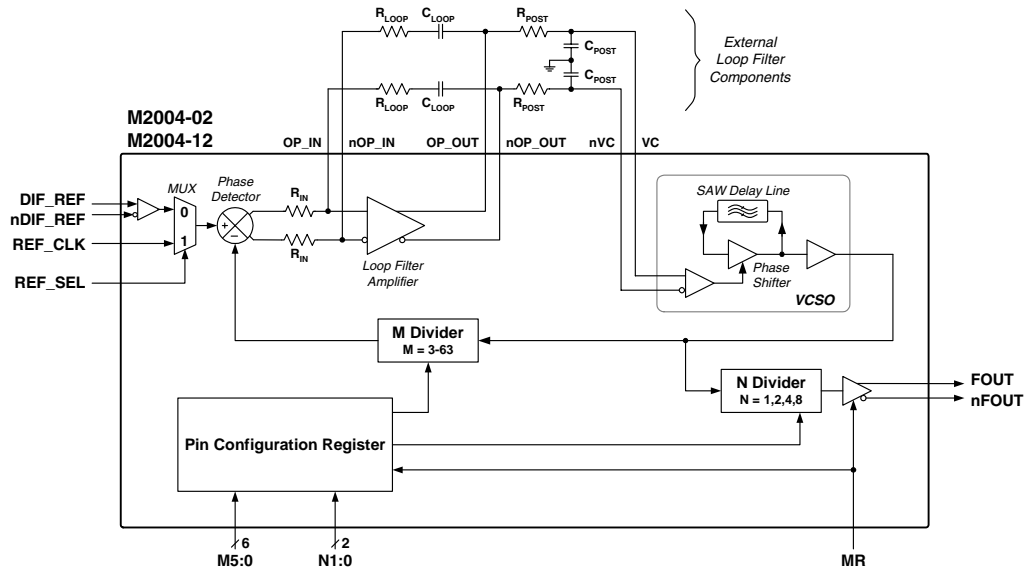
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DETAILED BLOCK DIAGRAM

Figure 3: Detailed Block Diagram

PLL DIVIDER SELECTION TABLES

Reference Clock Input Selection

REF_SEL Pin Setting (Pin 22)	Reference Input Selection
0	DIF_REF, nDIF_REF
1	REF_CLK

Table 3: Reference Clock Input Selection

N Divider Pin Selection

N1:0 Settings (Pin 13 and 12) N1	N0	N Divider Value	Sample Output Frequency (MHz) [1] (FOUT, nFOUT)
0	0	1	622.08
0	1	2	311.04
1	0	4	155.52
1	1	8	77.76

Table 5: N Divider Pin Selection

Note 1: F_{VCSO} = 622.08MHz (e.g., M2004-02-622.0800)

M Divider Pin Selection

M5:0 Pin Settings (Pins 32 - 27) M5 - M0	Definition	Sample Input Clock Freq (MHz) F_{VCSO}=622.08 [1],	F_{VCSO}=625.00 [2]
5[3] 4 3 2 1 0	**Feedback Divider Value "M"**		
0 0 0 0 1 1	M = 3 minimum		
0 0 0 1 0 0	M = 4	155.52	156.25
⋮			
0 0 1 0 0 0	M = 8	77.76	
⋮			
0 1 0 0 0 0	M = 16	38.80	
⋮			
0 1 1 0 0 1	M = 25		25.00
⋮			
1 0 0 0 0 0	M = 32	19.44	
⋮			
1 1 1 1 1 1	M = 63		

Table 4: M Divider Pin Selection

Note 1: F_{VCSO} = 622.08 MHz (e.g., M2004-02-622.0800)
Note 2: F_{VCSO} = 625.00 MHz (e.g., M2004-02-625.0000)
Note 3: M5 pin has a pull-up resister; M4-M0, pull-down.

FUNCTIONAL DESCRIPTION

The M2004-02/-12 is a PLL (Phase Locked Loop) based clock generator that generates output clocks synchronized to one of two selectable input reference clocks. An internal high "Q" SAW delay line provides a low jitter clock signal.

The device can be pin-configured for feedback divider and output divider values. Output is LVPECL compatible. External loop filter component values set the PLL bandwidth to optimize jitter attenuation characteristics.

The M2004-12 adds Hitless Switching with Phase Build-out (HS/PBO) to provide SONET/SDH MTIE and TDEV compliance during a reference clock reselection using the internal mux or when using an external mux.

The M2004-02/-12 is ideal for clock jitter attenuation and frequency translation in 2.5 or 10 Gb optical network line card applications.

Input Reference Clocks

An internal input MUX is provided for input reference clock selection. One input reference clock is selected from between a single-ended LVCMOS / LVTTL clock input or a differential LVPECL or LVDS clock input pair. The maximum input frequency is 175MHz.

PLL Operation

The M2004-02/-12 is a complete clock PLL. It uses a phase detector and configurable dividers to synchronize the output of the VCSO with the selected reference clock.

The "M Divider" divides the VCSO output frequency, feeding the result into the phase detector. The selected input reference clock is fed into the other input of the phase detector. The phase detector compares its two inputs. It then causes the VCSO to increase or decrease in speed as needed to phase- and frequency-lock the VCSO to the reference input.

The value of M directly affects closed loop bandwidth.

The M Divider

The relationship between the VCSO center frequency (Fvcso), the M divider, and the input reference frequency (Fref_clk) is:

$$Fvcso = Fref\_clk \times M$$

The product of M and the input frequency must be such that it falls within the "lock" range of the VCSO.

See APR in AC Characteristics on pg. 7.

N Divider and Outputs

The M2004-02/-12 provides one differential LVPECL output pair: FOUT, nFOUT. By using the N divider, the output frequency can be the VCSO center frequency (Fvcso) or 1/2, 1/4, or 1/8 Fvcso.

See Table 5, N Divider Pin Selection, on pg. 3.

When the N divider is included, the complete relationship for the output frequency (Fout) is defined as:

$$Fout = \frac{Fvcso}{N} = Fref\_clk \times \frac{M}{N}$$

Configuration of M and N Dividers

The M and N dividers can be set by pin configuration using the input pins M0 - M5, N0, and N1.

The data on pins M5:0 and pins N1:0 is passed directly to the M and N dividers.

The divider configuration of the M2004-02/-12 is reset when the input pin MR is set HIGH. MR is set LOW for divider configuration to be operational.

Hitless Switching and Phase Build-out [*]

A proprietary automatic Hitless Switching (HS) function is included in the M2004-12. The HS function provides SONET/SDH MTIE and TDEV compliance during a reference clock reselection using the internal mux or when using an external mux (through detection of the resulting phase transient).[**] A Phase Build-out (PBO) function is also incorporated to absorb most of the phase change in the reference clock input.

The combined HS/PBO function is armed after the device locks to the input clock reference. Once armed, HS/PBO is triggered by either:

- Changing REF_SEL to switch the input reference clock.
- Detection at the phase detector of an input phase transient beyond 4 ns.

Once triggered, the HS function narrows loop band-width to control MTIE during locking to the new input phase. With proper configuration of the external loop filter, the output clocks will comply with MTIE and TDEV specifications for GR-253 (SONET) and ITU G.813 (SDH) during input reference clock changes.

The Phase Build-out (PBO) function enables the PLL to absorb most of the phase change of the input clock. The PBO function selects a new VCSO clock edge for the phase detector feedback clock, selecting the edge closest in phase to the new input clock phase. This reduces re-lock time, the generation of wander, and extra output clock cycles.

Note *: The M2004-02 does not include HS/PBO.

Note **:Transient-triggered HS/PBO is not suitable for use with an unstable reference clock that would induce phase jitter beyond 2 ns at the phase detector (e.g., Stratum DPLL clock sources and unstable recovered network clocks intended for loop timing configuration). Therefore, the M2004-12 also offers the internal mux-triggered HS/PBO capability.

When the PLL locks to within 2 ns of the input clock phase, the PLL returns to normal loop bandwidth and the HS/PBO function is re-armed.

External Loop Filter

To provide stable PLL operation, and thereby a low jitter output clock, the M2004-02/-12 requires the use of an external loop filter components. These are connected to the provided filter pins (see Figure 4). Due to the differential signal path design, the implementation consists of two identical complementary RC filters as shown in Figure 4, below.
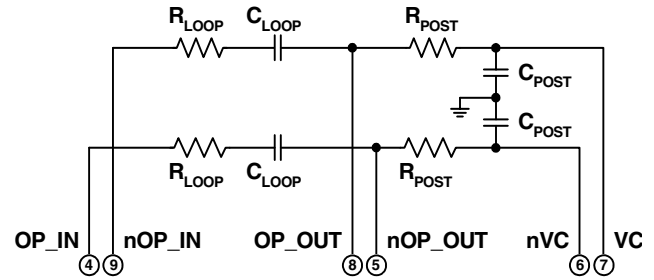

Figure 4: External Loop Filter

PLL bandwidth is affected by the "M" value as well as the VCSO frequency. See Table 6, External Loop Filter Component Values M2004-02/-12, on pg. 5.

PLL Simulator Tool Available

A free PC software utility is available on the ICS website (www.icst.com). The M2000 Timing Modules PLL Simulator is a downloadable application that simulates PLL jitter and wander transfer characteristics. This enables the user to set appropriate external loop component values in a given application.

External Loop Filter Component Values [1] M2004-02/-12

VCSO Parameters: K_{VCO} = 800kHz/V, R_{IN} = 16kΩ, VCSO Bandwidth = 700kHz. See AC Characteristics on pg. 7 for PLL Loop Constants.

Device Configuration			Example External Loop Filter Component Values				Nominal Performance Using These Values		
F_{Ref} (MHz)	F_{VCSO} (MHz)	M Divider Value	R loop	C loop	R post	C post	PLL Loop Bandwidth	Damping Factor	Passband Peaking (dB)
19.44	622.08	32	13kΩ	0.47μF	33kΩ	220pF	3.8kHz	5.6	0.06
19.44	622.08	32	39kΩ	0.022μF	20kΩ	220pF	12.7kHz	7.7	0.03
19.44	622.08	32	2.2kΩ	10.0μF	22kΩ	3300pF	710Hz	4.4	0.10
155.52	622.08	4	3.9kΩ	0.47μF	39kΩ	100pF	11.0kHz	4.7	0.09
155.52	622.08	4	750Ω	10.0μF	7.5kΩ	1000pF	1.6kHz	4.2	0.10

Table 6: External Loop Filter Component Values M2004-02/-12

Note 1: K_{VCO}, VCSO Bandwidth, M Divider Value, and External Loop Filter Component Values determine Loop Bandwidth, Damping Factor, and Passband Peaking. For PLL Simulator software, go to www.icst.com.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Rating	Unit
V_I	Inputs	-0.5 to V_{CC} +0.5	V
V_O	Outputs	-0.5 to V_{CC} +0.5	V
V_{CC}	Power Supply Voltage	4.6	V
T_S	Storage Temperature	-45 to +100	^oC

Table 7: Absolute Maximum Ratings

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in Recommended Conditions of Operation, DC Characteristics, or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

RECOMMENDED CONDITIONS OF OPERATION

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V
T_A	Ambient Operating Temperature					
		Commercial	0		+70	^oC
		Industrial	-40		+85	^oC

Table 8: Recommended Conditions of Operation

ELECTRICAL SPECIFICATIONS

DC Characteristics

Unless stated otherwise, V_{CC} = 3.3V $\pm$5%, T_A = 0 ^oC to +70 ^oC (commercial), F_{VCSO} = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 ^oC to +85 ^oC (industrial)

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
Power Supply	V_{CC}	Positive Supply Voltage		3.135	3.3	3.465	V	
	I_{CC}	Power Supply Current			162		mA	
Differential Input: LVDS / LVPECL	V_{P-P}	Peak to Peak Input Voltage [1]	DIF_REF, nDIF_REF	0.15			V	
	V_{CMR}	Common Mode Input [1]		0.5		V_{CC} - 0.85	V	
LVCMOS / LVTTL Input	V_{IH}	Input High Voltage	REF_CLK, REF_SEL, MR, N0:N1, M0:M5	2		V_{CC} + 0.3	V	
	V_{IL}	Input Low Voltage		-0.3		1.3	V	
Inputs with Pull-down	I_{IH}	Input High Current	DIF_REF, REF_CLK, REF_SEL, MR, N0:N1, M0:M4			150	μA	V_{CC} = V_{IN} = 3.456V
	I_{IL}	Input Low Current		-5			μA	
	$R_{pulldown}$	Internal Pull-down Resistor			51		kΩ	
Inputs with Pull-up	I_{IH}	Input High Current	nDIF_REF, M5			5	μA	V_{CC} = 3.456V V_{IN} = 0 V
	I_{IL}	Input Low Current		-150			μA	
	R_{pullup}	Internal Pull-up Resistor			51		kΩ	
All Inputs	C_{IN}	Input Capacitance	All Inputs			4	pF	
Differential Outputs	V_{OH}	Output High Voltage	FOUT, nFOUT	V_{CC} - 1.4		V_{CC} - 1.0	V	
	V_{OL}	Output Low Voltage		V_{CC} - 2.0		V_{CC} - 1.7	V	
	V_{P-P}	Peak to Peak Output Voltage [2]		0.4		0.85	V	

Table 9: DC Characteristics

Note 1: Single-ended measurement. See Figure 6, Differential Input Level on pg. 8.
Note 2: Single-ended measurement. See Figure 5, Input and Output Rise and Fall Time on pg. 8.

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ELECTRICAL SPECIFICATIONS (CONTINUED)
AC Characteristics
*Unless stated otherwise, V_{CC} = 3.3V $\pm$5%, T_A = 0 °C to +70 °C (commercial), F_{VCSO} = F_{OUT} = 622-675MHz, Outputs terminated with 50Ω to V_{CC} - 2V
T_A = -40 °C to +85 °C (industrial)*

	Symbol	Parameter		Min	Typ	Max	Unit	Conditions
	F_{IN}	Input Frequency	DIF_REF, nDIF_REF, REF_CLK	1		175	MHz	
	F_{OUT}	Output Frequency	FOUT, nFOUT	38		700	MHz	
	APR	VCSO Pull-Range	Commercial	$\pm$120	$\pm$200		ppm	
			Industrial	$\pm$50	$\pm$150		ppm	
PLL Loop Constants [1]	K_{VCO}	VCO Gain			800		kHz/V	
	R_{IN}	Internal Loop Resistor			16		kΩ	
	BW_{VCSO}	VCSO Bandwidth			700		kHz	
Phase Noise and Jitter	Φn	Single Side Band Phase Noise @622.08MHz	1kHz Offset		-72		dBc/Hz	
			10kHz Offset		-94		dBc/Hz	
			100kHz Offset		-123		dBc/Hz	
	J(t)	Jitter (rms)	12kHz to 20MHz		0.5		ps	
			50kHz to 80MHz		0.5		ps	
	odc	Output Duty Cycle [2]	N = 2, 4, or 8	45	50	55	%	
			N = 1	40	50	60	%	
			N = 1, using AC coupled LVPECL output circuit as shown in Figure 8, page 8	45	50	55	%	
	t_R	Output Rise Time [2] for FOUT, nFOUT	F_{OUT} =155.52MHz N = 4 (N1:0 = 10)	350	450	550	ps	20% to 80%
			F_{OUT} =311.04MHz N = 2 (N1:0 = 01)	325	425	500	ps	
			F_{OUT} =622.08MHz N = 1 (N1:0 = 00)	200	275	350	ps	
	t_F	Output Fall Time [2] for FOUT, nFOUT	F_{OUT} =155.52MHz N = 4 (N1:0 = 10)	350	450	550	ps	20% to 80%
			F_{OUT} =311.04MHz N = 2 (N1:0 = 01)	325	425	500	ps	
			F_{OUT} =622.08MHz N = 1 (N1:0 = 00)	200	275	350	ps	
	t_{LOCK}	PLL Lock Time				100	ms	
	MTIE	Mean Time Interval Error [3] M2004-12		Compliant with GR-253-CORE				

Table 10: AC Characteristics

Note 1: Parameters needed for PLL Simulator software; see Table 6, External Loop Filter Component Values M2004-02/-12 on pg. 5.
Note 2: See Parameter Measurement Information below.
Note 3: Requires proper loop filter settings. Consult factory.

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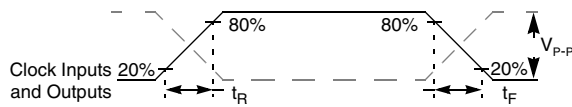# PARAMETER MEASUREMENT INFORMATION

Input and Output Rise and Fall Time

Figure 5: Input and Output Rise and Fall Time
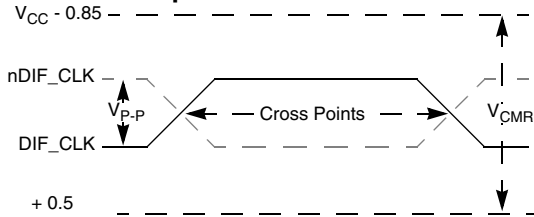
Differential Input Level

Figure 6: Differential Input Level
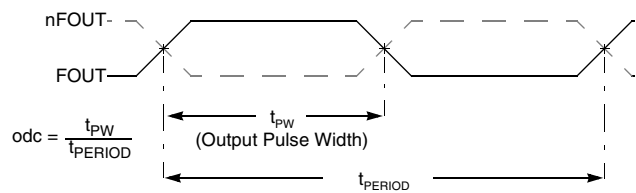
Output Duty Cycle

$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

Figure 7: Output Duty Cycle

AC Coupled LVPECL Output Circuit for 45-55% Duty Cycle at Fvco

Figure 8: AC Coupled Output

AC coupled termination can be used with the M2004-02/-12 LVPECL output, as shown above in Figure 8, to achieve an improved output duty cycle of 45-55% or better at the load when N=1 (output N Divider). This performance has been characterized when R1 = R2 = 200Ω, C1 = C2 = 0.1μF, and when termination resistance at the receiver (combination of R3 with R5, and R4 with R6) is 50 ohms.

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DEVICE PACKAGE - 9 x 9mm CERAMIC LEADLESS CHIP CARRIER

Mechanical Dimensions:

NOTES:
1. DIMENSIONS ARE IN INCHES, DIMENSIONS IN [ ] ARE MM.
2. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE ±.005 [.13]

RECOMMENDED FOOTPRINT

Figure 9: Device Package - 9 x 9mm Ceramic Leadless Chip Carrier

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ORDERING INFORMATION

Part Number: **M2004-x2-xxx.xxxx**

Device Variant

Added Features

-02	none (base)		
-12	HS/PBO		
-22		Fixed NBW	See *M2004-x2 Preliminary Information*
-32	HS/PBO	Fixed NBW	
-42	HS/PBO		
-52	HS/PBO	Fixed NBW	

Feature Key
HS/PBO = Hitless Switching with Phase Build-out

Temperature
"**-**" = 0 to +70 °C (commercial)
I = - 40 to +85 °C (industrial)

Frequency (MHz)
Consult ICS for available VCSO frequencies

Figure 10: Ordering Information

Example Part Numbers

For VCSO Freq (MHz)	Temperature	Part Number
622.08	commercial	**M2004-02- 622.0800** or **M2004-12- 622.0800**
	industrial	**M2004-02I 622.0800** or **M2004-12I 622.0800**

Table 11: Example Part Numbers

Consult ICS for the availability of other VCSO frequencies.