

## Evaluating the AD1974 Four ADC with PLL 192 kHz, 24-Bit Codec

### EVAL-AD1974AZ PACKAGE CONTENTS

- AD1974 evaluation board
- USBi control interface board
- USB cable

### OTHER SUPPORTING DOCUMENTATION

- [AD1974 data sheet](#)

### EVALUATION BOARD OVERVIEW

This document explains the design and setup of the evaluation board for the AD1974. The evaluation board must be connected to an external  $\pm 12\text{ V}$  dc power supply and ground. On-board regulators derive the  $3.3\text{ V}$  supplies for the AD1974. The AD1974 is controlled through an SPI interface. A small external

interface board, EVAL-ADUSB2EBZ (also called USBi), connects to a PC USB port and provides SPI access to the evaluation board through a ribbon cable. A graphical user interface (GUI) program is provided for easy programming of the chip in a Microsoft® Windows® PC environment. The evaluation board allows demonstration and performance testing of most AD1974 features, including the four ADCs, as well as the digital audio ports.

Additional analog circuitry (ADC input filter/buffer) and digital interfaces such as S/PDIF are provided to ease product evaluation.

All analog audio interfaces are accessible with stereo audio 3.5 mm TRS connectors.

### FUNCTIONAL BLOCK DIAGRAM

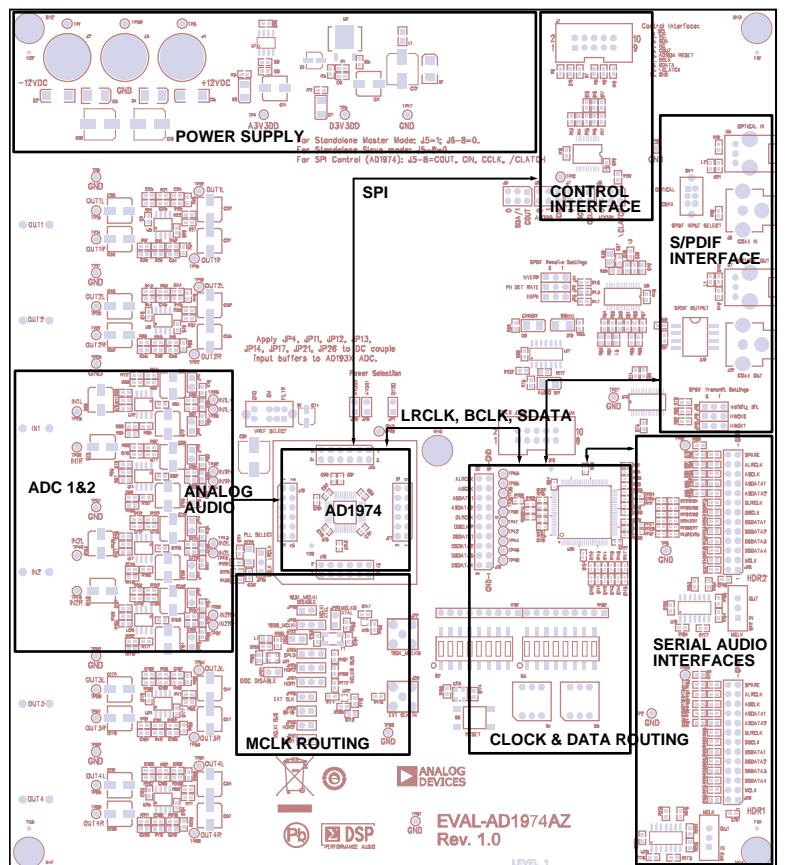


Figure 1.

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**REVISION HISTORY**

**2/10—Revision 0: Initial Version**

## SETTING UP THE EVALUATION BOARD

### STANDALONE MODE

It is possible to run the board and the AD1974 ADC in stand-alone mode, which fixes the functionality of the AD1974 into the I<sup>2</sup>S data format, running at  $256 \times f_s$  (default register condition). The ADC BCLK and LRCLK ports are flipped between slave and master (input and output) by tying COUT (Pin 24) to low or high. This is accomplished by moving the J5 jumper to either 0 or SDA/1 (see Figure 2 and Figure 3 for the correct settings).

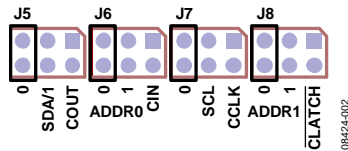


Figure 2. Standalone Slave Mode

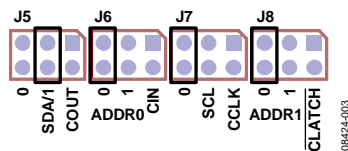


Figure 3. Standalone Master Mode

With the control jumpers set to standalone master mode, the S2 DIP switches set to on, the S3 DIP switch sets to off, and both rotary hex mode switches, S4 and S5, set to 0, the AD1974 is the LRCLK, BCLK, and SDATA source. The default MCLK jumper setting uses the on-board oscillator as MCLK for the AD1974 as well as the S/PDIF transmitter and HDR1 port. The board passes analog audio from the IN1 stereo to the S/PDIF and HDR1 output ports. IN2 can be selected by changing S3, Position 8, to on. Other serial audio clock and data routing configurations are described in the Switch and Jumper Settings section.

### SPI CONTROL

The evaluation board can be configured for interactive control of the registers in the AD1974 by connecting the SPI port to the USBi. The SPI jumper settings are shown in Figure 4.

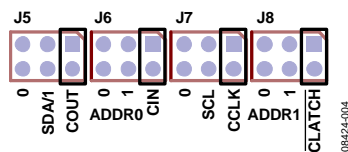


Figure 4. SPI Control

The **Automated Register Window Builder** software controls the AD1974 and is available at [www.analog.com/AD1974](http://www.analog.com/AD1974).

### AUTOMATED REGISTER WINDOW BUILDER SOFTWARE INSTALLATION

The **Automated Register Window Builder** is a program that launches a graphical user interface for direct, live control of the AD1974 registers. The GUI content for the part is defined in a part-specific .xml file; this file is included in the software

installation. To install the **Automated Register Window Builder** software, follow these steps:

1. At [www.analog.com/AD1974](http://www.analog.com/AD1974), find the **Resources & Tools** list.
2. In the list, find **Evaluation Boards & Development Kits** and click **Evaluation Boards/Tools** to open the provided **ARWBvXX.zip** file.
3. Double-click the provided .msi file to extract the files to an empty folder on your PC.
4. Then double-click **setup.exe** and follow the prompts to install the **Automated Register Window Builder**. A computer restart is not required.
5. Copy the .xml file for the AD1974 from the extraction folder into the **C:\Program Files\Analog Devices Inc\AutomatedRegWin** folder, if it does not appear in the folder after installation.

### HARDWARE SETUP, USBi

To set up the USBi hardware, follow these steps:

1. Plug the USBi ribbon cable into the J1 control interface header.
2. Connect the USB cable to your computer and to the USBi.
3. When prompted for drivers, follow these steps:
  - a. Choose **Install from a list or a specific location**.
  - b. Choose **Search for the best driver in these locations**.
  - c. Check the box for **Include this location in the search**.
  - d. Find the USBi driver in **C:\Program Files\ Analog Devices Inc\AutomatedRegWin\USB drivers**.
  - e. Click **Next**.
  - f. If prompted to choose a driver, select **CyUSB.sys**.
  - g. If the PC is running Windows XP and you receive a message that the software has not passed Windows logo testing, click **Continue Anyway**.

You can now open the **Automated Register Window Builder** application and load the .xml file for the part onto your evaluation board.

### POWERING THE BOARD

The AD1974 evaluation board requires power supply input of  $\pm 12$  V dc and ground to the three binding posts; +12 V draws ~250 mA and -12 V draws ~100mA. The on-board regulators provide two 3.3 V rails, one each for AVDD and DVDD for the AD1974. DVDD also supplies power for the active peripheral components on the board. Jumpers are provided to allow access to the power connections of the AD1974. These are convenient points to insert a current measuring device. The only components on the AD1974 side of the jumper are the part itself and the local power supply decoupling. The jumper blocks are shown in Figure 5.

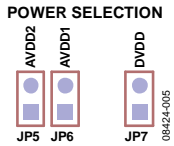


Figure 5. AD1974 Power Jumpers

### SETTING UP THE MASTER CLOCK (MCLK)

The AD1974 evaluation board has a series of jumpers that give the user great flexibility in the MCLK clock source for the AD1974. MCLK can come from five sources: passive crystal, active oscillator, external clock in, and two header connections. Note that the CPLD on the board must have a valid clock source; the frequency is not critical. These jumper blocks can assign this CPLD clock. Most applications of the board use MCLK from either the oscillator or one of the header (HDR) inputs. Figure 6 to Figure 7 show the on-board active oscillator disabled so that it does not interfere with the selected clock. The clock feed to the CPLD comes directly from the clock source.

Note that, if the HDR connectors are to be driven with MCLK from a source on the evaluation board, SW2 and/or SW3 must be switched from the IN position to the OUT position.

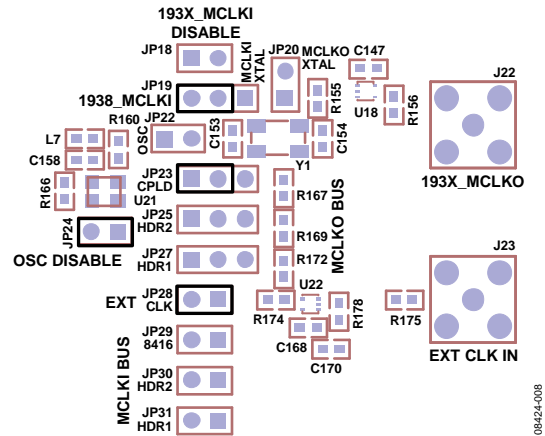


Figure 8. External Clock In as Master; the AD1974 and CPLD as Slaves

The MCLK configurations shown in Figure 9 and Figure 10 use the AD1974 MCLKO port to drive the CPLD and, possibly, the HDRs. The passive crystal runs the AD1974 at 12.288 MHz. Figure 10 shows the MCLKI shut off; this is the case when the PLL is set to LRCLK instead of to MCLK.

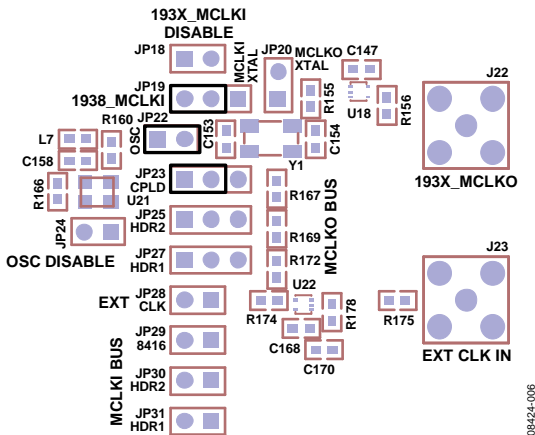


Figure 6. Active On-Board Oscillator as Master; the AD1974 and CPLD as Slaves

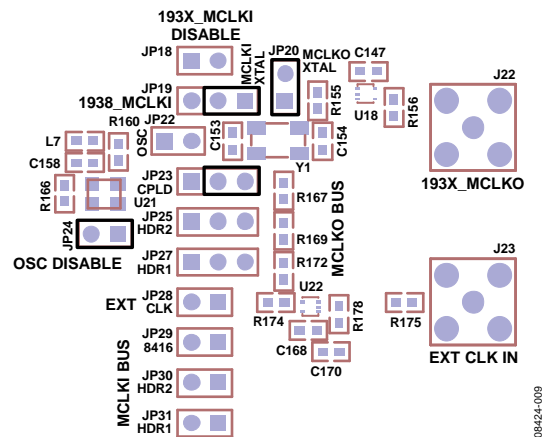


Figure 9. Passive Crystal; the AD1974 Is Master; the CPLD Is Slave from the MCLKO Port

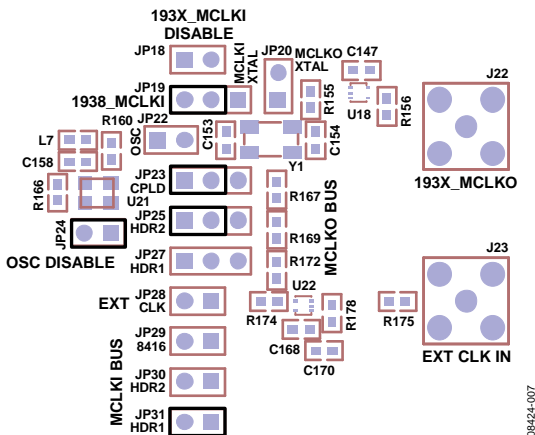


Figure 7. HDR1 as MCLK Master; the AD1974, CPLD, and HDR2 as Slaves

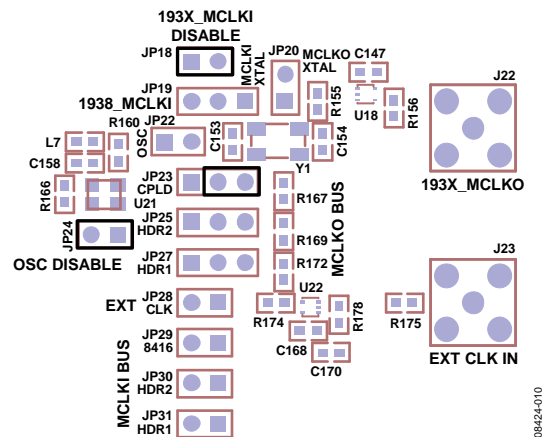


Figure 10. LRCLK Is the Master Clock Using the PLL; MCLKI Is Disabled, and CPLD Is Slave to the MCLKO Port

### CONFIGURING THE PLL FILTER

The PLL for the AD1974 can run from either MCLK or LRCLK, according to its setting in the PLL and Clock Control 0 register, Bits[6:5]. The matching RC loop filter must be connected to LF (Pin 47) using JP15. See Figure 11 and Figure 12 for the jumper positions.

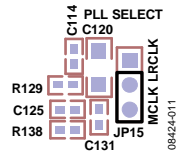


Figure 11. MCLK Loop Filter Selected



Figure 12. LRCLK Loop Filter Selected

Normally, the MCLK filter is the default selection; it is also possible to use the register control window to program the PLL to run from the LRCLK. In this case, the jumper must be changed as shown in Figure 12.

### CONNECTING AUDIO CABLES

#### Analog Audio

The analog inputs and outputs use 3.5 mm TRS jacks; they are configured in the standard configuration: tip = left, ring = right, sleeve = ground. The analog inputs to IN1 and IN2 generate 0 dBFS from a 1 V rms analog signal. The on-board buffer circuit creates the differential signal to drive the ADC with 2 V rms at the maximum level. There are test points that allow direct access to the ADC pins; note that the ADC pins have a common mode voltage of 1.5 V dc. These test points require proper care so that improper loading does not drag down the common-mode voltage, and the headroom and performance of the part do not suffer.

The ADC buffer circuit has been designed with a switch (S1) that allows the user to change the voltage reference for all of the amplifiers. GND, CM and FILTR can be selected as a reference; it is advisable to shut down the power to the board before changing this switch. The CM and FILTR lines are very sensitive and do not react well to a change in load while the AD1974 is active. A series of jumpers allows the user to dc-couple the buffer circuit to the ADC analog port in when CM and FILTR are selected (see Figure 13).

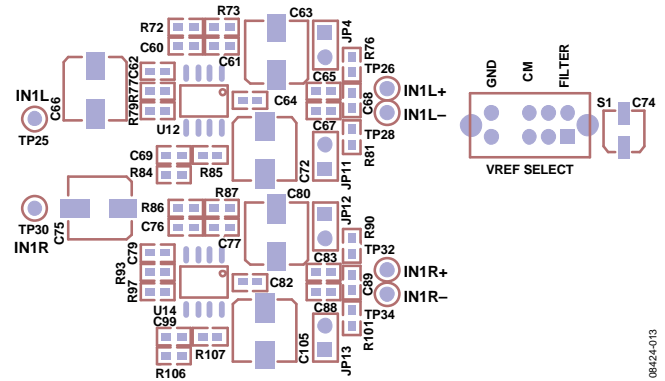


Figure 13. VREF Selection and DC Coupling Jumpers

#### Digital Audio

There are two types of digital interfacing, S/PDIF and discrete serial. The S/PDIF transmitter port has both optical and coaxial connectors that can be used simultaneously. The serial audio connectors use 1 × 2 100 mil spaced headers, signal and ground. The LRCLK, BCLK, and SDATA paths are available for the ADC on the HDR1 and HDR2 connectors. Each has a connection for MCLK; each HDR MCLK interface has a switch to set the port as an input or output, depending on the configuration of the evaluation board.

### SWITCH AND JUMPER SETTINGS

#### Clock and Control

The AD1974 is designed to run in standalone mode at a sample rate ( $f_s$ ) of 48 kHz, with an MCLK of 12.288 MHz ( $256 \times f_s$ ). In standalone slave mode, the ADC port must receive valid BCLK and LRCLK. The AD1974 can be clocked from the HDR1 connector; the ADC BCLK and LRCK port sources are selected with S2, Position 2 and Position 3. For HDR1 as master, S2, Position 3, should be on (see the detail in Figure 14 and Figure 15). Note that HDR2 is not implemented in the CPLD routing code.

It is also possible to configure the AD1974 ADC BCLK and LRCK ports to run in standalone master mode; moving J5 to SDA/1, as shown in Figure 3, changes the state of the AD1974. Setting S2, Position 2, to on selects the proper routing to both the S/PDIF transmitter and the HDR1 connector. In this mode, the AD1974 ADC port generates BCLK and LRCLK when given a valid MCLK.

For the full flexibility of the AD1974, the part can be put in SPI control mode and programmed with the **Automated Register Window Builder** application (see Figure 4 for the appropriate jumper settings). Changing the registers and setting the DIP switches allow many possible configurations. In the various master and slave modes, the AD1974 takes MCLK from a selected source and can be set to generate or receive either BCLK or LRCLK to or from either the ADC or the DAC port, depending on the settings and requirements.

As an example, to set the ADC port as master, switch the ADC Control Register 2 bits for BCLK and LRCLK to master and change S2, Position 2, and S2, Position 5, to on. In this mode, the board is configured so that the ADC BCLK and LRCLK pins are the clock source for both the ADC destination and the DAC data source. For the DAC port to be the master, the DAC Control Register 1 bits for BCLK and LRCLK must be changed to master, and S2, Position 2 and Position 3, and S2, Position 5 and Position 6, must all be on. On this evaluation board, these settings allow the master port on the [AD1974](#) to drive both the S/PDIF and the HDR connections. Many combinations of master and slave are possible (see Figure 14 and Figure 15 for the correct settings).

#### **S/PDIF Audio**

The settings in Figure 14 and Figure 15 show the details of clock routing and control for the ADC port. The board is shipped with the IN1 analog port selected as default feed to the S/PDIF transmitter; the hex switches are set to 0 and only the S2, Position 2, DIP switch is on. All other switches are set to off. The evaluation board is shipped in standalone master mode

(see Figure 3); the BCLK and LRCLK signals run from the ADC port of the AD1974 to the S/PDIF transmitter and HDR1.

In this default configuration, IN1 analog is routed through the AD1974 ADC ASDATA1 path to the S/PDIF output. By changing DIP switch S3, Position 8, from 0 to 1, IN2 is selected.

#### **HDR Connectors—Serial Audio**

Routing of serial audio to the HDR1 connector is controlled by DIP S3, Position 6 and Position 7. The default condition routes IN1 to ASDATA1 and IN2 to ASDATA2.

#### **Other Options**

To use other  $f_s$  rates, the USBi must be connected and the AD1974 registers must be programmed accordingly. For example, adjusting the  $f_s$  rate to 96 kHz requires that the ADC Control 0 register have the sample rate set to 96 kHz (see Figure 14 and Figure 15 for the complete list of options).

The CPLD code is presented in the CPLD Code section and is included with the evaluation board; alterations and additions to the functionality of the CPLD are possible by altering the code and reprogramming the CPLD.

# ROTARY AND DIP SWITCH SETTINGS

**AD1974/ADAU132X Rev-E Evaluation Board Configuration: (\* indicates default setting)**

- 1) DIP Switch S2 Position-8 (SPDIF\_RX\_TX reset) must be toggled after power-up for proper operation of the SPDIF receiver and transmitter.
  - 2) The AD1974 evaluation board defaults the AD1974 codec to standalone mode preventing SPI/I<sup>2</sup>C operation. The J5, J6, J7, and J8 header jumpers can be changed for SPI/I<sup>2</sup>C operation.
- 1) DIP Switch S2 controls the AD1974 ADC and DAC serial clock source selection. One of four clock sources is selected based on the setting. SPDIF Receiver CS8416, Header Connector HDR1, ADC serial clocks, or DAC serial clock can be the clock source. ADC and DAC serial clock selection is controlled independently.
  - 2) The AD1974 master clock source should be selected using the JP28, JP29, JP30, and JP31 header jumpers such that the MCLK source is in sync with the DAC/ADC serial clock and data source.

DIP Switch S2 position:		Description	
<b>Position-1</b>			
<b>ADC - ABCLK, ALRCLK Clock Disable</b>			
Off*	Enable	Enable ADC clocks	
On	Disable	Tristate ADC clocks	
<b>Position-2</b>			
<b>ADC - ABCLK, ALRCLK Source Selection</b>			
Off*	SPDIF_RX_8416	ALRCLK Source	SPDIF_RX_8416
Off	HDR1_ABCLK	HDR1_ALRCLK	Slave
On	Off	ADC-ABCLK	Slave
On	On	DAC-DBCLK	Slave
<b>Position-3</b>			
<b>DAC - DBCLK, DLRCLK Clock Disable</b>			
Off*	Enable	Enable DAC clocks	
On	Disable	Tristate DAC clocks	
<b>Position-4</b>			
<b>DAC - DBCLK, DLRCLK Source Selection</b>			
Off*	SPDIF_RX_8416	DLRCLK Source	SPDIF_RX_8416
Off	HDR1_DBCLK	HDR1_DLRCLK	Slave
On	Off	ADC-ABCLK	Slave
On	On	DAC-DBCLK	Slave
<b>Position-5</b>			
<b>DAC - DBCLK, DLRCLK TX Clock Rate Selection</b>			
Off*	SPDIF_RX_TX MCLK Rate = 256xfs	SPDIF_TX Clocks	Slave
On	SPDIF_RX_TX MCLK Rate = 128xfs	HDR1 Clocks	Master
<b>Position-6</b>			
<b>DAC - DBCLK, DLRCLK TX/RESET</b>			
Off*	SPDIF_RX_TX in active mode	SPDIF_RX Clocks	Slave
On	SPDIF_RX_TX in reset mode	SPDIF_TX Clocks	Slave
<b>Position-7</b>			
<b>SPDIF_TX - CS8406 MCLK Jumper Settings</b>			
Off*	SPDIF_TX_CS8406 MCLK JP10	ADC Clocks	N/A
On	JP9	DAC Clocks	N/A
<b>Position-8</b>			
<b>SPDIF_TX_RX/RESET</b>			
Off*	SPDIF_RX_TX in active mode	HDR1 Clocks	Slave
On	SPDIF_RX_TX in reset mode	ADC Clocks	N/A
<b>SPDIF_RX - CS8416 Jumpers</b>			
<b>JP1</b>			
0 = Normal update rate phase detector, increased clock jitter	JP2	ADC Clocks	N/A
1 = High update rate phase detector, low clock jitter	0 = NVERR selected	DAC Clocks	Slave
	1 = RERR selected	HDR1 Clocks	Master
<b>SPDIF_TX - CS8406 Jumpers</b>			
<b>JP18</b>			
0 = The V pin input determines the state of the validity bit in the outgoing AES3 transmitted data	JP9	ADC Clocks	N/A
1 = The V pin input determines the state of the validity bit in the outgoing AES3 transmitted data	JP10	DAC Clocks	Slave
	0	HDR1 Clocks	Slave
	1	ADC Clocks	Master
		DAC Clocks	Slave

(Note: This position must be toggled after power-up for proper operation.)

Figure 14. Settings Chart 1

DAC and ADC Serial Data (DSDATA/ASDATA) Source Selection and Routing (Switch S4 and Switch S3)

Rotary hex Switch S4 selects the AD1974 DAC serial data source. The DAC data source can be either SPDIF Receiver CS8416 or can be provided by the Header Connector HDR1. It is important to note that the DAC data source should be in sync with the DAC serial/port clock source (set by DIP Switch S2, Positions [5:6]). DIP Switch S3 routes the ADC serial data among AD193x, SPDIF Transmitter CS8406, and Header Connector HDR1 in stereo, TDM, and aux mode.

***** Signal sources to the DAC data lines (DSDATA1/2/3/4) fill the columns, column header is the destination *****		DAC2 (DSDATA2)		DAC3 (DSDATA3)		DAC4 (DSDATA4)		Description	
S4 Position	DAC1 (DSDATA1)	DAC2 (DSDATA2)	DAC3 (DSDATA3)	DAC4 (DSDATA4)	DAC1 (DSDATA1)	DAC2 (DSDATA2)	DAC3 (DSDATA3)	DAC4 (DSDATA4)	Description
0*	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416 stereo data to all eight DAC channels
1	SPDIF_RX_8416	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1_DSDATA4	SPDIF_RX_8416 stereo data to DAC1 only, rest DACs 2/3/4 data from HDR1 connector
2	HDR1_DSDATA1	SPDIF_RX_8416	HDR1_DSDATA3	HDR1_DSDATA4	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1_DSDATA4	SPDIF_RX_8416 data to DAC2 only, rest DACs 1/3/4 data from HDR1 connector
3	HDR1_DSDATA1	HDR1_DSDATA2	SPDIF_RX_8416	HDR1_DSDATA4	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1_DSDATA4	SPDIF_RX_8416 data to DAC3 only, rest DACs 1/2/4 data from HDR1 connector
4	HDR1_DSDATA1	N/A	HDR1_DSDATA3	N/A	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1_DSDATA4	SPDIF_RX_8416 data to DAC4 only, rest DACs 1/2/3 data from HDR1 connector
5	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	Source zero data to all eight DAC channels
6	N/A	ZERO DATA	ZERO DATA	ZERO DATA	ZERO DATA	ZERO DATA	ZERO DATA	ZERO DATA	HDR1 Connector Signal HDR1_DSDATA1 drives all four DAC pairs
7	Stereo/TDM	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive corresponding DAC data lines
8	Stereo	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive/receive corresponding DAC data lines in TDM mode
9	TDM	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive/receive corresponding DAC data lines in TDM mode
A	Dual-Line TDM	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive/receive corresponding DAC data lines in TDM mode
B	DAC aux mode	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive/receive corresponding DAC data lines in TDM mode
C	DAC aux mode	Aux ADC1 input	Aux ADC2 input	Aux ADC3 input	Aux ADC2 input	Aux ADC3 input	Aux ADC4 input	Aux ADC4 output	
D									
E									
F	Stereo/TDM	TRISTATE	TRISTATE	TRISTATE	TRISTATE	TRISTATE	TRISTATE	TRISTATE	Tristate all DAC data lines, DSDATA1, DSDATA2, DSDATA3, and DSDATA4

***** Column content indicates the direction of the DAC data pins and corresponding HDR1 connector DAC data pins *****		DAC2 (DSDATA2)		DAC3 (DSDATA3)		DAC4 (DSDATA4)		Description	
S4 Position	DAC1 (DSDATA1)	DAC2 (DSDATA2)	DAC3 (DSDATA3)	DAC4 (DSDATA4)	DAC1 (DSDATA1)	DAC2 (DSDATA2)	DAC3 (DSDATA3)	DAC4 (DSDATA4)	Description
0*	Input	Input	Input	Input	N/A	N/A	N/A	N/A	Master
1	Input	Input	Input	Input	N/A	Input	Input	Input	Master
2	Input	Input	Input	Input	Input	N/A	Input	Input	Master
3	Input	Input	Input	Input	Input	Input	N/A	Input	Master
4	Input	Input	Input	Input	Input	Input	Input	Input	Master
5	Input	Input	Input	Input	Input	Input	Input	Input	Master
6	Input	Input	Input	Input	Output	Output	Output	Output	N/A
7	Input	Input	Input	Input	Input	Input	Input	Input	Master
8	Input	Input	Input	Input	Input	Input	Input	Input	Master
9	Output	Output	Output	Output	Input	Input	Input	Input	Master
A	Output	Output	Output	Output	Input	Input	Input	Input	Master
B	Output	Output	Output	Output	Input	Input	Input	Input	Master
C	Output	Output	Output	Output	Input	Input	Input	Input	Master
D	Output	Output	Output	Output	Input	Input	Input	Input	Master
E	Output	Output	Output	Output	Input	Input	Input	Input	Master
F	TRISTATE	TRISTATE	TRISTATE	TRISTATE	TRISTATE	TRISTATE	TRISTATE	TRISTATE	Master

DIP Switch S3 Position:		ADC Serial Format		HDR1_ASDATA1		HDR1_ASDATA2		Description (HDR1 ADC Data Source Selection)	
Position-6	Position-7	Stereo	Stereo	ASDATA1	ASDATA2	ASDATA1	ASDATA2	HDR1 Connector ADC Data Lines ASDATA1 and ASDATA2 receive corresponding ADC data stream	
Off*	On	Stereo	Stereo	ASDATA1	ASDATA2	ASDATA1	ASDATA2	HDR1 Connector ADC Data Line ASDATA1 receive ADC2 data line ASDATA2	
On	Off	Stereo	Stereo	ASDATA1	ASDATA2	ASDATA1	ASDATA2	HDR1 Connector ADC Data Line ASDATA1 receive ADC2 data line ASDATA2	
On	On	TDM	TDM	ASDATA1	ASDATA2	ASDATA1	ASDATA2	HDR1 Connector ADC Data Line ASDATA1 receive ADC TDM out data stream	
On	On	ADC Aux (see note)	ADC Aux (see note)	ASDATA1	ASDATA2	ASDATA1	ASDATA2	HDR1 Connector ADC Data Line ASDATA1 receive ADC TDM out data stream	

DIP Switch S3 Position:		HDR1_ASDATA1		HDR1_ASDATA2		ADC1 (ASDATA1)		ADC2 (ASDATA2)	
Position-6	Position-7	Output	Output	Output	Output	Output	Output	Output	
Off*	On	Output	Output	Output	Output	Output	Output	Output	
Off	Off	Output	Output	Output	Output	Output	Output	Output	
On	Off	Output	Output	Output	Output	Output	Output	Output	
On	On	Output	Output	Output	Output	Output	Output	Output	

DIP Switch S3 Position:		ADC1 Data Stream ASDATA1		ADC2 Data Stream ASDATA2	
Position-8	Position-9	ASDATA1	ASDATA2	ASDATA1	ASDATA2
Off*	On	ASDATA1	ASDATA2	ASDATA1	ASDATA2
On	Off	ASDATA1	ASDATA2	ASDATA1	ASDATA2

Figure 15. Settings Chart 2





08424-017

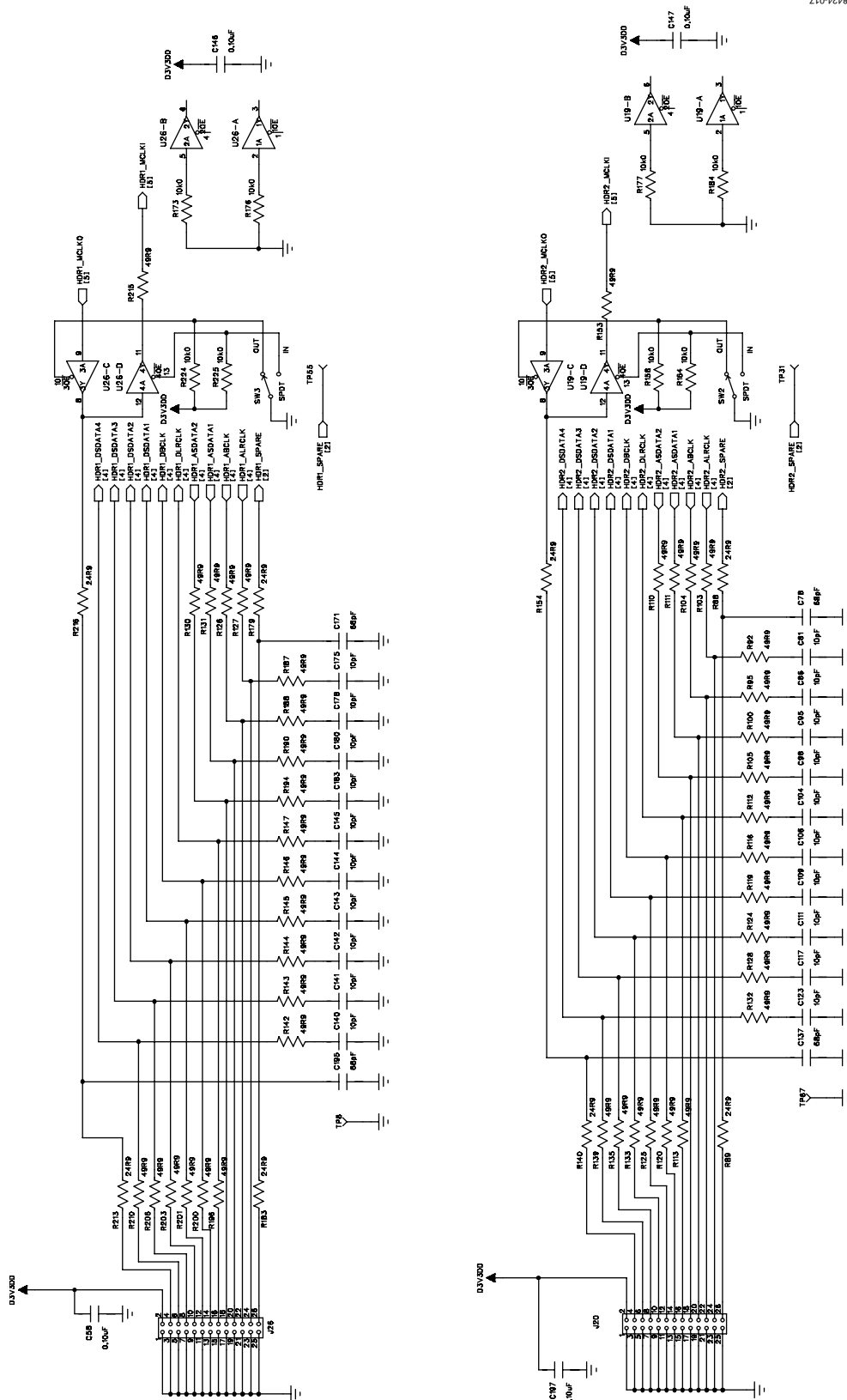


Figure 17. Board Schematics, Page 2—Serial Digital Audio Interface Headers with MCLK Direction Switching

08424-018

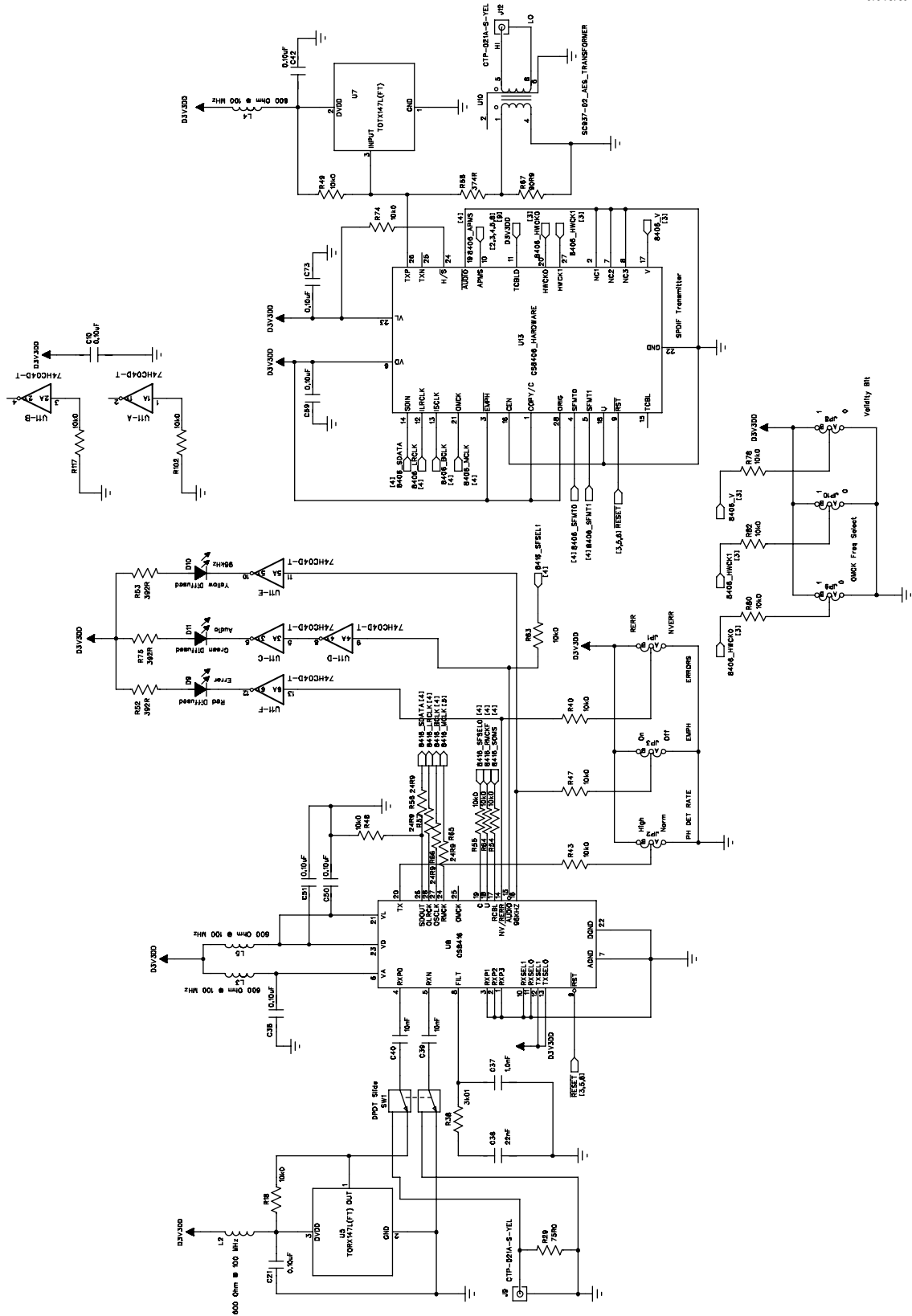


Figure 18. Board Schematics, Page 3—S/PDIF Receive and Transmit Interfaces

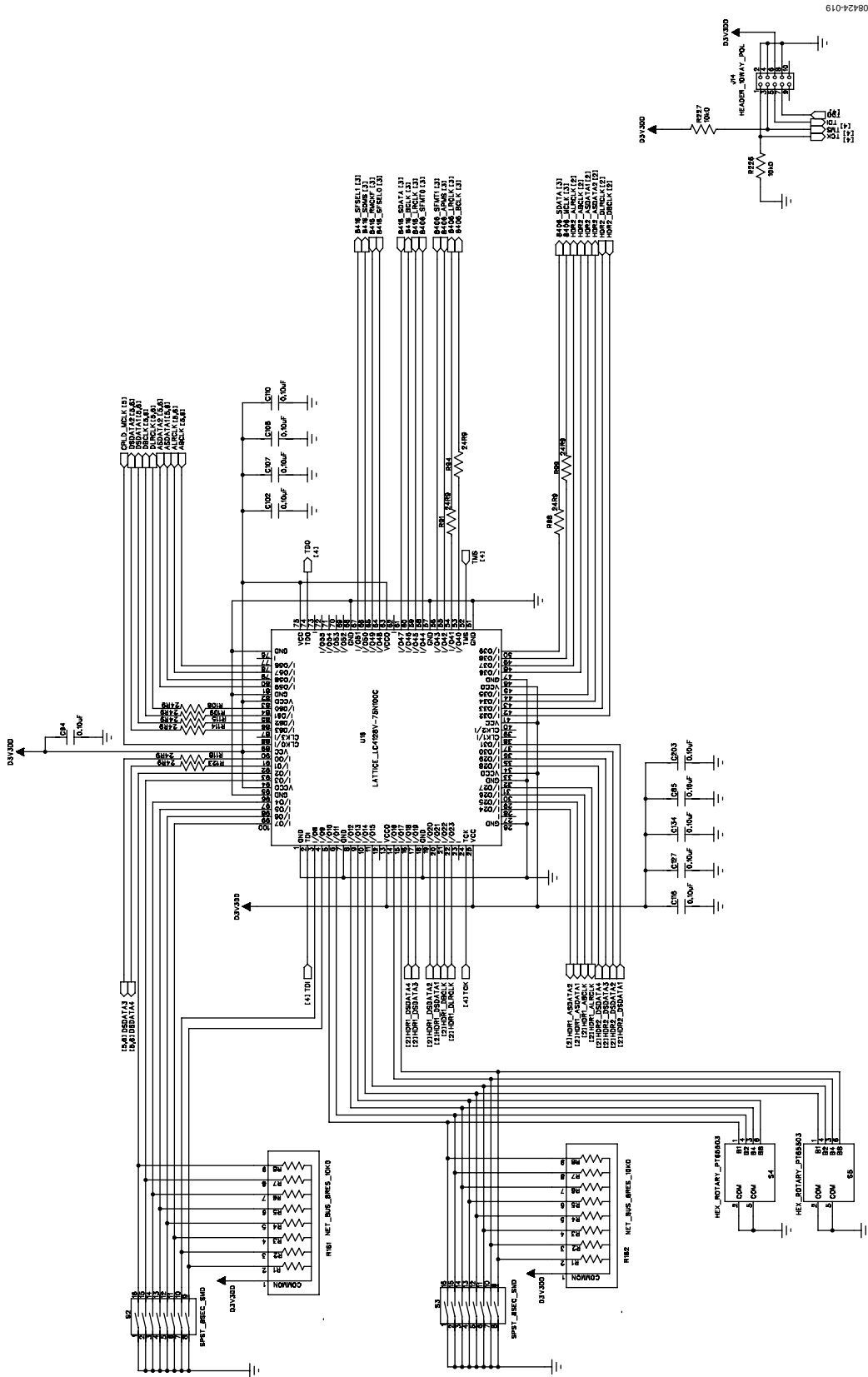


Figure 19. Board Schematics, Page 4—Serial Digital Audio Routing and Control CPLD

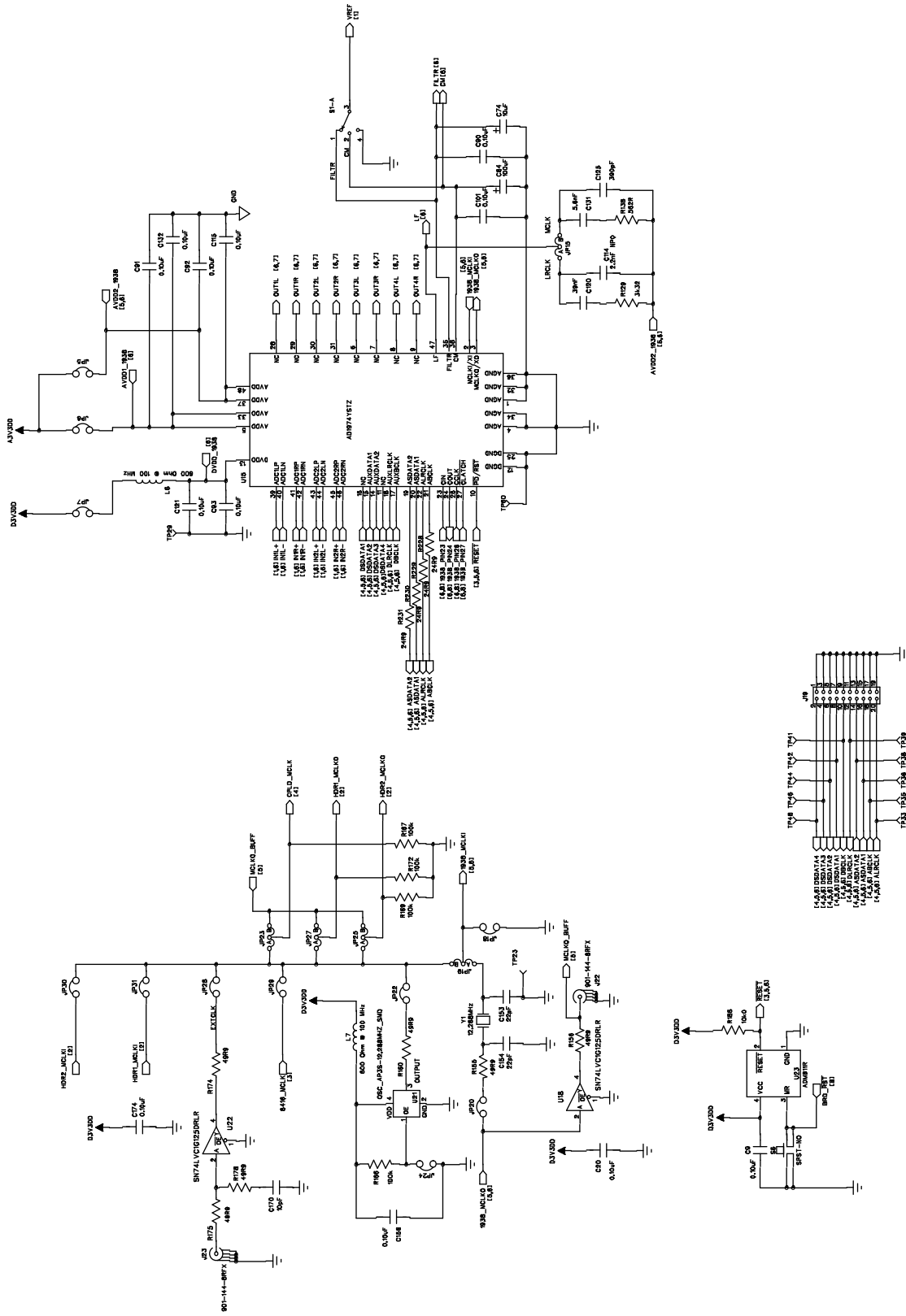
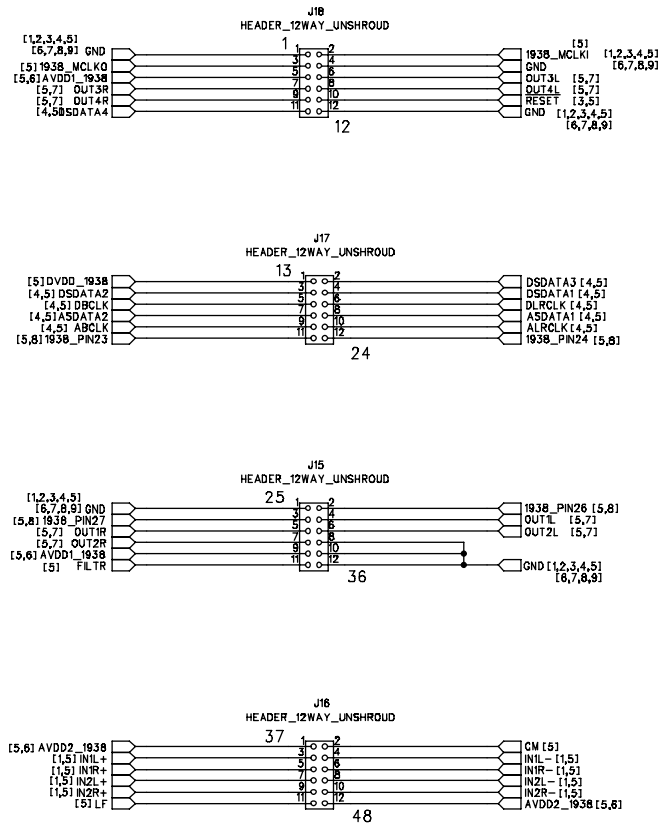


Figure 20. Board Schematic, Page 5—AD1974 with MCLK Selection Jumpers



08424-021

Figure 21. Board Schematics, Page 6—Daughter Card Interface, Useful as Test Points

08424-022

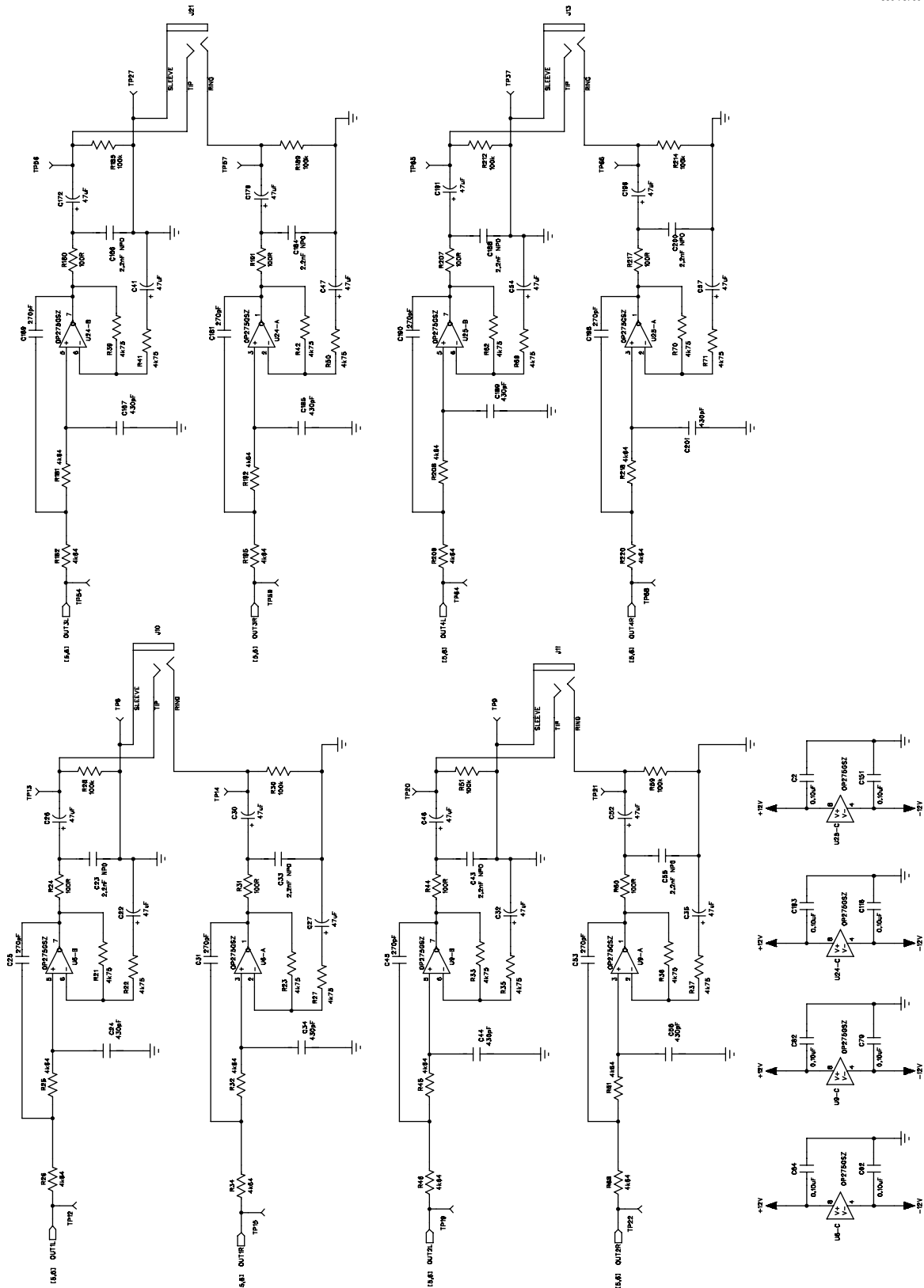


Figure 22. Board Schematics, Page 7—DAC Buffer Circuits

08424-023

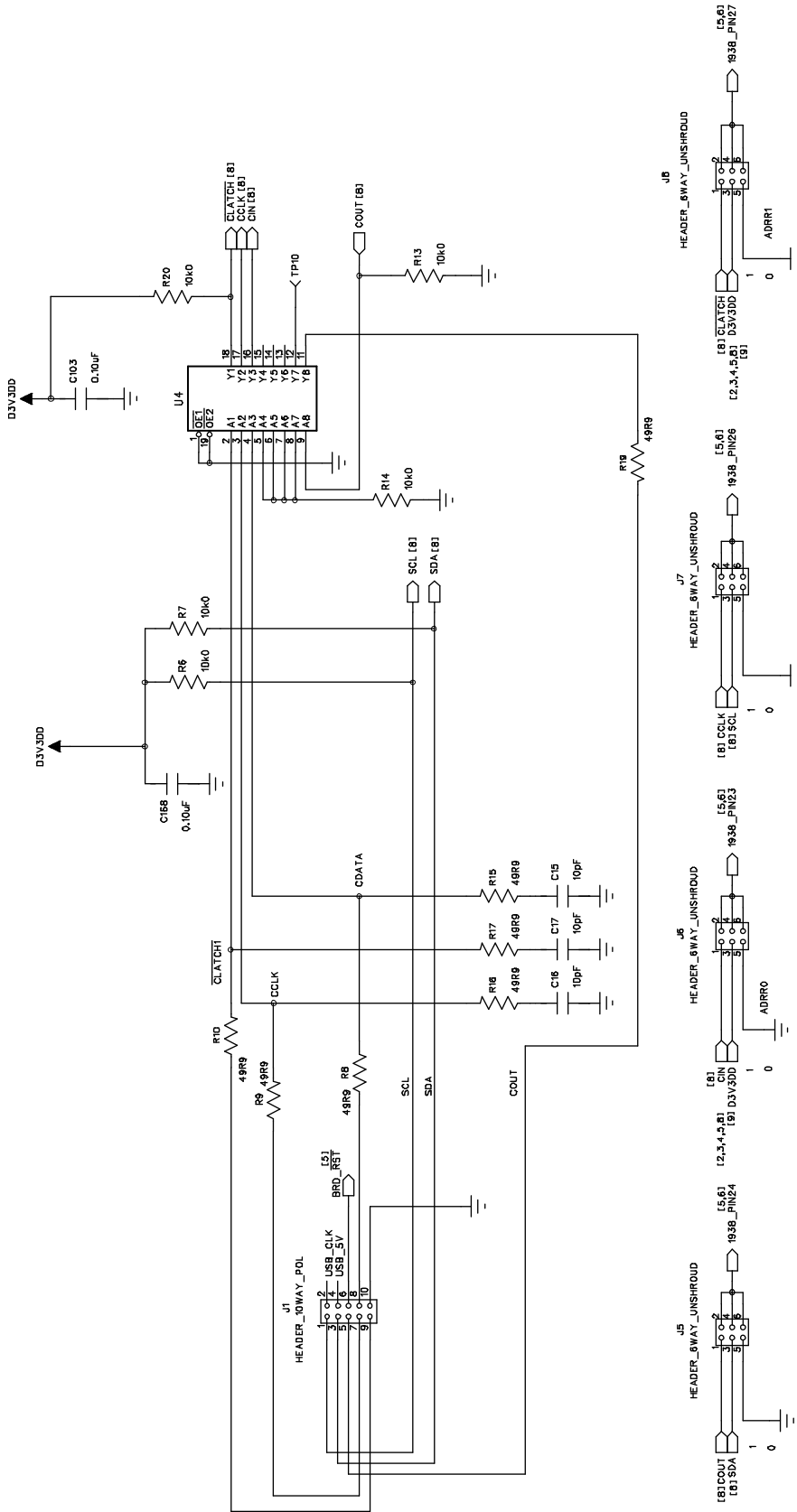


Figure 23. Board Schematics, Page 8—SPI Control Interface

- For AD1974 (SPI), JP5-8 to 1-2 position.
- For AD1976 (I2C), JP5&7 to 3-4 to select I2C mode.
- AD1976 (I2C) ADDR jumpers (J6&8) must match Global Address Bits
- For Standalone Master mode: All=0, except 1938\_PIN24=SDA (J5).
- For Standalone Slave mode: All=0.
- Any change to this configuration requires that the part be reset.



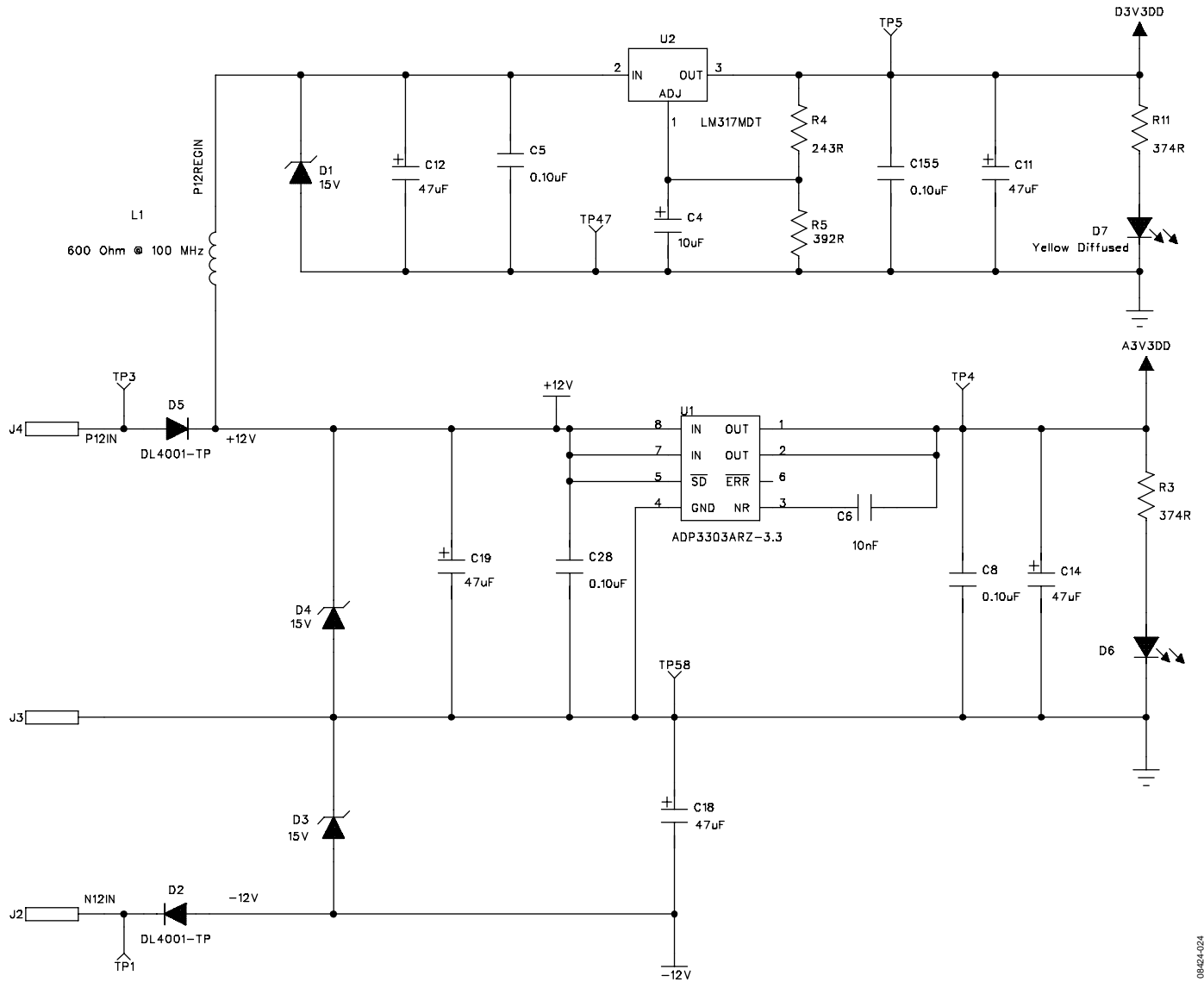


Figure 24. Board Schematics, Page 9—Power Supply

06924-024

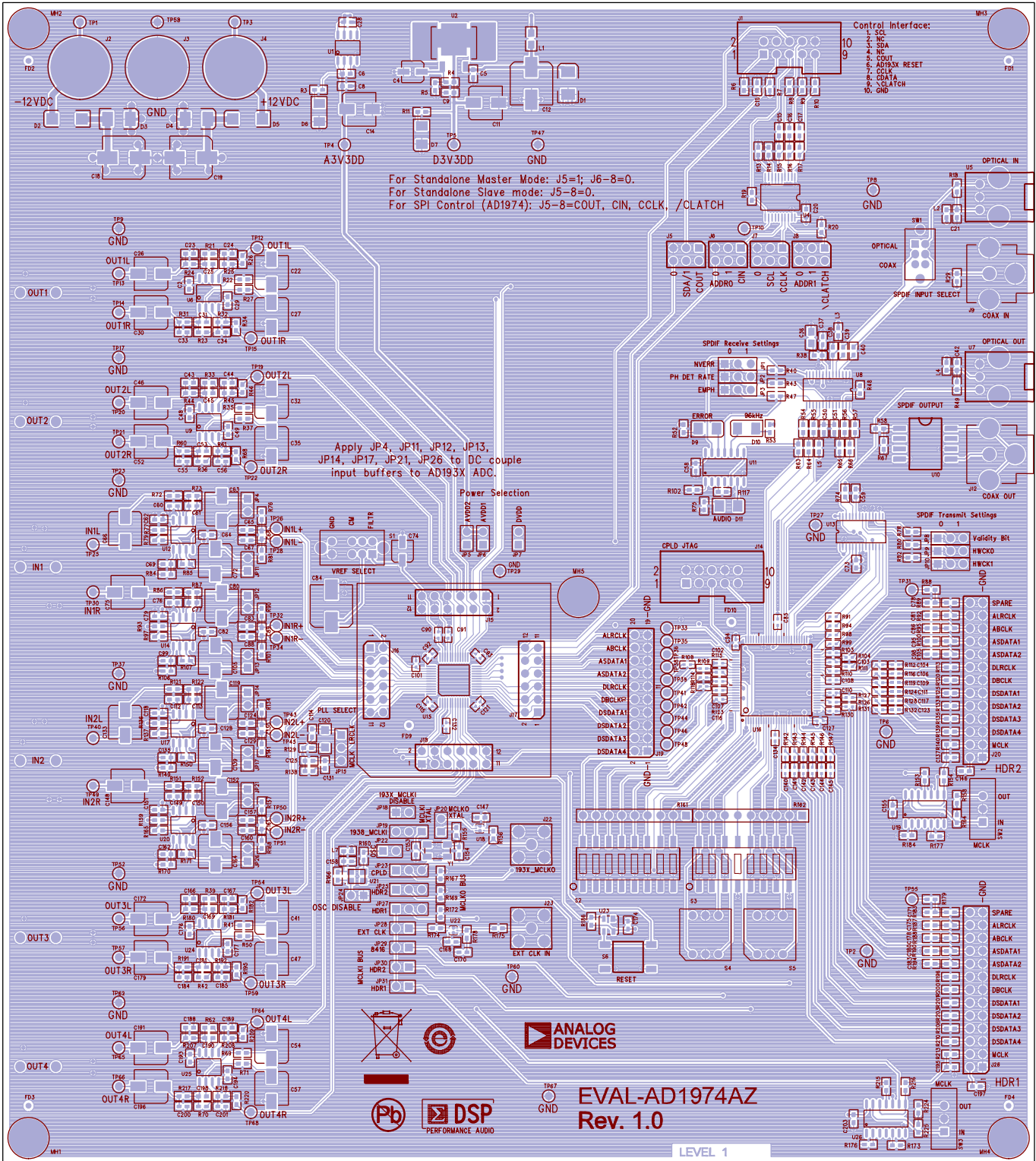


Figure 25. Top Assembly Layer

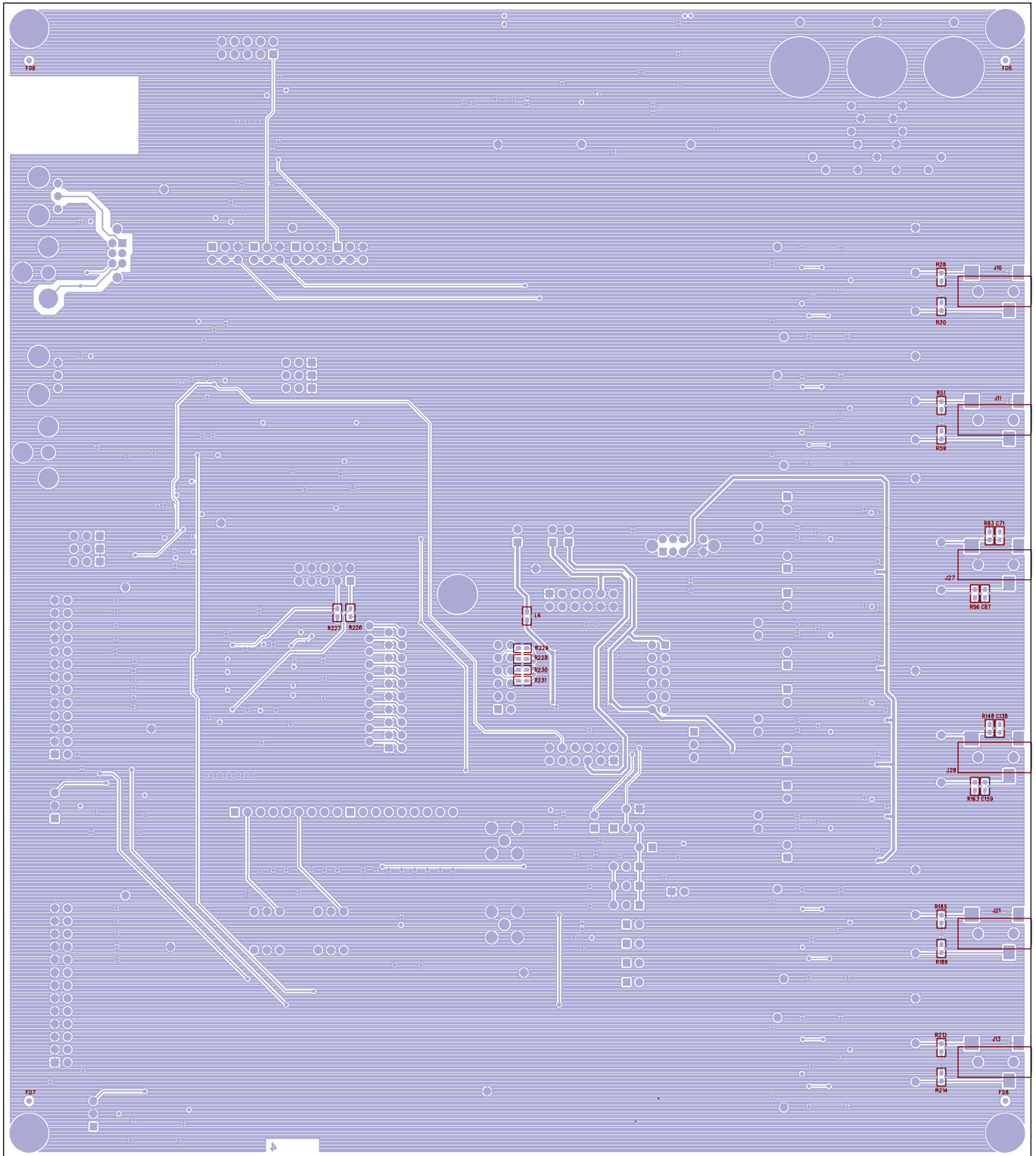


Figure 26. Bottom Assembly Layer

08424-026

**CPLD CODE**

```

MODULE                                IF_Logic
TITLE      'AD1974 EVB Input Interface Logic'
//=====
// FILE:                                AD1974_pld_revE.abl
// REVISION DATE:                        04-16-09 (rev-E)
// REVISION:                              E
// DESCRIPTION:
//=====

LIBRARY 'MACH';

"INPUTS -----
// AD1974 CODEC pins
DSDATA1,DSDATA2                pin 86, 87 istype 'com';
DSDATA3,DSDATA4                pin 91, 92 istype 'com';
DBCLK,DLRCLK                   pin 85, 84 istype 'com';
ASDATA1,ASDATA2                pin 80, 81 istype 'com';
ABCLK,ALRCLK                   pin 78, 79 istype 'com';

// 25-pin header connector HDR1 pins
HDR1_DSDATA1                   pin 20 istype 'com';
HDR1_DSDATA2                   pin 19 istype 'com';
HDR1_DSDATA3                   pin 17 istype 'com';
HDR1_DSDATA4                   pin 16 istype 'com';
HDR1_DBCLK                     pin 21 istype 'com';
HDR1_DLRCLK                    pin 22 istype 'com';
HDR1_ASDATA1                   pin 29 istype 'com, buffer';
HDR1_ASDATA2                   pin 28 istype 'com, buffer';
HDR1_ABCLK                     pin 30 istype 'com';
HDR1_ALRCLK                    pin 31 istype 'com';

// 25-pin header connector HDR2 pins
HDR2_DSDATA1                   pin 37 istype 'com';
HDR2_DSDATA2                   pin 36 istype 'com';
HDR2_DSDATA3                   pin 35 istype 'com';
HDR2_DSDATA4                   pin 34 istype 'com';
HDR2_DBCLK                     pin 41 istype 'com';
HDR2_DLRCLK                    pin 42 istype 'com';
HDR2_ASDATA1                   pin 44 istype 'com';
HDR2_ASDATA2                   pin 43 istype 'com, buffer';
HDR2_ABCLK                     pin 47 istype 'com';
HDR2_ALRCLK                    pin 48 istype 'com';

// S/PDIF Rx CS8414 pins
SDATA_8416                     pin 61 istype 'com';

```

```

BCLK_8416                pin 60 istype 'com';
LRCLK_8416                pin 59 istype 'com';
SOMS_RX,SFSEL1_RX,SFSEL0_RX,
RMCKF_RX pin 66,67,64,65 istype 'com';

// S/PDIF Tx CS8404 pins
SDATA_8406                pin 50 istype
'com';
BCLK_8406,LRCLK_8406      pin 53, 54 istype 'com';
MCLK_8406                pin 49 istype
'com';
APMS_TX,SFMT1_TX,SFMT0_TX pin 55,56,58 istype 'com';
CPLD_MCLK                pin 89 istype
'com';

// AD1974 SPI port pins
//CCLK,CDATA,CLATCH      pin 84, 83, 85 istype 'com';
//COUT                    pin 82 istype 'com';
//CLATCH2,CLATCH3,CLATCH4 pin 86, 56, 4 istype 'com';
//CONTROL_ENB            pin 81 istype
'com';

S/PDIF_RESET_OUT        pin 69 istype
'com';

// Switch S1, S2, S3 and S4 pins
ADC_CLK_OFF              pin 93 istype
'com'; // S2-1
ADC_CLK_SRC1             pin 94 istype 'com'; // S2-2
ADC_CLK_SRC0             pin 97 istype 'com'; // S2-3
DAC_CLK_OFF              pin 98 istype
'com'; // S2-4
DAC_CLK_SRC1             pin 99 istype 'com'; // S2-5
DAC_CLK_SRC0             pin 100 istype 'com'; // S2-6
S/PDIF_MCLK_RATE        pin 3 istype 'com'; // S2-7
S/PDIF_RESET_IN         pin 4 istype 'com'; // S2-8

MODE11,MODE12,MODE13,MODE14 pin 5,6,8,9 istype 'com'; // S4
STAND_ALONE,MODE22,MODE23,MODE24 pin 10,11,14,15 istype 'com'; // S5

"NODES
I_DSDATA1, I_DSDATA2, I_DSDATA3, I_DSDATA4 node istype 'com';
I_DBCLK, I_DLRCLK        node istype 'com';
I_ASDATA1, I_ASDATA2     node istype 'com, buffer';
I_ABCLK, I_ALRCLK        node istype 'com';
Qdivide                  node istype 'reg, buffer';

```

```
//=====
"MACROS

// Switch S3, DIP POSITIONS 6 AND 7

ADC_HDR_NORMAL      = ( MODE22 & MODE23);
ADC_HDR_DATA2_DATA1 = ( MODE22 & !MODE23);
ADC_HDR_TDM         = (!MODE22 & MODE23);
ADC_HDR_AUX         = (!MODE22 & !MODE23);

S/PDIF_OUT_MUX = MODE24;

// HEX Switch S4

                // S4 position 0,
DAC_RX_ALL  =  ( MODE14 & MODE13 & MODE12 & MODE11);

                // S4 position 1,
DAC_RX_1    =  ( MODE14 & MODE13 & MODE12 & !MODE11);

                // S4 position 2,
DAC_RX_2    =  ( MODE14 & MODE13 & !MODE12 & MODE11);

                // S4 position 3,
DAC_RX_3    =  ( MODE14 & MODE13 & !MODE12 & !MODE11);

                // S4 position 4,
DAC_RX_4    =  ( MODE14 & !MODE13 & MODE12 & MODE11);

                // S4 position 5,
NA1  =  ( MODE14 & !MODE13 & MODE12 & !MODE11);

                // S4 position 6,
NA2  =  ( MODE14 & !MODE13 & !MODE12 & MODE11);

                // S4 position 7,
DAC_DATA_ZERO = ( MODE14 & !MODE13 & !MODE12 & !MODE11);

                // S4 position 8,
DAC_HDR1_ALL  = ( !MODE14 & MODE13 & MODE12 & MODE11);

                // S4 position 9,
DAC_HDR1_IND  = ( !MODE14 & MODE13 & MODE12 & !MODE11);

                // S4 position A,
DAC_HDR1_TDM  = ( !MODE14 & MODE13 & !MODE12 & MODE11);
```

```

        // S4 position B,
DAC_DUAL_TDM = ( !MODE14 & MODE13 & !MODE12 & !MODE11);

        // S4 position C,
DAC_HDR1_AUX = ( !MODE14 & !MODE13 & MODE12 & MODE11);

        // S4 position D,
NA3 = ( !MODE14 & !MODE13 & MODE12 & !MODE11);

        // S4 position E,
NA4 = ( !MODE14 & !MODE13 & !MODE12 & MODE11);

        // S4 position F,
DAC_DATA_HIZ = ( !MODE14 & !MODE13 & !MODE12 & !MODE11);

// Switch S2

DAC_S/PDIF = (DAC_CLK_SRC1 & DAC_CLK_SRC0);
DAC_HDR1 = (DAC_CLK_SRC1 & !DAC_CLK_SRC0);
DAC_ADC = (!DAC_CLK_SRC1 & DAC_CLK_SRC0);
DAC_DAC = (!DAC_CLK_SRC1 & !DAC_CLK_SRC0);

ADC_S/PDIF = (ADC_CLK_SRC1 & ADC_CLK_SRC0);
ADC_HDR1 = (ADC_CLK_SRC1 & !ADC_CLK_SRC0);
ADC_ADC = (!ADC_CLK_SRC1 & ADC_CLK_SRC0);
ADC_DAC = (!ADC_CLK_SRC1 & !ADC_CLK_SRC0);

"=====
EQUATIONS

S/PDIF_RESET_OUT = S/PDIF_RESET_IN;

// Configuration of the CS8416, changes active on reset, BCLK_8416 and LRCLK_8416 are bi-
directional signals.
SOMS_RX = DAC_S/PDIF;
// SOMS = Serial Output Master/Slave Select
SFSEL1_RX = 0; //DIR_RJ # DIR_RJ16;
// SFSEL1 = Serial Format Select 1
SFSEL0_RX = 1; //DIR_I2S # DIR_DSP;
// SFSEL0 = Serial Format Select 0
RMCKF_RX = !S/PDIF_MCLK_RATE; // RMCKF =
Receive Master Clock Frequency

// M0_8414 = (0 # !DAC_S/PDIF);
// M1_8414 = 1;
// M2_8414 = 0;

```

```

// M3_8414 = 0;

// CS8404 Tx interface mode select
                APMS_TX = 0; // Tx serial port is always slave in this application
                SFMT1_TX = 0; // Tx data format is I2S always
                SFMT0_TX = 1;

// M0_8404 = 0;
// M1_8404 = 0;
// M2_8404 = 1; // I2S format only

// divide 256Fs clock by 2 for 128Fs clock to the the S/PDIF Tx
// Qdivide.clk = CPLD_MCLK;
// Qdivide.d = !Qdivide;

// MCLK_8406 = Qdivide;
                MCLK_8406 = CPLD_MCLK;

BCLK_8406 = I_ABCLK;
LRCLK_8406 = I_ALRCLK;
SDATA_8406 = (ASDATA1 & S/PDIF_OUT_MUX) # (ASDATA2 & !S/PDIF_OUT_MUX);

// For SPI mode, let external port drive the SPI port

DBCLK.oe = (DAC_S/PDIF # DAC_HDR1 # DAC_ADC # !DAC_DAC) & (DAC_CLK_OFF);
DLRCLK.oe = (DAC_S/PDIF # DAC_HDR1 # DAC_ADC # !DAC_DAC) & (DAC_CLK_OFF);
ABCLK.oe = (ADC_S/PDIF # ADC_HDR1 # !ADC_ADC # ADC_DAC) & (ADC_CLK_OFF);
ALRCLK.oe = (ADC_S/PDIF # ADC_HDR1 # !ADC_ADC # ADC_DAC) & (ADC_CLK_OFF);

HDR1_DBCLK.oe = (DAC_S/PDIF # !DAC_HDR1 # DAC_ADC # DAC_DAC);
HDR1_DLRCLK.oe = (DAC_S/PDIF # !DAC_HDR1 # DAC_ADC # DAC_DAC);
HDR1_ABCLK.oe = (ADC_S/PDIF # !ADC_HDR1 # ADC_ADC # ADC_DAC);
HDR1_ALRCLK.oe = (ADC_S/PDIF # !ADC_HDR1 # ADC_ADC # ADC_DAC);

BCLK_8416.oe = (!DAC_S/PDIF);
LRCLK_8416.oe = (!DAC_S/PDIF);
BCLK_8416 = I_DBCLK;
LRCLK_8416 = I_DLRCLK;

DSDATA1.oe = (!DAC_DATA_HIZ);
DSDATA2.oe = (!(DAC_HDR1_TDM # DAC_DUAL_TDM # DAC_DATA_HIZ)); //DSDATA2 is output in DAC
TDM-daisy chain mode
DSDATA3.oe = (!DAC_DATA_HIZ);
DSDATA4.oe = (!(DAC_DUAL_TDM # ADC_HDR_AUX # DAC_HDR1_AUX # DAC_DATA_HIZ)); // SECOND
TDM-OUT IN DUAL LINE DAC TDM MODE
ASDATA2.oe = (ADC_HDR_TDM); //ASDATA2 is input in ADC TDM mode

HDR1_DSDATA2.oe = (DAC_HDR1_TDM # DAC_DUAL_TDM);

```



```

HDR1_DSDATA4.oe = (DAC_DUAL_TDM # ADC_HDR_AUX # DAC_HDR1_AUX);
HDR1_ASDATA2.oe = (!ADC_HDR_TDM);

DBCLK      = I_DBCLK;
DLRCLK     = I_DLRCLK;
ABCLK      = I_ABCLK;
ALRCLK     = I_ALRCLK;

DSDATA1    = (HDR1_DSDATA1 & (DAC_HDR1_ALL # DAC_HDR1_IND # DAC_RX_2 # DAC_RX_3 # DAC_RX_4 #
DAC_HDR1_TDM # DAC_DUAL_TDM # ADC_HDR_AUX))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_1)) # (0 & DAC_DATA_ZERO);
DSDATA2    = (HDR1_DSDATA1 & DAC_HDR1_ALL) # (HDR1_DSDATA2 & (DAC_HDR1_IND # ADC_HDR_AUX #
DAC_HDR1_AUX # DAC_RX_1 # DAC_RX_3 # DAC_RX_4))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_2)) # (0 & DAC_DATA_ZERO);
DSDATA3    = (HDR1_DSDATA1 & (DAC_HDR1_ALL)) # (HDR1_DSDATA3 & (DAC_HDR1_IND # DAC_DUAL_TDM #
ADC_HDR_AUX # DAC_HDR1_AUX # DAC_RX_1 # DAC_RX_2 # DAC_RX_4))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_3)) # (0 & DAC_DATA_ZERO);
DSDATA4    = (HDR1_DSDATA1 & (DAC_HDR1_ALL)) # (HDR1_DSDATA4 & (DAC_HDR1_IND # DAC_RX_1 #
DAC_RX_2 # DAC_RX_3))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_4)) # (0 & DAC_DATA_ZERO);

HDR1_DBCLK  = I_DBCLK;
HDR1_DLRCLK = I_DLRCLK;
HDR1_ABCLK  = I_ABCLK;
HDR1_ALRCLK = I_ALRCLK;

HDR1_ASDATA1 = (ASDATA1 & (ADC_HDR_NORMAL # ADC_HDR_TDM # ADC_HDR_AUX # DAC_HDR1_AUX )) #
(ASDATA2 & ADC_HDR_DATA2_DATA1);
HDR1_ASDATA2 = ASDATA2;
ASDATA2      = HDR1_ASDATA2;

HDR1_DSDATA2 = DSDATA2;
HDR1_DSDATA4 = DSDATA4;

// Internal node signals
I_DBCLK      = (BCLK_8416 & DAC_S/PDIF) # (HDR1_DBCLK & DAC_HDR1) # (DBCLK & DAC_DAC) #
(I_ABCLK & DAC_ADC);

I_DLRCLK     = (LRCLK_8416 & DAC_S/PDIF) # (HDR1_DLRCLK & DAC_HDR1) # (DLRCLK & DAC_DAC) #
(I_ALRCLK & DAC_ADC);

I_ABCLK      = (BCLK_8416 & ADC_S/PDIF) # (HDR1_ABCLK & ADC_HDR1) # (ABCLK & ADC_ADC) #
(I_DBCLK & ADC_DAC);

I_ALRCLK     = (LRCLK_8416 & ADC_S/PDIF) # (HDR1_ALRCLK & ADC_HDR1) # (ALRCLK & ADC_ADC) #
(I_DLRCLK & ADC_DAC);
"=====
END IF_Logic

```

## ORDERING INFORMATION

## BILL OF MATERIALS

Table 1.

Qty	Designator	Description	Manufacturer	Part Number
18	C85, C90 to C94, C101 to C103, C107, C108, C110, C115, C116, C121, C127, C132, C134	Multilayer ceramic capacitor, 16 V, X7R (0402)	Panasonic EC	ECJ-0EX1C104K
46	C2, C5, C8 to C10, C20, C21, C28, C29, C38, C42, C48 to C51, C58 to C60, C62, C64, C69, C73, C76, C79, C82, C99, C112, C118, C128, C135, C146, C147, C149, C151, C155, C156, C158, C162, C168, C174, C176, C177, C193, C194, C197, C203	Multilayer ceramic capacitor, 50 V, X7R (0603)	Panasonic EC	ECJ-1VB1H104K
9	C37, C65, C67, C83, C88, C124, C129, C157, C160	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Panasonic EC	ECJ-1VC1H102J
12	R28, R30, R51, R59, R166, R167, R169, R172, R185, R189, R212, R214	Chip resistor, 100 k $\Omega$ , 1%, 125 mW, thick film (0603)	Panasonic EC	ERJ-3EKF1003V
8	C68, C71, C87, C89, C130, C138, C159, C161	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Panasonic EC	ECJ-1VC1H101J
16	R24, R31, R44, R60, R77, R84, R93, R106, R136, R149, R159, R170, R180, R191, R207, R217	Chip resistor, 100 k $\Omega$ , 1%, 100 mW, thick film (0603)	Panasonic EC	ERJ-3EKF1000V
1	C84	Aluminum electrolytic capacitor, 100 $\mu$ F, 16 V, FC, 105 deg, SMD_E	Panasonic EC	EEE-FC1C101P
32	R6, R7, R13, R14, R18, R20, R40, R43, R47 to R49, R54, R55, R63, R64, R74, R78, R80, R82, R102, R117, R158, R164, R173, R176, R177, R184, R186, R224 to R227	Chip resistor, 10 k $\Omega$ , 1%, 125 mW, thick film (0603)	Panasonic EC	ERJ-3EKF1002V
3	C6, C39, C40	Multilayer ceramic capacitor, 25 V, NP0 (0603)	TDK Corp	C1608C0G1E103J
12	C15 to C17, C81, C86, C95, C98, C170, C175, C178, C180, C183	Multilayer ceramic capacitor, 100 V, NP0 (0603)	Panasonic EC	ECJ-1VC2A100D
12	C104, C106, C109, C111, C117, C123, C140 to C145	Multilayer ceramic capacitor, 50 V, NP0 (0402)	Kemet	C0402C100J5GACTU
2	C4, C74	Aluminum electrolytic capacitor, 16 V, FC, 105 deg, SMD_B	Panasonic EC	EEE-FC1C100R
4	C61, C77, C113, C150	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Panasonic EC	ECJ-1VC1H121J
3	D1, D3, D4	TVS Zener, 15 V, 600 W, SMB	ON Semiconductor	1SMB15AT3G
9	C23, C33, C43, C55, C114, C166, C184, C188, C200	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Murata Electronics	GRM1885C1H222JA01D
1	C36	Multilayer ceramic capacitor, 25 V, NP0 (0805)	Murata ENA	GRM21B5C1H223JA01L
2	C153, C154	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Panasonic EC	ECJ-1VC1H220J
8	R76, R81, R90, R101, R134, R141, R157, R168	Chip resistor, 237 $\Omega$ , 1%, 125 mW, thick film (0603)	Panasonic EC	ERJ-3EKF2370V
2	R4	Chip resistor, 243 $\Omega$ , 1%, 100 mW, thick film (0603)	Panasonic EC	ERJ-3EKF2430V
10	R91, R94, R98, R99, R108, R109, R114, R115, R118, R123	Chip resistor, 24.9 $\Omega$ , 1%, 63 mW, thick film (0402)	Rohm	MCR01MZPF24R9

Qty	Designator	Description	Manufacturer	Part Number
16	R56, R57, R65, R66, R88, R89, R140, R154, R179, R183, R213, R216, R228 to R231	Chip resistor, 24.9 $\Omega$ , 1%, 100 mW, thick film (0603)	Rohm	MCR03EZPFX24R9
8	C25, C31, C45, C53, C169, C181, C190, C198	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Rohm	MCH185A271JK
3	R3, R11, R58	Chip resistor, 374 $\Omega$ , 1%, 100 mW, thick film (0603)	Rohm	MCR03EZPFX3740
1	C125	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Panasonic EC	ECJ-1VC1H391J
4	R5, R52, R53, R75	Chip resistor, 392 $\Omega$ , 1%, 100 mW, thick film (0603)	Rohm	MCR03EZPFX3920
1	C120	Multilayer ceramic capacitor, 16 V, ECH-U (1206)	Panasonic EC	ECH-U1C393JB5
33	R38	Chip resistor, 3.01 k $\Omega$ , 1%, 100 mW, thick film (0603)	Rohm	MCR03EZPFX3011
1	R129	Chip resistor, 3.32 k $\Omega$ , 1%, 100 mW, thick film (0603)	Rohm	MCR03EZPFX3321
8	C24, C34, C44, C56, C167, C185, C189, C201	Multilayer ceramic capacitor, 50 V, NP0 (0603)	Murata ENA	GRM1885C1H431JA01D
30	C11, C14, C22, C26, C27, C30, C32, C35, C41, C46, C47, C52, C54, C57, C63, C66, C72, C75, C80, C105, C119, C133, C139, C148, C152, C164, C172, C179, C191, C196	Aluminum electrolytic capacitor, 16 V, FC, 105 deg, SMD_D	Panasonic EC	EEE-FC1C470P
3	C12, C18, C19	Aluminum electrolytic capacitor, FC, 105 deg, SMD_E	Panasonic EC	EEE-FC1E470P
4	R83, R96, R148, R163	Chip resistor, 49.9 k $\Omega$ , 1%, 100 mW, thick film (0603)	Panasonic EC	ERJ-3EKF4992V
20	R103, R104, R110 to R112, R116, R119, R124, R126 to R128, R130 to R132, R142 to R147	Chip resistor, 49.9 k $\Omega$ , 1%, 63 mW, thick film (0402)	Rohm	MCR01MZPF49R9
35	R8 to R10, R15 to R17, R19, R92, R95, R100, R105, R113, R120, R125, R133, R135, R139, R153, R155, R156, R160, R174, R175, R178, R187, R188, R190, R194, R196, R200, R201, R203, R206, R210, R215	Chip resistor, 49.9 k $\Omega$ , 1%, 100 mW, thick film (0603)	Panasonic EC	ERJ-3EKF49R9V
16	R25, R26, R32, R34, R45, R46, R61, R68, R181, R182, R192, R195, R208, R209, R218, R220	Chip resistor, 49.9 k $\Omega$ , 1%, 100 mW, thick film (0603)	Panasonic EC	ERJ-3EKF4641V
16	R21 to R23, R27, R33, R35 to R37, R39, R41, R42, R50, R62, R69 to R71	Chip resistor, 49.9 k $\Omega$ , 1%, 100 mW, thick film (0603)	Panasonic EC	ERJ-3EKF4751V
1	C131	Multilayer ceramic capacitor, 25 V, NP0 (0603)	TDK Corp	C1608C0G1E562J
1	R138	Chip resistor, 562 $\Omega$ , 1%, 125 mW, thick film (0603)	Panasonic EC	ERJ-3EKF5620V
16	R72, R73, R79, R85 to R87, R97, R107, R121, R122, R137, R150 to R152, R165, R171	Chip resistor, 5.76 k $\Omega$ , 1%, 125 mW, thick film (0603)	Panasonic EC	ERJ-3EKF5761V
4	C78, C137, C171, C195	Multilayer ceramic capacitor, 100 V, NP0 (0603)	Panasonic EC	ECJ-1VC2A680J
1	U11	IC inverter, hex, TTL/LSTTL, 14 SOIC	NXP Semi	74HC04D-T
2	U19, U26	IC buffer, quad, three state, 14 SOIC	Texas Instruments	SN74LV125AD
1	R29	Chip resistor, 75 $\Omega$ , 1%, 100 mW, thick film (0603)	Panasonic EC	ERJ-3EKF75R0V
1	R67	Chip resistor, 90.9 $\Omega$ , 1% 100 mW, thick film (0603)	Rohm	MCR03EZPFX90R9

Qty	Designator	Description	Manufacturer	Part Number
1	Y1	Crystal, 12.288 MHz, SMT, 10 pF	Abracon Corp	ABM3B-12.288MHZ-10-1-U-T
1	U15	Four ADC/eight DAC with PLL, 192 kHz, 24-bit CODEC	Analog Devices	AD1974YSTZ
1	U23	Microprocessor voltage supervisor	Analog Devices	ADM811RARTZ-REEL7
1	U1	Voltage regulator, low dropout	Analog Devices	ADP3303ARZ-3.3
1	J2	5-way binding post, black, uninsulated base TH	Deltron Components	552-0100 BLK
1	J3	5-way binding post, mini, green, uninsulated base TH	Deltron Components	552-0400 GRN
1	J4	5-way binding post, mini, red, uninsulated base TH	Deltron Components	552-0500 RED
2	J22, J23	SMA receptacle, straight PCB mount	Amp-RF Division	901-144-8RFX
1	U8	192 kHz digital audio receiver (DGTL RCVR 28-TSSOP)	Cirrus Logic	CS8416-CZZ
1	U13	192 kHz digital audio interface (S/PDIF transmitter)	Cirrus Logic	CS8406-CZZ
2	D2, D5	Passivated rectifier, 1 A, 50 V, MELF	Micro Commercial	DL4001-TP
1	S1	Switch slide, DP3T, PC MNT, L = 4 mm	E-Switch	EG2305
1	SW1	DPDT slide switch, vertical	E-Switch	EG2207
6	L2 to L7	Chip ferrite bead, 600 $\Omega$ at 100 MHz	TDK	MPZ1608S601A
1	L1	Chip ferrite bead, 600 $\Omega$ at 100 MHz	Steward	HZ0805E601R-10
2	J1, J14	10-way shrouded polarized header	3M	N2510-6002RB
4	J15 to J18	16-way unshrouded, not populated	3M	N/A
1	J19	Connector header, 0.100 dual STR, 72 POS	Sullins	PBC10DAAN; or cut PBC36DAAN
2	J20, J26	Connector header, 0.100 dual STR, 72 POS	Sullins	PBC13DAAN; or cut PBC36DAAN
4	J5 to J8	Connector header, 0.100 dual STR, 72 POS	Sullins	PBC06DAAN; or cut PBC36DAAN
2	S4, S5	16-position rotary switch, hex	APEM	PT65503
19	JP4 to JP7, JP11 to JP14, JP17, JP18, JP20 to JP22, JP24, JP26, JP28 to JP31	2-pin header, unshrouded jumper, 0.10"; use shunt Tyco 881545-2	Sullins	PBC02SAAN; or cut PBC36SAAN
11	JP1 to JP3, JP8 to JP10, JP15, JP19, JP23, JP25, JP27	3-position SIP header	Sullins	PBC03SAAN; or cut PBC36SAAN
1	U16	Complex programmable logic devices (CPLD), HI PERF, E2CMOS, PLD	Lattice Semiconductor	LC4128V-75TN100C
1	D11	Green, diffused, 10 millicandela, 565 nm (1206)	Lumex Opto	SML-LX1206GW-TR
2	D6, D9	Red, diffused, 6.0 millicandela, 635 nm (1206)	Lumex Opto	SML-LX1206IW-TR
2	D7, D10	Yellow, diffused, 4.0 millicandela, 585 nm (1206)	CML Innovative Tech	CMD15-21VYD/TR8
2	U2, U3	3-terminal, adjustable voltage regulator, DPak	STMicroelectronics	LM317MDT-TR
6	J10, J11, J13, J21, J27, J28	Stereo mini jack, SMT	CUI	SJ-3523-SMT
2	R161, R162	Resistor network, bussed 9 res	CTS	773091103
8	U6, U9, U12, U14, U17, U20, U24, U25	Dual bipolar/JFET audio op amp.	Analog Devices	OP275GSZ
1	U21	12.288 MHz fixed SMD oscillator, 1.8 V dc to 3.3 V dc	Abracon Corp	AP3S-12.288MHz-F-J-B
2	J9, J12	RCA jack, PCB, TH mount, R/A, yellow	Connect-Tech Products	CTP-021A-S-YEL

Qty	Designator	Description	Manufacturer	Part Number
1	U10	110 Ω AES/EBU transformer	Scientific Conversion	SC937-02
2	U18, U22	Buffer, three-state, single gate	Texas Instruments	SN74LVC1G125DRLR
1	U4	Octal, three-state buffer/driver	Texas Instruments	SN74LVC541ADBR
2	SW2, SW3	SPDT slide switch PC mount	E-Switch	EG1218
2	S2, S3	8-position SPST SMD switch, flush, actuated	CTS Corp	219-8LPST
1	S6	Tact switch, 6 mm gull wing	Tyco/Alcoswitch	FSM6JSMA
1	U5	15 Mb/sec fiber optic receiving module with shutter	Toshiba	TORX147L(F,T)
1	U7	Fiber optic transmit module, 15 Mb/sec	Toshiba	TOTX147L(F,T)
60	TP1 to TP6, TP8 to TP10, TP12 to TP15, TP17, TP19 to TP23, TP25 to TP52, TP54 to TP60, TP62, TP64 to TP68	Mini test point, white, 0.1 inch, OD	Keystone Electronics	5002

**NOTES**

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## NOTES

**ESD Caution**

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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