LTC4226
Wide Operating Range Dual Hot Swap Controller

DESCRIPTION

Demonstration circuit 1627A is intended to display the Hot Swap™ functionality of the LTC®4226 wide operating range dual Hot Swap controller. The DC1627A has two independent circuits, each for two rails. The circuit placed on the upper board area is for a high current load.

The first channel of the upper board circuit operates with a 10A maximum in the +12V rail while the second channel operates with a 5A maximum in the +5V rail. Provision is made for the installation of several MOSFET packages to test the LTC4226's performance during a short time with the larger current. Circuit LEDs indicate a presence of the input rail voltages and fault conditions in each rail. There are two jumpers: one for the current limit multiplicity selection and the other one for overvoltage protection configuration.

The circuit located on the lower board area is a special compact circuit for the Apple FireWire/IEEE 1394 power distribution.

Both channels of this circuit operate with a 1.25A maximum current in the 12V rails. It is not recommended to use this circuit for other operating conditions.

There are two versions of the controller: LTC4226-1 and LTC4226-2. The LTC4226-1 remains off after a fault while the LTC4226-2 automatically retries after a 0.5 second delay.

The DC1627A allows estimating the performance of the LTC4226 in different operation modes such as ramp-up, steady-state, and overcurrent fault conditions.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Upper Circuit +12V Channel						
V_{CC1}	Input Supply Range		9.79	12	16	V
$V_{CC1(UV)}$	Input Supply Undervoltage	V_{CC} Rising; Based on the ON1 Pin Threshold	9.15	9.79	10.53	V
$V_{CC1(OV)}$	Input Supply Overvoltage	V_{CC} Rising	15.4	16	17	V
S1	Output Voltage Slew Rate	No Current Limit	12000			V/s
I_{CB1}	Circuit Breaker Current Limit		8.91	10	11.11	A
t_{CB1}	Timer Period During Circuit Breaker Operation		19	29	48	ms
I_{LIM1}	Current Limit by Current Limit (CL) Amplifier	CLS = 0V (1.5×) CLS = Open (2×) CLS = 3V (3×)	13.86 18.42 38.2	17.2 23 34.6	20.80 27.47 41.4	A A A
t_{FTMR1}	Fault Timer Period During CL operation	CLS = 0V (1.5×) CLS = Open (2×) CLS = 3V (3×)	2 1.12 0.5	2.9 1.6 0.7	4.6 2.6 1.15	ms ms ms
Upper Circuit +5V Channel						
V_{CC2}	Input Supply Range		4.11	5	7.3	V
$V_{CC2(UV)}$	Input Supply Undervoltage	V_{CC} Rising; Based on the ON2 Pin Threshold	3.86	4.11	4.37	V
$V_{CC2(OV)}$	Input Supply Overvoltage	V_{CC} Rising	6.8	7.3	7.7	V
S2	Output Voltage Slew Rate	No Current Limit	12000			V/s

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CB2}	Circuit Breaker Current Limit		4.45	5	5.55	A
t_{CB2}	Timer Period During Circuit Breaker Operation		39	50	80	ms
I_{LIM2}	Current Limit by CL Amplifier	CLS = 0V (1.5×) CLS = Open (2×) CLS = 3V (3×)	6.9 9.2 13.8	8.6 11.5 17.3	10.4 13.7 20.7	A A A
t_{FTMR2}	Fault Timer Period	CLS = 0V (1.5×) CLS = Open (2×) CLS = 3V (3×)	3.3 1.9 0.8	5.1 2.8 1.3	8.4 4.7 2.1	ms ms ms
Compact Circuit for FireWire Power Distribution						
V_{CC}	Input Supply Range	Based on the ON Pin Threshold	4.62		16.7	V
$V_{CC(UV)}$	Input Supply Undervoltage	V_{CC} Rising	4.62	4.96	5.28	V
I_{CB}	Circuit Breaker Current Limit		1.35	1.51	1.68	A
t_{CB}	Timer Period During Circuit Breaker Operation		6.07	9.2	15.3	ms
I_{LIM}	Current Limit by CL Amplifier	CLS = 0V (1.5×) CLS = Open (2×) CLS = 3V (3×)	2.1 2.8 4.2	2.6 3.5 5.3	3.2 4.2 6.3	A A A
t_{FTMR}	Fault Timer Period	CLS = 0V (1.5×) CLS = Open (2×) CLS = 3V (3×)	0.6 0.35 0.15	0.9 0.5 0.25	1.6 0.9 0.39	ms ms ms

OPERATING PRINCIPLES

The LTC4226 controls two rails with external N-channel MOSFETs. Two independent ON*n* comparators allow ramping rails up and down independently.

During normal operation, the charge pump delivers 9µA to the gate driver to turn on the external N-channel MOSFET.

Each channel's circuit breaker (CB) comparator and current limit (CL) amplifier monitor the load current using the sense resistor voltage between the V_{CC}*n* and the SENSE*n* pins. When the sense resistor voltage exceeds circuit breaker threshold (V_{CB}), (but lower than V_{LIMIT}) the CB comparator enables a 2µA current source, and the voltage at the fault timer (FTMR*n*) capacitor ramps up. When the FTMR*n* comparator voltage reaches 1.23V threshold, the corresponding MOSFET is turned off.

When the sense resistor voltage exceeds V_{LIMIT}, the CL amplifier limits the current in the load by reducing the gate-to-out voltage in an active control loop. The fast response CL amplifier can quickly adjust the gate-to-out voltage in the event of an output-to-ground short circuit. The FTMR*n* capacitor voltage ramps up with a 20µA (or 36µA, or 80µA) current source instead of the 2µA in the active current limiting. By this means, the timer period during an active current limit is ten times less than it is in the circuit breaker operation.

The LTC4226-1 latches off after the MOSFET is turned off under an overcurrent condition. The ON pin status must be recycled low to high for the gate drive to restart. The demo board with LTC4226-1 is labeled as DC1627A-A.

The LTC4226-2 automatically retries after an overcurrent condition. It begins with a 0.5 second delay before resetting the fault timer with a 100µA pull-down, followed by gate restart if ON pin is high. The demo board with LTC4226-2 is labeled as DC1627A-B.

Both channels share a common current limit select functionality with the current limit select (CLS) pin signal. This signal can have three input states: low, open and high. The three input states correspond to the preset current limit values. V_{LIMIT} becomes 1.5×, or 2.0×, or 3.0× of 1.15× V_{CB}.

Undervoltage protection in the upper circuit is based on the ON*n* pin threshold. The resistors of each ON*n* pin divider are selected to have a threshold voltage at the LTC4226 ON

OPERATING PRINCIPLES

pin, when the input voltage equals the defined minimum. The Performance Summary table shows their values with consideration for the voltage tolerance of the comparator threshold and for 1% resistor tolerance.

Overvoltage protection in the upper circuit is built with Zener and Schottky diodes to trigger an artificial overcurrent mode by charging the FTMR capacitor. Due to the peculiar current leakage of some devices and their sensitivity to higher temperature a small initial voltage (0.1V to 0.2V) on the FTMR capacitor can be found. It lowers the time in current limit mode. Overvoltage protection levels shown in the Performance Summary table were obtained by simulation.

Inherent in the LTC4226 is an undervoltage protection feature that allows the channels to operate only if V_{CC} is above 3.7V. When V_{CC} rises above the undervoltage lockout level, there is a delay of 50ms before the gate starts to ramp.

QUICK START PROCEDURE

The test procedure for each channel of the LTC4226 is identical and includes verification of the main circuit parameters:

- S1-S2 output voltage slew rate;
- I_{CB1}-I_{CB2} circuit breaker level performed by the circuit breaker and fault timer period (FTMR), when an overcurrent mode is initiated after power up has been completed;
- I_{CL1}-I_{CL2} the current limit level performed by the current limit amplifier and fault timer period (FTMR) with an initially shorted output and CLS pin grounded.

If there is a need to test a channel with rail voltages other than those used for the DC1627A design (+5V, and +12V), make changes to the appropriate ON pin signal divider (R5, R10, R12 for channel 1 or R23, R29, and R31 for channel 2).

If any LTC4226 channel should operate at other than a factory assigned current, change the value of the sense resistor (R2, R22) and select the desired position for the current limit selection (CLS) jumper. Verify the power MOSFET current capability in the steady-state and in the power-up modes. Replace Q1 or Q3 with a suitably packaged MOSFET.

Demonstration circuit DC1627A is easy to set up to evaluate the performance of the each LTC4226 Hot Swap channel. Refer to Figure 1 for the proper measurement equipment setup for one channel and follow the procedure listed next.

UPPER CIRCUIT TEST

Jacks and Joined Turrets

- J1 (VCC1): 12V supply input; do not exceed 35V
- J2 (GND): Ground connection for 12V input supply
- J3 (OUT1): Output for 12V rail
- J4 (GND): Ground connection for 12V output
- J5 (VCC2): 5V supply input; do not exceed 35V
- J6 (GND): Ground connection for 5V input supply
- J7 (OUT2): Output for 5V rail
- J8 (GND): Ground connection for 5V output

Turrets Connected to Controller Pins

- E3 (ON1)
- E4 (FTMR1)
- E5 (CLS)
- E6 ($\overline{\text{FAULT1}}$)
- E7 ($\overline{\text{FAULT2}}$)
- E8 (FTMR2)
- E11 (ON2)
- E26 (DCLA)

Jumpers

JP1 (CLS): Current limit selection: Use 1.5X position to have 1.725X circuit breaker current limit (CBCL); use 2X position to have 2.3X CBCL; use 3X position to have 3.45X CBCL.

QUICK START PROCEDURE

JP2 (OVBLK): Overvoltage blocking selection: Use SEP position for individual channel blocking under overvoltage condition; use BOTH position for both channel blocking under any channel's overvoltage condition.

LEDs

- D3 (green): +12V supply is present
- D15 (green): +5V supply is present
- D7 (red): +12V channel fault
- D9 (red): +5V channel fault

+12V Hot Swap

As the test procedures for all LTC4226 channels are identical, the following detailed description of the steps for +12V channel test can be used for the other DC1627's channels with the only difference being the mentioned component designators.

1. The jumpers' shunts should be placed in the following position:

   JP1 (CLS) 1.5×

   JP2 (OVBLK) SEP

   Connect ON1 and GND turrets with an external wire to disable the +12V Hot Swap circuit.

2. Connect the +12V supply terminals to the +12V and GND demo board jacks appropriately and place scope probes on the OUT1 and FTMR1 turrets and a current probe to measure the +12V wire current.

   Turn on the +12V supply. +12V green LED (D3) will light indicating the presence of input voltage. Disconnect the ON1 and GND turrets to provide an ON1 pin signal, and verify that the output voltage rises in less than 1ms.

3. Keep the scope probes and current probe in the same place. Initiate +12V channel operation with no load, gradually increasing the load current with an electronic or resistive load and verify that the circuit breaker is in the range of 8.9A to 11.11A and the timer period is between 19ms and 48ms. Disable the +12V channel by connecting the ON1 and GND turrets.

4. With the +12V channel disabled, short the output to GND with an external wire. Monitor the current in the shorting wire with a current probe. Place the scope probes on the V_{CC1} and FTMR1 turrets. Enable the channel with an ON1 pin signal and verify that current is limited in the range 13.86A to 20.8A and current limit mode takes from 2ms to 4.6ms.

   The upper circuit provides options for current limit selection (CLS JP1) and overvoltage protection (JP OVBLK).

   Three positions of the current limit selection (CLS) jumper (JP1) correspond with the three pair of current limit parameters: current level and timer period. Estimated values for these parameters are shown in the Performance Summary table.

   Special attention should be given to verification of the MOSFET's SOA regarding these parameters.

5. Each channel's overvoltage protection circuit can block its own channel if the OVBLK jumper header is installed in the position SEP, or both channels if the OVBLK is in the position BOTH. The +12V rail overvoltage protection is in the 15.4V to 17V range, and +5V rail is in the 6.8V to 7.7V range.

   To test the overvoltage protection level place a scope probe at the FTMR turret and start to gradually increase the input voltage. The protection level is estimated when FTMR voltage reaches threshold and drops low. It means that an auxiliary overcurrent mode has been generated.

+5V Hot Swap

6. The jumpers' shunts should be placed in the following position:

   JP1 (CLS) 1.5×

   JP2 (OVBLK) SEP

   Connect ON2 and GND turrets with an external wire to disable the +5V Hot Swap circuit.

QUICK START PROCEDURE

7. Connect the +5V supply terminals to the +5V and GND demo board jacks appropriately and place scope probes on the OUT2 and FTMR2 turrets and current probe to measure the +5V wire current.

   Turn on the +5V supply. +5V green LED (D15) will light up indicating the presence of input voltage. Disconnect the ON2 and GND turrets to provide an ON2 pin signal, and verify that the output voltage rises in less than 1ms.

8. Keeping the scope probes and current probe in the same place, initiate +5V channel operation with no load, gradually increasing the load current with an electronic or resistive load and verify that the circuit breaker is in the range of 4.45A to 5.55A and timer period is from 39ms to 80ms. Disable the +5V channel by connecting the ON2 and GND turrets.

9. With the +5V channel disabled, short the output to GND with an external wire. Monitor the current in the shorting wire with a current probe. Place the scope probes on the V_{CC2} and FTMR2 turrets. Enable the channel with an ON2 pin signal and verify that current is limited in the range of 6.9A to 10.4A and current limit mode takes from 3.3ms to 8.4ms.

10. Confirm that each position of the current limit jumper corresponds to the appropriate current limit level and timer period. Special attention should be given to verification of the MOSFET's SOA regarding these parameters.

COMPACT CIRCUIT TEST

Turrets

- E1 and E16: Circuit GND
- E13: 1st channel +12V supply input; do not exceed 35V
- E14 (OUT1): 1st channel output
- E15: 2nd channel +12V supply input; do not exceed 35V
- E17 (ON1)
- E18 (FTMR1)
- E19 (CLS)
- E20 (FAULT1)
- E21 (FAULT2)
- E22 (FTMR2)
- E23 (ON2)
- E24 (OUT2)

Connect ON1 and GND turrets with an external wire to disable the +12V hot swap circuit. Connect CLS and GND turrets to select the lowest CL level.

1. Connect the +12V supply terminals to the +12V and GND demo board turrets. Place scope probes on the OUT1 and FTMR1 turrets and a current probe to measure +12V wire current.

2. Turn on the +12V supply. Disconnect ON1 and GND turrets to provide an ON1 pin signal, and verify that the output voltage rises in less than 1ms.

3. Keeping the scope probes and current probe in the same place, initiate the +12V channel operation with no load, gradually increasing the load current with an electronic or resistive load and verify that the circuit breaker is in the range of 1.35A to 1.68A and timer period 6.1ms to 15.3ms. Disable the +12V channel by connection of the ON1 and GND turrets.

4. With the +12V channel disabled, short the output to GND with an external wire. Monitor the current in the shorting wire with a current probe. Place the scope probes on the V_{CC1} and FTMR1 turrets. Enable the channel with an ON1 pin signal and verify that current is limited in the range of 2.1A to 3.2A and current limit mode takes 0.6ms to 1.6ms.

QUICK START PROCEDURE

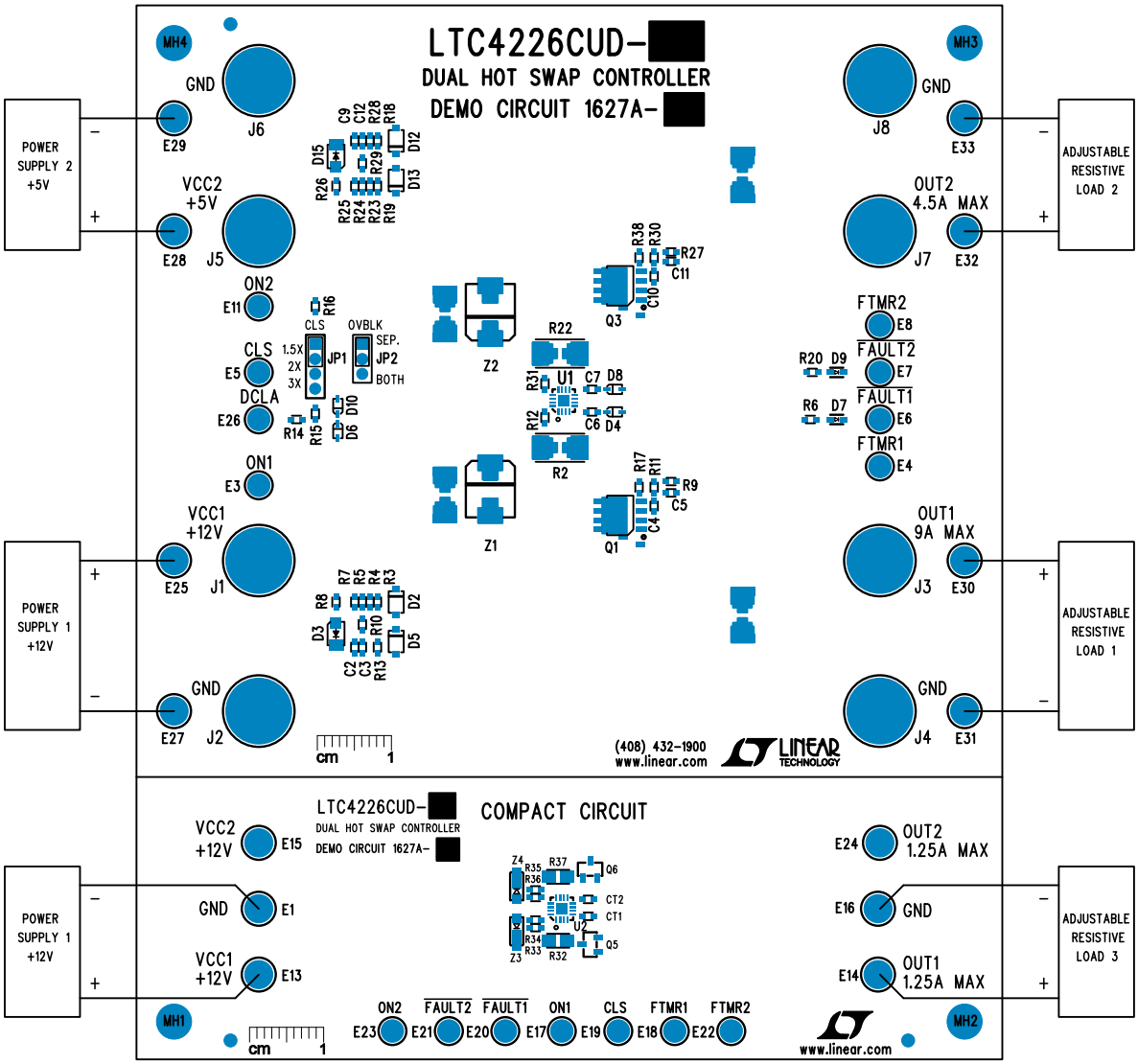
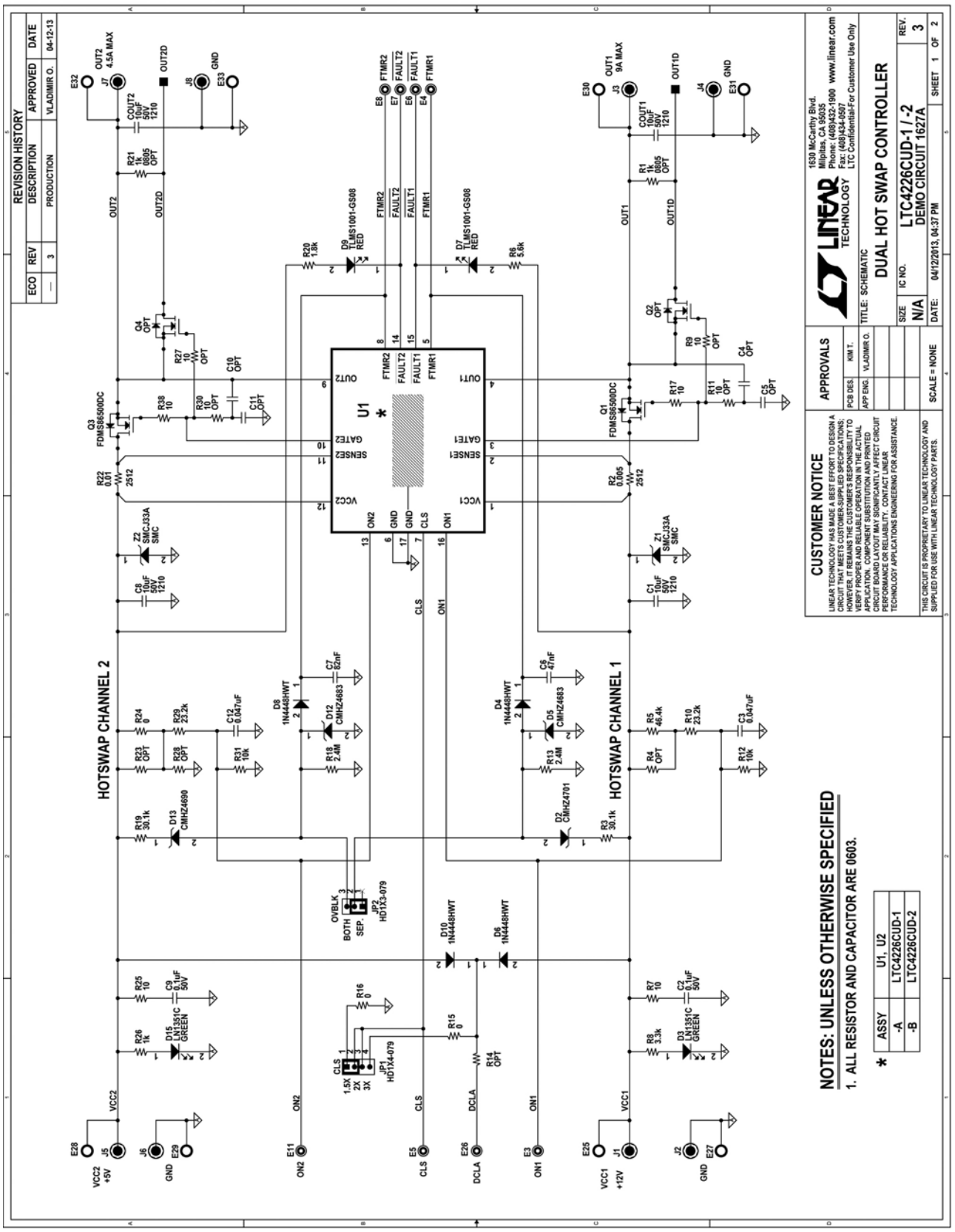


Figure 1. DC1627A Measurement Equipment Setup

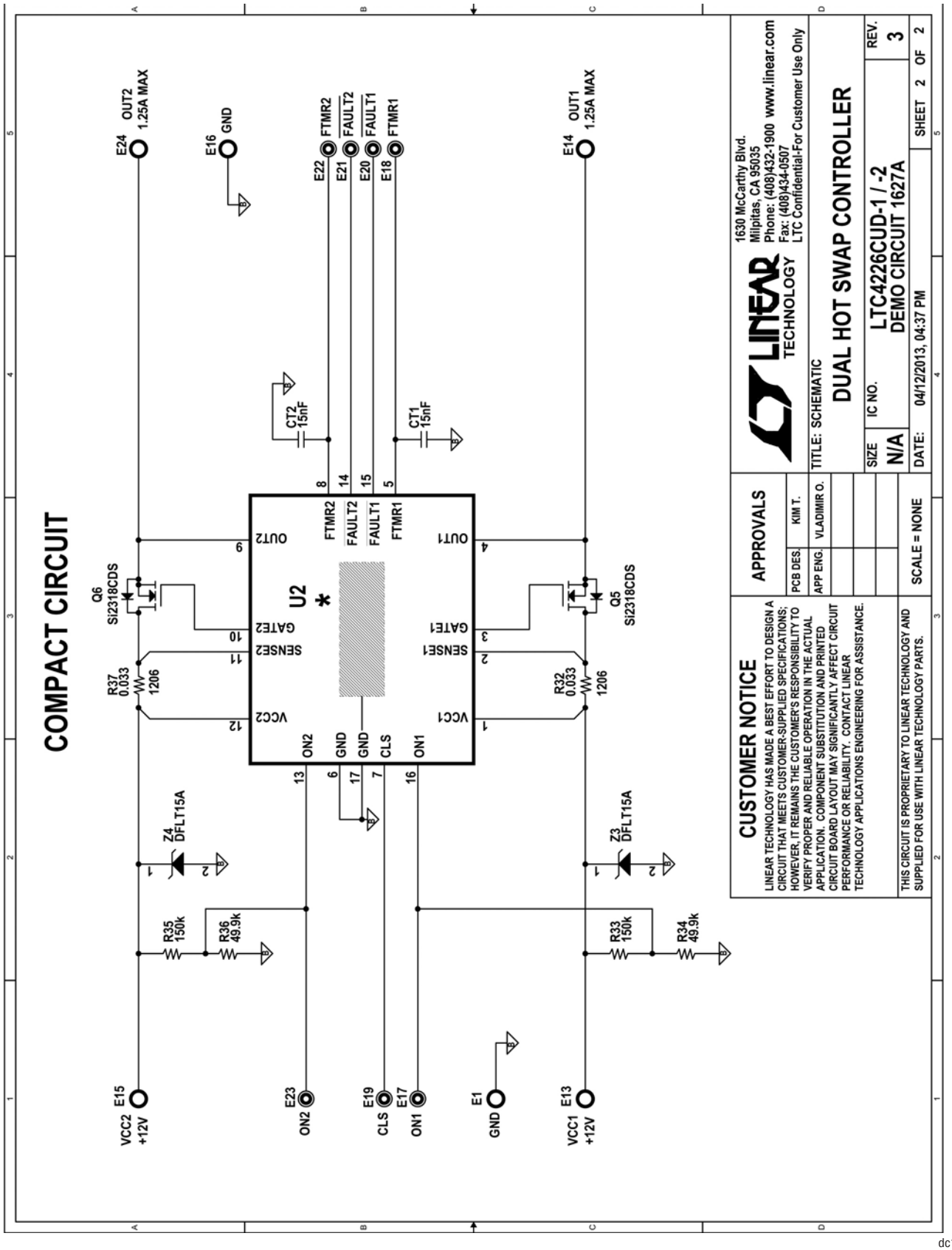
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	4	COUT1, C1, COUT2, C8	CAP., X7R, 10µF 50V, 10%, 1210	MURATA, GRM32ER71H106KA12L
2	2	CT1, CT2	CAP., X7R, 15nF, 50V 10%, 0603	AVX, 06035C153KAT2A
3	2	C2, C9	CAP., X7R, 0.1µF 10% 10V, 0603	AVX, 0603ZC104KAT
4	2	C3, C12	CAP., X7R, 0.047µF 10% 10V, 0603	AVX, 0603ZC473KAT2A
5	0	C4, C5, C10, C11	CAP., 0603	OPT
6	1	C6	CAP., X7R, 47nF, 50V 5%, 0603	AVX, 06035C473JAT2A
7	1	C7	CAP., X7R, 82nF, 50V 10%, 0603	AVX, 06035C823KAT2A
8	1	D2	DIODE ZENER, 1.8V 500mW, 5%, SOD123	CENTRAL SEMI., CMHZ4701
9	2	D3, D15	LED, GREEN	PANASONIC, LN1351C-(TR)
10	4	D4, D6, D8, D10	DIODE, FAST SWITCHING, SOD523	DIODES INC., 1N4448HWT
11	2	D5, D12	DIODE ZENER, 1.8V 500mW, 5%, SOD123	CENTRAL SEMI., CMHZ4683
12	2	D7, D9	LED, RED, 0603	VISHAY, TLMS1001-GS08
13	1	D13	DIODE ZENER, 1.8V 500mW, 5%, SOD123	CENTRAL SEMI., CMHZ4690
14	15	E3-E8, E11, E17-E23, E26	TP, TURRET, 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
15	14	E1, E13-E16, E24, E25, E27-E33	TP, TURRET, 0.094"	MILL-MAX, 2501-2-00-80-00-00-07-0
16	1	JP1	JMP, 4-PIN, 2mm	SAMTEC, TMM-104-02-L-S
17	1	JP2	JMP, 3-PIN, 2mm	SAMTEC, TMM-103-02-L-S
18	8	J1, J2, J3, J4, J5, J6, J7, J8	JACK, BANANA	KEYSTONE, 575-4
19	2	Q1, Q3	MOSFET, N-CH, POWER56	FAICHILD SEMI., FDMS86500DC
20	0	Q2, Q4	MOSFET, N-CH, SO8-POWERPAK	OPT
21	2	Q5, Q6	MOSFET, N-CH, 40V(D-S), SOT23	VISHAY, Si2318CDS
22	0	R1, R21	RES, 1k, 0805	OPT
23	1	R2	RES, 0.005Ω, 1% 1/4W, 1206	VISHAY, WSL12065L000FEA
24	2	R3, R19	RES, 30.1k, 5% 1/10W, 0603	VISHAY, CRCW060330K1JKEA
25	0	R4, R14, R23, R28	RES, 0603	OPT
26	1	R5	RES, 46.4k, 1% 1/10W, 0603	VISHAY, CRCW060346K4FKEA
27	1	R6	RES, 5.6k, 5% 1/10W, 0603	VISHAY, CRCW06035K60JKEA
28	4	R7, R17, R25, R38	RES, 10Ω, 5% 1/10W, 0603	VISHAY, CRCW060310R0JNEA
29	1	R8	RES, 3.3k, 5% 1/10W, 0603	VISHAY, CRCW06033K30JKEA
30	0	R9, R11, R27, R30	RES, 10Ω, 0603	OPT
31	2	R10, R29	RES, 23.2k, 1% 1/10W, 0603	VISHAY, CRCW060323K2FKEA
32	2	R12, R31	RES, 10k, 5% 1/10W, 0603	VISHAY, CRCW060310K0JNEA
33	2	R13, R18	RES, 2.4M, 5% 1/10W, 0603	PANASONIC, ERJ-3GEYJ245V
34	3	R15, R16, R24	RES., CHIP, 0Ω, 0603	VISHAY, CRCW06030000Z0EA
35	1	R20	RES, 1.8k, 5% 1/10W, 0603	VISHAY, CRCW06031K80JKEA
36	1	R22	RES, 0.01Ω, 1% 1/4W, 1206	VISHAY, WSL1206R0100FEA
37	1	R26	RES, 1k, 5% 1/10W, 0603	VISHAY, CRCW06031K00JNEA
38	2	R32, R37	RES, 0.033Ω, 1% 1/4W, 1206	VISHAY, WSL1206R0330FEA
39	2	R33, R35	RES,150k, 5% 1/10W, 0603	VISHAY, CRCW0603150KJKEA
40	2	R34, R36	RES, 49.9k, 5% 1/10W, 0603	VISHAY, CRCW060349K9JKEA
41	2	Z1, Z2	DIODE, SMC-DIODE	DIODES INC., SMCJ33CA-13-F
42	2	Z3, Z4	DIODE, TRANSIENT VOLTAGE SUPPRESSOR, POWEREDi123	DIODES INC., DFLT15A
43	2	SHUNTS ON JP1&JP2	SHUNT, 2mm	SAMTEC, 2SN-BK-G
44	2	U1, U2	IC LTC4226CUD-1, DC1627A-A	LINEAR TECHNOLOGY CORP
45	2	U1, U2	IC LTC4226CUD-2, DC1627A-B	LINEAR TECHNOLOGY CORP

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



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