

# 4G bits DDR2 Mobile RAM™ PoP (14mm × 14mm, 240-ball FBGA)

## EDB4064B3PD

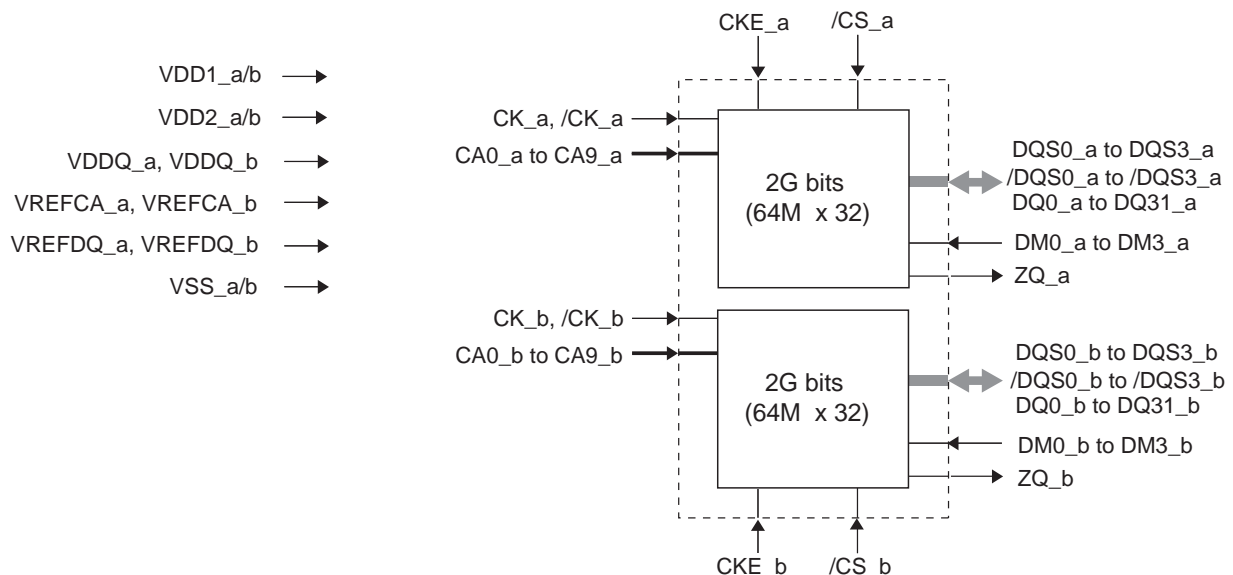
### Specifications

- Density: 4G bits
- Organization
  - 2 pieces of 2Gb (8M words × 32 bits × 8 banks) in one package
  - Independent 2-channel bus
- Data rate: 1066Mbps (max.)
- Package: 240-ball FBGA
  - Package size: 14.0mm × 14.0mm
  - Ball pitch: 0.5mm
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply
  - VDD1 = 1.70V to 1.95V
  - VDD2, VDDQ = 1.14V to 1.30V
- Interface: HSUL\_12
- Operating case temperature range
  - TC = -30°C to +85°C

### Features

- DLL is not implemented
- Low power consumption
- Mobile RAM functions
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
  - Deep power-down mode
  - Per Bank Refresh
- This FBGA is suitable for Package on Package (PoP)

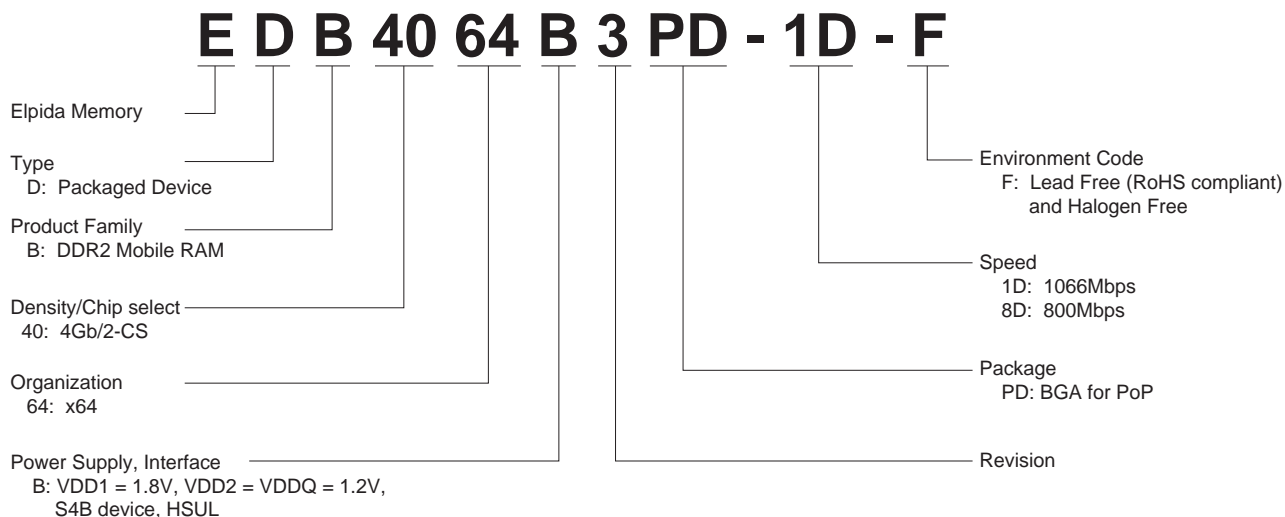
### Block Diagram



### Ordering Information

| Part number      | Organization<br>(words x bits) | Clock frequency | Data rate | Read latency | Package       |
|------------------|--------------------------------|-----------------|-----------|--------------|---------------|
| EDB4064B3PD-1D-F | 64M x 64                       | 533MHz          | 1066Mbps  | 8            | 240-ball FBGA |
| EDB4064B3PD-8D-F | (64M x 32 x 2pcs)              | 400MHz          | 800Mbps   | 6            |               |

### Part Number



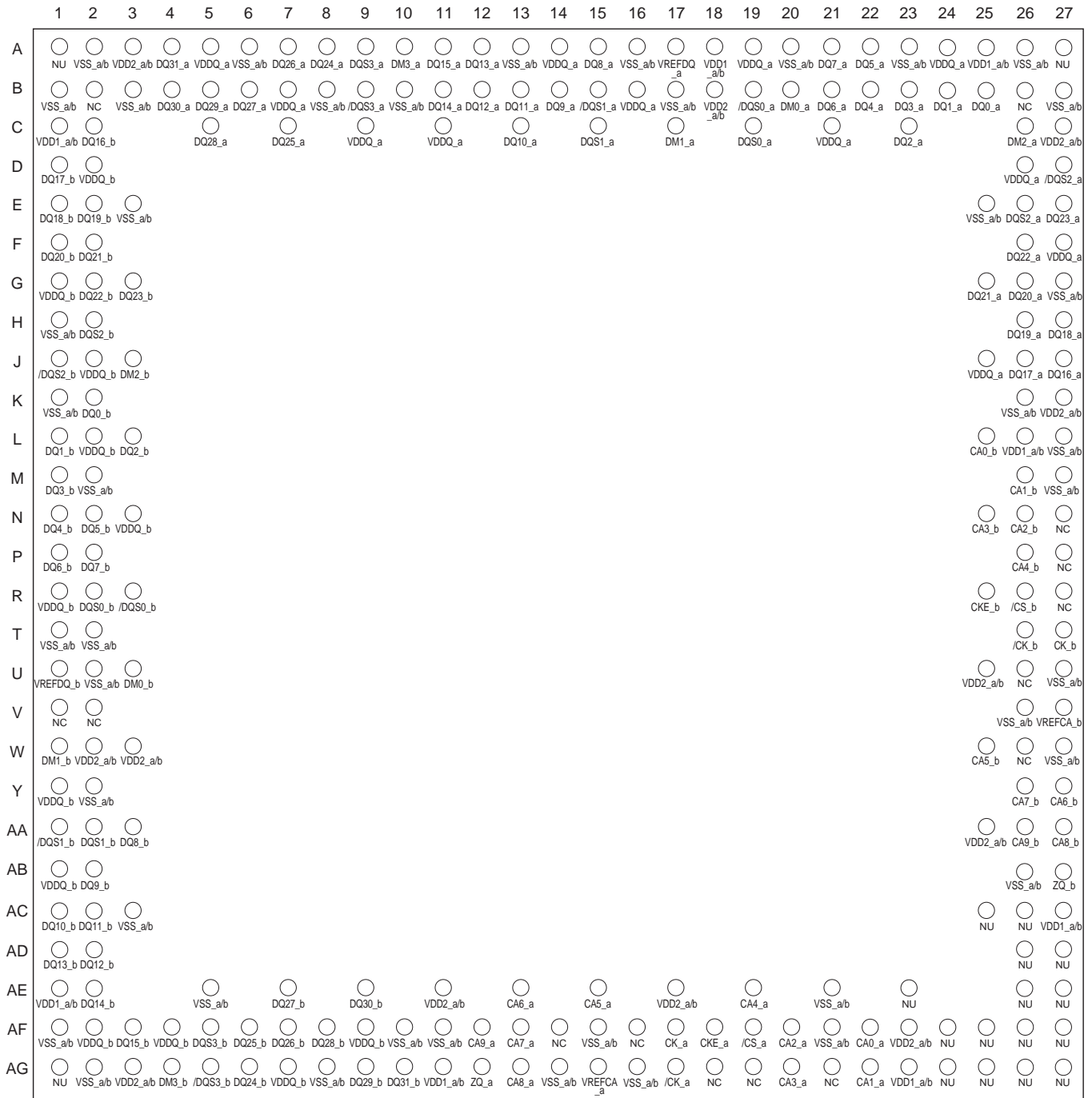
**CONTENTS**

|   |    |
|---|----|
| Specifications .....                          | 1  |
| Block Diagram .....                           | 1  |
| Features .....                                | 1  |
| Ordering Information .....                    | 2  |
| Part Number .....                             | 2  |
| Pin Configurations .....                      | 4  |
| Pin Descriptions .....                        | 5  |
| Pin Capacitance .....                         | 6  |
| Package Drawing .....                         | 7  |
| Mode Register Specification .....             | 8  |
| 1. Electrical Conditions .....                | 9  |
| 1.1 Absolute Maximum Ratings .....            | 9  |
| 1.2 Recommended DC Operating Conditions ..... | 9  |
| 2. Electrical Specifications .....            | 10 |
| 2.1 DC Characteristics 1 .....                | 10 |
| 2.2 DC Characteristics 2 .....                | 12 |
| 2.3 AC Characteristics .....                  | 13 |

Pin Configurations

/xxx indicate active low signal.

240-ball FBGA



(Top view)

## Pin Descriptions

### [DDR2 Mobile RAM\_a]

| Pin name                             | Function   |
|--------------------------------------|--|
| CK_a, /CK_a                          | Clock  |
| CKE_a                                | Clock enable   |
| /CS_a                                | Chip select  |
| CA0_a to CA9_a                       | DDR command/address inputs<br>(Address configurations: Row:R0-R13,<br>Column:C0-C8,<br>Bank:BA0-BA2) |
| DM0_a to DM3_a                       | Input data mask  |
| DQ0_a to DQ31_a                      | Data input/output  |
| DQS0_a to DQS3_a, /DQS0_a to /DQS3_a | Data strobe  |
| VDDQ_a                               | I/O power supply   |
| VREFCA_a                             | Reference voltage for CA input receiver  |
| VREFDQ_a                             | Reference voltage for DQ input receiver  |
| ZQ_a                                 | Reference pin for output drive strength calibration  |

### [DDR2 Mobile RAM\_b]

| Pin name                             | Function   |
|--------------------------------------|--|
| CK_b, /CK_b                          | Clock  |
| CKE_b                                | Clock enable   |
| /CS_b                                | Chip select  |
| CA0_b to CA9_b                       | DDR command/address inputs<br>(Address configurations: Row:R0-R13,<br>Column:C0-C8,<br>Bank:BA0-BA2) |
| DM0_b to DM3_b                       | Input data mask  |
| DQ0_b to DQ31_b                      | Data input/output  |
| DQS0_b to DQS3_b, /DQS0_b to /DQS3_b | Data strobe  |
| VDDQ_b                               | I/O power supply   |
| VREFCA_b                             | Reference voltage for CA input receiver  |
| VREFDQ_b                             | Reference voltage for DQ input receiver  |
| ZQ_b                                 | Reference pin for output drive strength calibration  |

### [Common]

| Pin name         | Function   |
|------------------|--|
| VDD1_a/b         | Core Power Supply 1 for a and b channels                                 |
| VDD2_a/b         | Core Power Supply 2 for a and b channels and input receiver power supply |
| VSS_a/b          | Ground for a and b channels  |
| NC <sup>*1</sup> | No connection  |
| NU <sup>*2</sup> | Not usable   |

- Notes: 1. Not internally connected.  
2. Don't connect. Internally connected.

## Pin Capacitance

| Parameter                     | Symbol | Pins   | min. | max. | Unit | Note    |
|-------------------------------|--------|--|------|------|------|---------|
| Input capacitance             | CI1    | CK_a, /CK_a, CK_b, /CK_b                             | 1.5  | 3.0  | pF   | 1, 2    |
|                               | CI2    | All other DDR2 Mobile RAM input only pins            | 1.5  | 3.5  | pF   | 1, 2    |
| Data input/output capacitance | CI/O   | DQ_a, DQ_b, DM_a, DM_b, DQS_a, /DQS_a, DQS_b, /DQS_b | 2.0  | 4.5  | pF   | 1, 2, 3 |
|                               | CZQ    | ZQ_a, ZQ_b   | 1.5  | 3.0  | pF   | 1, 2, 3 |

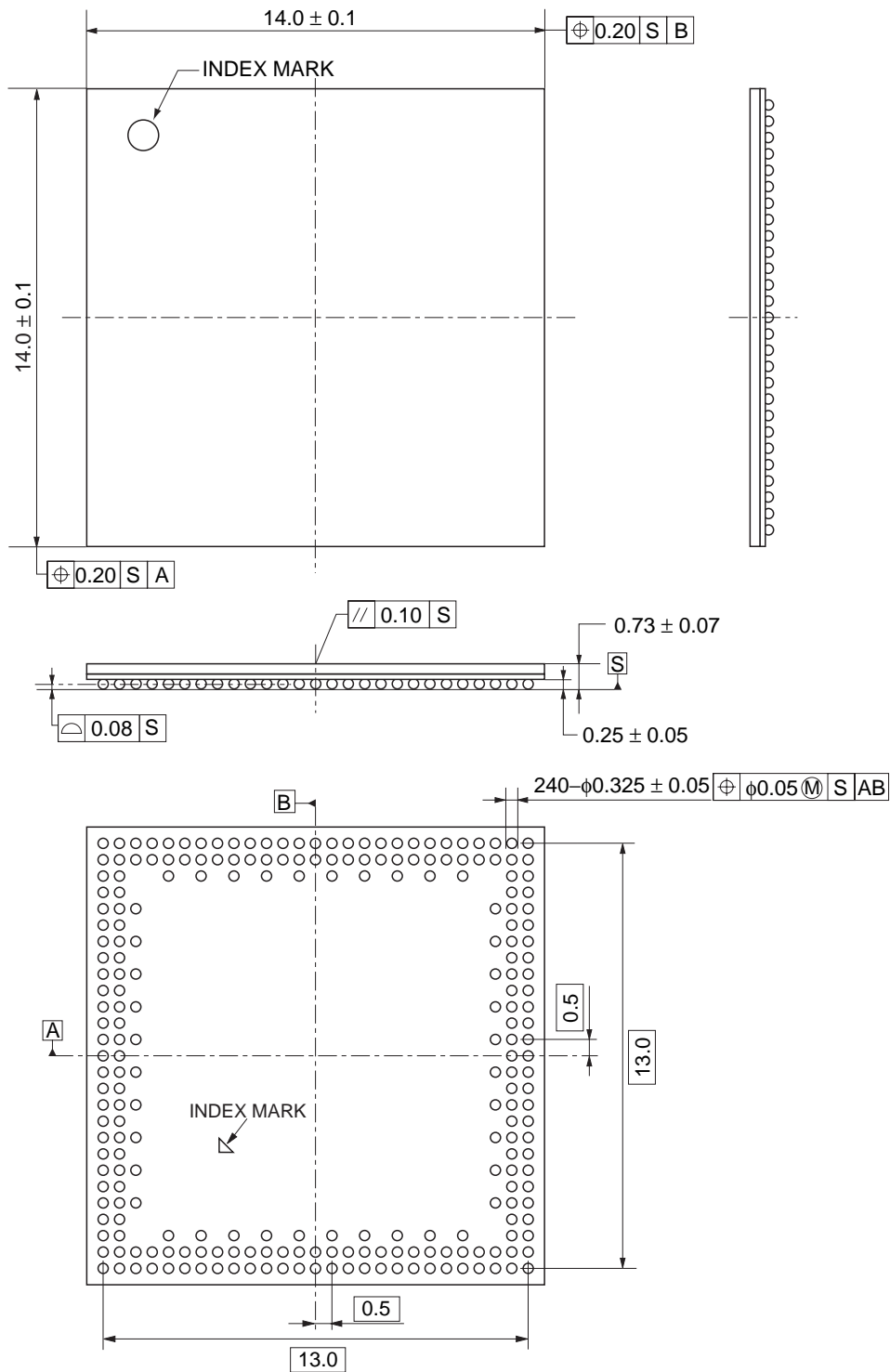
- Notes: 1. This parameter is not subject to production test. It is verified by design and characterization.  
 2. These parameters are measured on  $f = 100\text{MHz}$ ,  $V_{\text{OUT}} = V_{\text{DDQ}}/2$ ,  $T_{\text{A}} = +25^{\circ}\text{C}$ .  
 3. DOUT circuits are disabled.

Package Drawing

240-ball FBGA

Solder ball: Lead free

Unit: mm



ECA-TS2-0438-01

## Mode Register Specification

The following table shows the specifications of mode register values (MR5, 6, 7, 8) for the manufacturer ID and the device descriptions such as DRAM type, density, I/O and die revision.

| MR# | MA <7:0> | OP7                       | OP6 | OP5                    | OP4 | OP3 | OP2 | OP1       | OP0 |
|-----|----------|---------------------------|-----|------------------------|-----|-----|-----|-----------|-----|
| 5   | 05h      | 0                         | 0   | 0                      | 0   | 0   | 0   | 1         | 1   |
|     |          | Manufacturer ID : ELPIDA  |     |                        |     |     |     |           |     |
| 6   | 06h      | 0                         | 0   | 0                      | 0   | 0   | 0   | 1         | 0   |
|     |          | Die Revision : Revision C |     |                        |     |     |     |           |     |
| 7   | 07h      | 0                         | 0   | 0                      | 0   | 0   | 0   | 0         | 0   |
|     |          | RFU : Default value       |     |                        |     |     |     |           |     |
| 8   | 08h      | 0                         | 0   | 0                      | 1   | 0   | 1   | 0         | 0   |
|     |          | I/O : ×32                 |     | Density of Die : 2Gbit |     |     |     | Type : S4 |     |

Note: 1. The register values specify monolithic die information in a package.  
Therefore, please refer to the block diagram for understanding whole memory configuration of the product containing multiple dice in a package.



## 1. Electrical Conditions

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.
- Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR2 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

### 1.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings**

| Parameter                            | Symbol    | min. | max. | Unit | Note |
|--------------------------------------|-----------|------|------|------|------|
| VDD1 supply voltage relative to VSS  | VDD1      | -0.4 | 2.3  | V    | 2    |
| VDD2 supply voltage relative to VSS  | VDD2      | -0.4 | 1.6  | V    | 2    |
| VDDQ supply voltage relative to VSSQ | VDDQ      | -0.4 | 1.6  | V    | 2, 3 |
| Voltage on any ball relative to VSS  | VIN, VOUT | -0.4 | 1.6  | V    |      |
| Storage Temperature                  | TSTG      | -55  | 125  | °C   |      |

- Notes: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See Power-Ramp section "Power-up, initialization and Power-Off" in the individual DDR2 Mobile RAM data sheet for relationship between power supplies.
3.  $V_{REF} \leq 0.6 \times V_{DDQ}$ ; however,  $V_{REF}$  may be  $\geq V_{DDQ}$  provided that  $V_{REF} \leq 300\text{mV}$ .
4. Storage Temperature is the case surface temperature on the center/top side of the DDR2 Mobile RAM Device. For the measurement conditions, please refer to JE5D51-2 standard.

### Caution

**Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.**

### 1.2 Recommended DC Operating Conditions

**Table 2 Recommended DC Operating Conditions(TC = -30°C to +85°C)**

| Parameter                       | Symbol | min. | typ. | max. | Unit |
|---------------------------------|--------|------|------|------|------|
| Core Power1                     | VDD1   | 1.70 | 1.80 | 1.95 | V    |
| Core Power2, Input Buffer Power | VDD2   | 1.14 | 1.20 | 1.30 | V    |
| I/O Buffer Power                | VDDQ   | 1.14 | 1.20 | 1.30 | V    |

## 2. Electrical Specifications

### 2.1 DC Characteristics 1

(TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

**Table 3 IDD Specification Parameters and Operating Conditions**

| Symbol    | Power Supply | 1066 | 800  | Unit | Parameter/Condition  |
|-----------|--------------|------|------|------|--|
|           |              | max. | max. |      |  |
| IDD0_1    | VDD1         | 14   | 14   | mA   | <b>All devices in operating one bank active-precharge</b><br>tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH;<br>/CS is HIGH between valid commands;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE      |
| IDD0_2    | VDD2         | 80   | 76   | mA   |  |
| IDD0_IN   | VDDQ         | 2.0  | 2.0  | mA   |  |
| IDD2P_1   | VDD1         | 0.6  | 0.6  | mA   | <b>All devices in idle power-down standby current</b><br>tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; All banks idle;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE                                   |
| IDD2P_2   | VDD2         | 1.6  | 1.6  | mA   |  |
| IDD2P_IN  | VDDQ         | 0.2  | 0.2  | mA   |  |
| IDD2PS_1  | VDD1         | 0.6  | 0.6  | mA   | <b>All devices in idle power-down standby current with clock stop</b><br>CK=LOW, /CK=HIGH; CKE is LOW; /CS is HIGH; All banks idle;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE                       |
| IDD2PS_2  | VDD2         | 1.6  | 1.6  | mA   |  |
| IDD2PS_IN | VDDQ         | 0.2  | 0.2  | mA   |  |
| IDD2N_1   | VDD1         | 1.2  | 1.2  | mA   | <b>All devices in idle non power-down standby current</b><br>tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; All banks idle;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE                              |
| IDD2N_2   | VDD2         | 28   | 24   | mA   |  |
| IDD2N_IN  | VDDQ         | 2.0  | 2.0  | mA   |  |
| IDD2NS_1  | VDD1         | 1.2  | 1.2  | mA   | <b>All devices in idle non power-down standby current with clock stop</b><br>CK=LOW, /CK=HIGH; CKE is HIGH; /CS is HIGH; All banks idle;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE                  |
| IDD2NS_2  | VDD2         | 14   | 14   | mA   |  |
| IDD2NS_IN | VDDQ         | 2.0  | 2.0  | mA   |  |
| IDD3P_1   | VDD1         | 1.4  | 1.4  | mA   | <b>All devices in active power-down standby current</b><br>tCK = tCK(avg)min; CKE is LOW; /CS is HIGH; One bank active;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE                                |
| IDD3P_2   | VDD2         | 8.0  | 8.0  | mA   |  |
| IDD3P_IN  | VDDQ         | 0.2  | 0.2  | mA   |  |
| IDD3PS_1  | VDD1         | 1.4  | 1.4  | mA   | <b>All devices in active power-down standby current with clock stop</b><br>CK=LOW, /CK=HIGH; CKE is LOW; /CS is HIGH; One bank active;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE                    |
| IDD3PS_2  | VDD2         | 8.0  | 8.0  | mA   |  |
| IDD3PS_IN | VDDQ         | 0.2  | 0.2  | mA   |  |
| IDD3N_1   | VDD1         | 3.0  | 3.0  | mA   | <b>All devices in active non power-down standby current</b><br>tCK = tCK(avg)min; CKE is HIGH; /CS is HIGH; One bank active;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE                           |
| IDD3N_2   | VDD2         | 34   | 30   | mA   |  |
| IDD3N_IN  | VDDQ         | 2.0  | 2.0  | mA   |  |
| IDD3NS_1  | VDD1         | 3.0  | 3.0  | mA   | <b>All devices in active non power-down standby current with clock stop</b><br>CK=LOW, /CK=HIGH; CKE is HIGH; /CS is HIGH; One bank active;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE               |
| IDD3NS_2  | VDD2         | 20   | 20   | mA   |  |
| IDD3NS_IN | VDDQ         | 2.0  | 2.0  | mA   |  |
| IDD4R_1   | VDD1         | 4.0  | 4.0  | mA   | <b>All devices in operating burst read</b><br>tCK = tCK(avg)min; /CS is HIGH between valid commands;<br>One bank active; BL = 4; RL = RLmin;<br>CA bus inputs are SWITCHING;<br>50% data change each burst transfer; |
| IDD4R_2   | VDD2         | 320  | 250  | mA   |  |

Table 3 IDD Specification Parameters and Operating Conditions (cont'd)

| Symbol    | Power Supply | 1066 | 800  | Unit | Parameter/Condition   |
|-----------|--------------|------|------|------|---|
|           |              | max. | max. |      |   |
| IDD4W_1   | VDD1         | 4.0  | 4.0  | mA   | <b>All devices in operating burst write</b><br>tCK = tCK(avg)min; /CS is HIGH between valid commands;<br>One bank active; BL = 4; WL = WLmin;<br>CA bus inputs are SWITCHING;<br>50% data change each burst transfer; |
| IDD4W_2   | VDD2         | 360  | 280  | mA   |   |
| IDD4W_IN  | VDDQ         | 2.0  | 2.0  | mA   |   |
| IDD5_1    | VDD1         | 46   | 46   | mA   | <b>All devices in all bank auto-refresh</b><br>tCK = tCK(avg)min; CKE is HIGH between valid commands;<br>tRC = tRFCabmin; Burst refresh;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE;               |
| IDD5_2    | VDD2         | 164  | 160  | mA   |   |
| IDD5_IN   | VDDQ         | 2.0  | 2.0  | mA   |   |
| IDD5AB_1  | VDD1         | 4.0  | 4.0  | mA   | <b>All devices in all bank auto-refresh</b><br>tCK = tCK(avg)min; CKE is HIGH between valid commands; tRC = tREFI;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE;                                     |
| IDD5AB_2  | VDD2         | 30   | 24   | mA   |   |
| IDD5AB_IN | VDDQ         | 2.0  | 2.0  | mA   |   |
| IDD5PB_1  | VDD1         | 4.0  | 4.0  | mA   | <b>All devices in per bank auto-refresh</b><br>tCK = tCK(avg)min; CKE is HIGH between valid commands;<br>tRC = tREFI/8;<br>CA bus inputs are SWITCHING;<br>Data bus inputs are STABLE;                                |
| IDD5PB_2  | VDD2         | 30   | 24   | mA   |   |
| IDD5PB_IN | VDDQ         | 2.0  | 2.0  | mA   |   |
| IDD8_1    | VDD1         | 20   | 20   | μA   | <b>All devices in deep power-down</b><br>CK = LOW, /CK = HIGH; CKE is LOW;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE;  |
| IDD8_2    | VDD2         | 20   | 20   | μA   |   |
| IDD8_IN   | VDDQ         | 20   | 20   | μA   |   |

Notes: 1. IDD values published are the maximum of the distribution of the arithmetic mean.

2. IDD current specifications are tested after the device is properly initialized.

**Table 4 IDD6 Full and Partial Array Self-Refresh Current**

| Parameter                     |            | Symbol  | Value | Unit | Condition  |
|-------------------------------|------------|---------|-------|------|--|
| Self-Refresh Current<br>+45°C | Full Array | IDD6_1  | 420   | μA   | <b>All devices in self-refresh</b><br>CK = LOW, /CK = HIGH;<br>CKE is LOW;<br>CA bus inputs are STABLE;<br>Data bus inputs are STABLE; |
|                               |            | IDD6_2  | 1200  | μA   |  |
|                               |            | IDD6_IN | 20    | μA   |  |
|                               | 1/2 Array  | IDD6_1  | 260   | μA   |  |
|                               |            | IDD6_2  | 780   | μA   |  |
|                               |            | IDD6_IN | 20    | μA   |  |
|                               | 1/4 Array  | IDD6_1  | 200   | μA   |  |
|                               |            | IDD6_2  | 540   | μA   |  |
|                               |            | IDD6_IN | 20    | μA   |  |
|                               | 1/8 Array  | IDD6_1  | 170   | μA   |  |
|                               |            | IDD6_2  | 420   | μA   |  |
|                               |            | IDD6_IN | 20    | μA   |  |
| Self-Refresh Current<br>+85°C | Full Array | IDD6_1  | 1100  | μA   |  |
|                               |            | IDD6_2  | 3400  | μA   |  |
|                               |            | IDD6_IN | 200   | μA   |  |
|                               | 1/2 Array  | IDD6_1  | 800   | μA   |  |
|                               |            | IDD6_2  | 2400  | μA   |  |
|                               |            | IDD6_IN | 200   | μA   |  |
|                               | 1/4 Array  | IDD6_1  | 700   | μA   |  |
|                               |            | IDD6_2  | 1800  | μA   |  |
|                               |            | IDD6_IN | 200   | μA   |  |
|                               | 1/8 Array  | IDD6_1  | 640   | μA   |  |
|                               |            | IDD6_2  | 1500  | μA   |  |
|                               |            | IDD6_IN | 200   | μA   |  |

Note: 1. IDD6 85°C is the maximum and IDD6 45°C is typical of the distribution of the arithmetic mean.

## 2.2 DC Characteristics 2

(TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

**Table 5 Electrical Characteristics and Operating Conditions**

| Symbol | min. | max. | Unit | Parameter/Condition   | Note |
|--------|------|------|------|---|------|
| IL     | -2   | +2   | μA   | <b>Input leakage current:</b><br>For CA, CKE, /CS, CK, /CK<br>Any input $0V \leq V_{IN} \leq V_{DD2}$<br>(All other pins not under test = 0V) | 2    |
| IVREF  | -1   | +1   | μA   | <b>VREF supply leakage current:</b><br>VREFDQ = VDDQ/2 or VREFCA = VDD2/2<br>(All other pins not under test = 0V)                             | 1    |

Notes: 1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.

2. Although DM is for input only, the DM leakage shall match the DQ and DQS, /DQS output leakage specification.

## 2.3 AC Characteristics

(TC = -30°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 6 AC Characteristics Table \*6

| Parameter   | Symbol                 | min.<br>max. | min.<br>tCK*9 | 1066   | 800  | Unit     |
|---|------------------------|--------------|---------------|--|------|----------|
| Max. Frequency*4  |                        |              | —             | 533  | 400  | MHz      |
| Clock Timing  |                        |              |               |  |      |          |
| Average Clock Period  | tCK(avg)               | min.         | —             | 1.875  | 2.5  | ns       |
|   |                        | max.         | —             | 100  |      | ns       |
| Average high pulse width  | tCH(avg)               | min.         | —             | 0.45   |      | tCK(avg) |
|   |                        | max.         | —             | 0.55   |      |          |
| Average low pulse width   | tCL(avg)               | min.         | —             | 0.45   |      | tCK(avg) |
|   |                        | max.         | —             | 0.55   |      |          |
| Absolute Clock Period   | tCK(abs)               | min.         | —             | tCK(avg)(min.) + tJIT(per)(min.)   |      | ps       |
| Absolute clock HIGH pulse width (with allowed jitter)                           | tCH(abs),<br>allowed   | min.         | —             | 0.43   |      | tCK(avg) |
|   |                        | max.         | —             | 0.57   |      |          |
| Absolute clock LOW pulse width (with allowed jitter)                            | tCL(abs),<br>allowed   | min.         | —             | 0.43   |      | tCK(avg) |
|   |                        | max.         | —             | 0.57   |      |          |
| Clock Period Jitter (with allowed jitter)                                       | tJIT(per),<br>allowed  | min.         | —             | -90  | -100 | ps       |
|   |                        | max.         | —             | 90   | 100  |          |
| Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter) | tJIT(cc),<br>allowed   | max.         | —             | 180  | 200  | ps       |
| Duty cycle Jitter (with allowed jitter)   | tJIT(duty),<br>allowed | min.         | —             | min((tCH(abs),min - tCH(avg),min), (tCL(abs),min - tCL(avg),min)) × tCK(avg) |      | ps       |
|   |                        | max.         | —             | max((tCH(abs),max - tCH(avg),max), (tCL(abs),max - tCL(avg),max)) × tCK(avg) |      |          |
| Cumulative error across 2 cycles  | tERR(2per),<br>allowed | min.         | —             | -132   | -147 | ps       |
|   |                        | max.         | —             | 132  | 147  |          |
| Cumulative error across 3 cycles  | tERR(3per),<br>allowed | min.         | —             | -157   | -175 | ps       |
|   |                        | max.         | —             | 157  | 175  |          |
| Cumulative error across 4 cycles  | tERR(4per),<br>allowed | min.         | —             | -175   | -194 | ps       |
|   |                        | max.         | —             | 175  | 194  |          |
| Cumulative error across 5 cycles  | tERR(5per),<br>allowed | min.         | —             | -188   | -209 | ps       |
|   |                        | max.         | —             | 188  | 209  |          |
| Cumulative error across 6 cycles  | tERR(6per),<br>allowed | min.         | —             | -200   | -222 | ps       |
|   |                        | max.         | —             | 200  | 222  |          |
| Cumulative error across 7 cycles  | tERR(7per),<br>allowed | min.         | —             | -209   | -232 | ps       |
|   |                        | max.         | —             | 209  | 232  |          |

Table 6 AC Characteristics Table\*6 (cont'd)

| Parameter  | Symbol                  | min.<br>max. | min.<br>tCK*9 | 1066   | 800  | Unit     |
|--|-------------------------|--------------|---------------|--|------|----------|
| Cumulative error across 8 cycles                       | tERR(8per),<br>allowed  | min.         | —             | -217   | -241 | ps       |
|  |                         | max.         | —             | 217  | 241  |          |
| Cumulative error across 9 cycles                       | tERR(9per),<br>allowed  | min.         | —             | -224   | -249 | ps       |
|  |                         | max.         | —             | 224  | 249  |          |
| Cumulative error across 10 cycles                      | tERR(10per),<br>allowed | min.         | —             | -231   | -257 | ps       |
|  |                         | max.         | —             | 231  | 257  |          |
| Cumulative error across 11 cycles                      | tERR(11per),<br>allowed | min.         | —             | -237   | -263 | ps       |
|  |                         | max.         | —             | 237  | 263  |          |
| Cumulative error across 12 cycles                      | tERR(12per),<br>allowed | min.         | —             | -242   | -269 | ps       |
|  |                         | max.         | —             | 242  | 269  |          |
| Cumulative error across n = 13, 14 . . . 49, 50 cycles | tERR(nper),<br>allowed  | min.         | —             | tERR(nper),allowed,min. =<br>(1 + 0.68ln(n)) ×<br>tJIT(per),allowed,min. |      | ps       |
|  |                         | max.         | —             | tERR(nper),allowed,max. =<br>(1 + 0.68ln(n)) ×<br>tJIT(per),allowed,max. |      |          |
| Read Parameters  |                         |              |               |  |      |          |
| DQS output access time from CK, /CK                    | tDQSCK                  | min.         | —             | 2500   |      | ps       |
|  |                         | max.         | —             | 5500   |      |          |
| DQSCK Delta Short*15                                   | tDQSCKDS                | max.         | —             | 330  | 450  | ps       |
| DQSCK Delta Medium*16                                  | tDQSCKDM                | max.         | —             | 680  | 900  | ps       |
| DQSCK Delta Long*17                                    | tDQSCKDL                | max.         | —             | 920  | 1200 | ps       |
| DQS – DQ skew  | tDQSQ                   | max.         | —             | 200  | 240  | ps       |
| Data hold skew factor                                  | tQHS                    | max.         | —             | 230  | 280  | ps       |
| DQS Output High Pulse Width                            | tQSH                    | min.         | —             | tCH(abs) - 0.05  |      | tCK(avg) |
| DQS Output Low Pulse Width                             | tQSL                    | min.         | —             | tCL(abs) - 0.05  |      | tCK(avg) |
| Data Half Period                                       | tQHP                    | min.         | —             | min(tQSH, tQSL)  |      | tCK(avg) |
| DQ / DQS output hold time from DQS                     | tQH                     | min.         | —             | tQHP - tQHS  |      | ps       |
| Read preamble*12,*13                                   | tRPRE                   | min.         | —             | 0.9  |      | tCK(avg) |
| Read postamble*12,*14                                  | tRPST                   | min.         | —             | tCL(abs) - 0.05  |      | tCK(avg) |
| DQS low-Z from clock*12                                | tLZ(DQS)                | min.         | —             | tDQSCK(min.) - 300   |      | ps       |
| DQ low-Z from clock*12                                 | tLZ(DQ)                 | min.         | —             | tDQSCK(min.) -<br>(1.4 × tQHS(max.))                                     |      | ps       |
| DQS high-Z from clock*12                               | tHZ(DQS)                | max.         | —             | tDQSCK(max.) - 100   |      | ps       |
| DQ high-Z from clock*12                                | tHZ(DQ)                 | max.         | —             | tDQSCK(max.) +<br>(1.4 × tDQSQ(max.))                                    |      | ps       |

Table 6 AC Characteristics Table\*6 (cont'd)

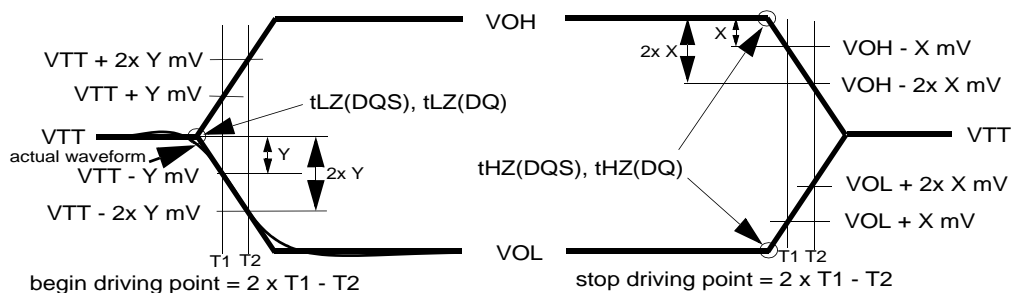
| Parameter   | Symbol   | min. max. | min. tCK*9 | 1066 | 800 | Unit     |
|---|----------|-----------|------------|------|-----|----------|
| Write Parameters*11                               |          |           |            |      |     |          |
| DQ and DM input hold time (VREF based)            | tDH      | min.      | —          | 210  | 270 | ps       |
| DQ and DM input setup time (VREF based)           | tDS      | min.      | —          | 210  | 270 | ps       |
| DQ and DM input pulse width                       | tDIPW    | min.      | —          | 0.35 |     | tCK(avg) |
| Write command to 1st DQS latching transition      | tDQSS    | min.      | —          | 0.75 |     | tCK(avg) |
|   |          | max.      | —          | 1.25 |     |          |
| DQS input high-level width                        | tDQSH    | min.      | —          | 0.4  |     | tCK(avg) |
| DQS input low-level width                         | tDQSL    | min.      | —          | 0.4  |     | tCK(avg) |
| DQS falling edge to CK setup time                 | tDSS     | min.      | —          | 0.2  |     | tCK(avg) |
| DQS falling edge hold time from CK                | tDSH     | min.      | —          | 0.2  |     | tCK(avg) |
| Write postamble                                   | tWPST    | min.      | —          | 0.4  |     | tCK(avg) |
| Write preamble                                    | tWPRE    | min.      | —          | 0.35 |     | tCK(avg) |
| CKE Input Parameters                              |          |           |            |      |     |          |
| CKE min. pulse width (high and low pulse width)   | tCKE     | min.      | 3          | 3    |     | tCK(avg) |
| CKE input setup time                              | tISCKE*2 | min.      | —          | 0.25 |     | tCK(avg) |
| CKE input hold time                               | tIHCKE*3 | min.      | —          | 0.25 |     | tCK(avg) |
| Command Address Input Parameters*11               |          |           |            |      |     |          |
| Address and control input setup time              | tIS*1    | min.      | —          | 220  | 290 | ps       |
| Address and control input hold time               | tIH*1    | min.      | —          | 220  | 290 | ps       |
| Address and control input pulse width             | tIPW     | min.      | —          | 0.40 |     | tCK(avg) |
| Boot Parameters (10 MHz – 55 MHz)*5,*7,*8         |          |           |            |      |     |          |
| Clock Cycle Time                                  | tCKb     | max.      | —          | 100  |     | ns       |
|   |          | min.      | —          | 18   |     |          |
| CKE Input Setup Time                              | tISCKEb  | min.      | —          | 2.5  |     | ns       |
| CKE Input Hold Time                               | tIHCKEb  | min.      | —          | 2.5  |     | ns       |
| Address & Control Input Setup Time                | tISb     | min.      | —          | 1150 |     | ps       |
| Address & Control Input Hold Time                 | tIHb     | min.      | —          | 1150 |     | ps       |
| DQS Output Data Access Time from CK, /CK          | tDQSCKb  | min.      | —          | 2.0  |     | ns       |
|   |          | max.      | —          | 10.0 |     |          |
| Data Strobe Edge to Output Data Edge tDQSQb - 1.2 | tDQSQb   | max.      | —          | 1.2  |     | ns       |
| Data Hold Skew Factor                             | tQHSb    | max.      | —          | 1.2  |     | ns       |
| Mode Register Parameters                          |          |           |            |      |     |          |
| Mode Register Write command period                | tMRW     | min.      | 5          | 5    |     | tCK(avg) |
| Mode Register Read command period                 | tMRR     | min.      | 2          | 2    |     | tCK(avg) |

Table 6 AC Characteristics Table\*<sup>6</sup> (cont'd)

| Parameter   | Symbol   | min. max. | min. tCK* <sup>9</sup> | 1066   | 800 | Unit     |
|---|----------|-----------|------------------------|--|-----|----------|
| DDR2 Mobile RAM Core Parameters* <sup>9</sup>                                     |          |           |                        |  |     |          |
| Read Latency  | RL       | min.      | 3                      | 8  | 6   | tCK(avg) |
| Write Latency   | WL       | min.      | 1                      | 4  | 3   | tCK(avg) |
| ACTIVE to ACTIVE command period   | tRC      | min.      | —                      | tRAS + tRPab<br>(with all-bank Precharge)<br>tRAS + tRPpb<br>(with per-bank Precharge) |     | ns       |
| CKE min. pulse width during Self-Refresh<br>(low pulse width during Self-Refresh) | tCKESR   | min.      | 3                      | 15   |     | ns       |
| Self-refresh exit to next valid command delay                                     | tXSR     | min.      | 2                      | tRFCab + 10  |     | ns       |
| Exit power down to next valid command delay                                       | tXP      | min.      | 2                      | 7.5  |     | ns       |
| CAS to CAS delay  | tCCD     | min.      | 2                      | 2  |     | tCK(avg) |
| Internal Read to Precharge command delay  | tRTP     | min.      | 2                      | 7.5  |     | ns       |
| RAS to CAS Delay  | tRCD     | min.      | 3                      | 18   |     | ns       |
| Row Precharge Time (single bank)  | tRPpb    | min.      | 3                      | 18   |     | ns       |
| Row Precharge Time (all banks)  | tRPab    | min.      | 3                      | 21   |     | ns       |
| Row Active Time   | tRAS     | min.      | 3                      | 42   |     | ns       |
|   |          | max.      | —                      | 70   |     | μs       |
| Write Recovery Time   | tWR      | min.      | 3                      | 15   |     | ns       |
| Internal Write to Read Command Delay  | tWTR     | min.      | 2                      | 7.5  |     | ns       |
| Active bank A to Active bank B  | tRRD     | min.      | 2                      | 10   |     | ns       |
| Four Bank Activate Window   | tFAW     | min.      | 8                      | 50   |     | ns       |
| Minimum Deep Power Down Time  | tDPD     | min.      | —                      | 500  |     | μs       |
| DDR2 Mobile RAM Refresh Requirement Parameters                                    |          |           |                        |  |     |          |
| Refresh Window  | tREFW    | max.      | —                      | 32   |     | ms       |
| Required number of REFRESH commands   | R        | min.      | —                      | 8192   |     |          |
| Average time between REFRESH commands<br>(for reference only)                     | tREFI    | max.      | —                      | 3.9  |     | μs       |
|   | tREFIpb  | max.      | —                      | 0.4875   |     | μs       |
| Refresh Cycle time  | tRFCab   | min.      | —                      | 130  |     | ns       |
| Per Bank Refresh Cycle time   | tRFCpb   | min.      | —                      | 60   |     | ns       |
| Burst Refresh Window<br>= 4 × 8 × tRFCab  | tREFBW   | min.      | —                      | 4.16   |     | μs       |
| ZQ Calibration Parameters* <sup>9</sup>   |          |           |                        |  |     |          |
| Initialization Calibration Time   | tZQINIT  | min.      | —                      | 1  |     | μs       |
| Long Calibration Time   | tZQCL    | min.      | 6                      | 360  |     | ns       |
| Short Calibration Time  | tZQCS    | min.      | 6                      | 90   |     | ns       |
| Calibration Reset Time  | tZQRESET | min.      | 3                      | 50   |     | ns       |



- Notes:
1. Input set-up/hold time for signal(CA0 – CA9, /CS).
  2. CKE input setup time is measured from CKE reaching high/low voltage level to CK, /CK crossing.
  3. CKE input hold time is measured from CK, /CK crossing to CKE reaching high/low voltage level.
  4. Frequency values are for reference only. Clock cycle time (tCK) shall be used to determine device capabilities.
  5. To guarantee device operation before the DDR2 Mobile RAM Device is configured a number of AC boot timing parameters are defined in the [Table 6 on page 13](#). Boot parameter symbols have the letter b appended, e.g. tCK during boot is tCKb.
  6. Frequency values are for reference only. Clock cycle time (tCK or tCKb) shall be used to determine device capabilities.
  7. The DDR2 Mobile RAM will set some Mode register default values upon receiving a RESET (MRW) command as specified in "Mode Register Definition" in the individual DDR2 Mobile RAM data sheet.
  8. The output skew parameters are measured with Ron default settings into the reference load.
  9. These parameters should be satisfied with both specification, analog (ns) value and min. tCK.
  10. All AC timings assume an input slew rate of 1V/ns.
  11. Read, Write, and Input Setup and Hold values are referenced to VREF.
  12. For low-to-high and high-to-low transitions the timing reference will be at the point when the signal crosses VTT. tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ) ), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ) ). [Figure 1](#) shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.



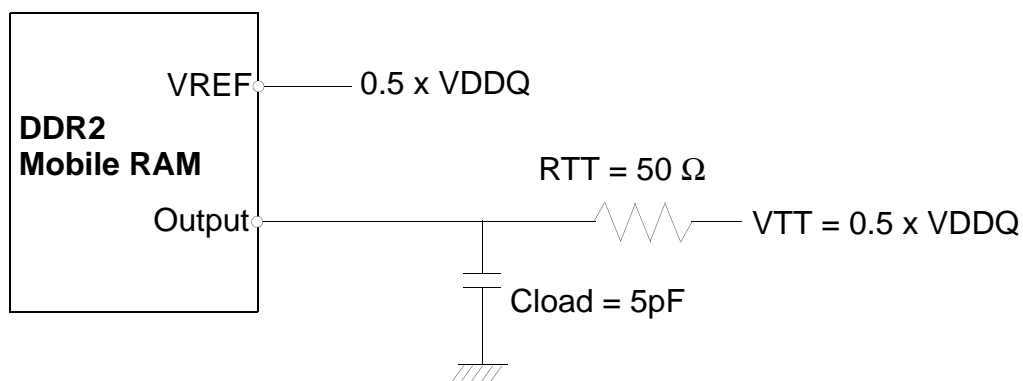
**Figure 1 — tLZ and tHZ Method for Calculating Transition and Endpoints**

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-/DQS.

13. Measured from the start driving of DQS – /DQS to the start driving the first rising strobe edge.
14. Measured from the from start driving the last falling strobe edge to the stop driving DQS – /DQS.
15. tDQCKDS is the absolute value of the difference between any two tDQCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160ns rolling window. tDQCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
16. tDQCKDM is the absolute value of the difference between any two tDQCK measurements (within a byte lane) within a 1.6µs rolling window. tDQCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.
17. tDQCKDL is the absolute value of the difference between any two tDQCK measurements (within a byte lane) within a 32ms rolling window. tDQCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10°C/s. Values do not include clock jitter.

### 2.3.1 HSUL\_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



**Figure 2 — HSUL\_12 Driver Output Reference Load for Timing and Slew Rate**

Note: 1. All output timing parameter values (like  $t_{DQSCK}$ ,  $t_{DQSQ}$ ,  $t_{QHS}$ ,  $t_{HZ}$ ,  $t_{RPRE}$  etc) are reported with respect to this reference load. This reference load is also used to report slew rate.

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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**[Usage environment]**

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Example:

- 1) Usage in liquids, including water, oils, chemicals and organic solvents.
- 2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
- 3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>x</sub>.
- 4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
- 5) Usage in places where dew forms.
- 6) Usage in environments with mechanical vibration, impact, or stress.
- 7) Usage near heating elements, igniters, or flammable items.

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