

# TPH6R30ANL

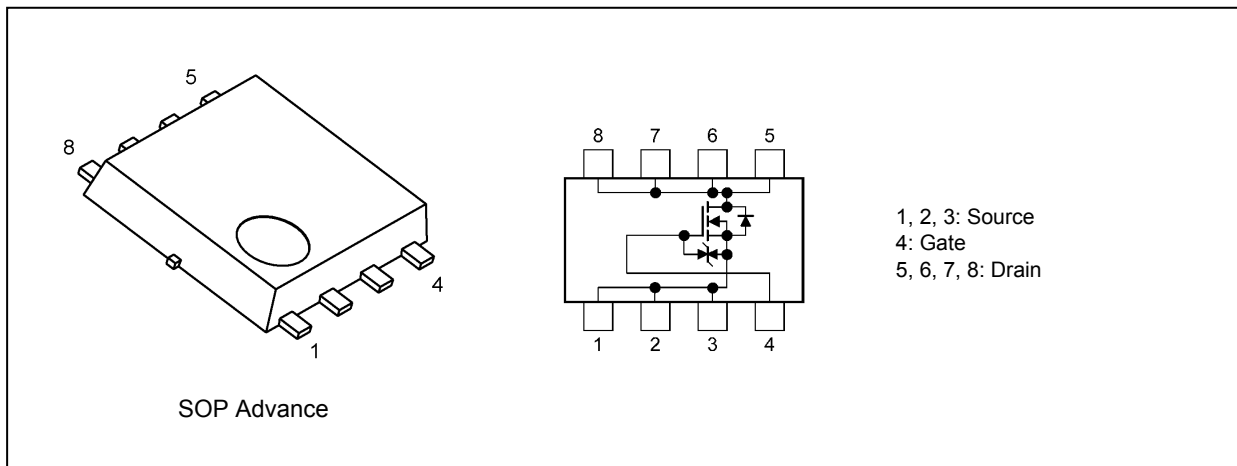
## 1. Applications

- High-Efficiency DC-DC Converters
- Switching Voltage Regulators
- Motor Drivers

## 2. Features

- (1) High-speed switching
- (2) Small gate charge :  $Q_{SW} = 14 \text{ nC (typ.)}$
- (3) Small output charge :  $Q_{OSS} = 46 \text{ nC (typ.)}$
- (4) Low drain-source on-resistance :  $R_{DS(ON)} = 5.1 \text{ m}\Omega \text{ (typ.) (} V_{GS} = 10 \text{ V)}$
- (5) Low leakage current :  $I_{DSS} = 10 \text{ }\mu\text{A (max) (} V_{DS} = 100 \text{ V)}$
- (6) Enhancement mode :  $V_{th} = 1.5 \text{ to } 2.5 \text{ V (} V_{DS} = 10 \text{ V, } I_D = 0.5 \text{ mA)}$

## 3. Packaging and Internal Circuit



Start of commercial production

2016-09

**4. Absolute Maximum Ratings (Note) ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

| Characteristics  | Symbol    | Rating     | Unit             |
|--|-----------|------------|------------------|
| Drain-source voltage   | $V_{DSS}$ | 100        | V                |
| Gate-source voltage  | $V_{GSS}$ | $\pm 20$   |                  |
| Drain current (DC) ( $T_c = 25\text{ }^\circ\text{C}$ ) (Note 1) | $I_D$     | 45         | A                |
| Drain current (DC) (Silicon limit) (Note 1), (Note 2)            | $I_D$     | 66         |                  |
| Drain current (pulsed) ( $t = 100\text{ }\mu\text{s}$ ) (Note 1) | $I_{DP}$  | 300        |                  |
| Power dissipation ( $T_c = 25\text{ }^\circ\text{C}$ )           | $P_D$     | 54         | W                |
| Power dissipation (Note 3)                                       | $P_D$     | 2.5        |                  |
| Power dissipation (Note 4)                                       | $P_D$     | 0.8        |                  |
| Single-pulse avalanche energy (Note 5)                           | $E_{AS}$  | 63         | mJ               |
| Single-pulse avalanche current (Note 5)                          | $I_{AS}$  | 45         | A                |
| Channel temperature  | $T_{ch}$  | 150        | $^\circ\text{C}$ |
| Storage temperature  | $T_{stg}$ | -55 to 150 |                  |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**5. Thermal Characteristics**

| Characteristics   | Symbol         | Max  | Unit                      |
|---|----------------|------|---------------------------|
| Channel-to-case thermal resistance ( $T_c = 25\text{ }^\circ\text{C}$ )             | $R_{th(ch-c)}$ | 2.31 | $^\circ\text{C}/\text{W}$ |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^\circ\text{C}$ ) (Note 3) | $R_{th(ch-a)}$ | 50   |                           |
| Channel-to-ambient thermal resistance ( $T_a = 25\text{ }^\circ\text{C}$ ) (Note 4) | $R_{th(ch-a)}$ | 156  |                           |

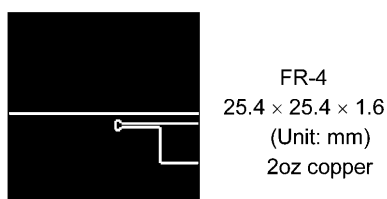
Note 1: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

Note 2: Limited by silicon chip capability.

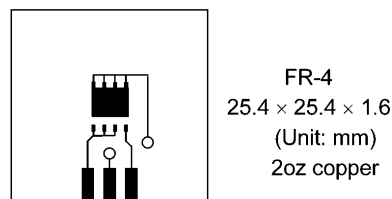
Note 3: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 4: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 5:  $V_{DD} = 60\text{ V}$ ,  $T_{ch} = 25\text{ }^\circ\text{C}$  (initial),  $L = 34\text{ }\mu\text{H}$ ,  $I_{AS} = 45\text{ A}$



**Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)**



**Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)**

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

**6. Electrical Characteristics**

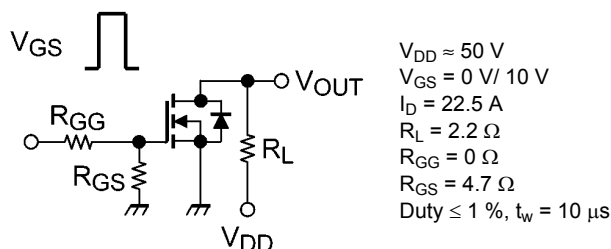
**6.1. Static Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

| Characteristics                         | Symbol        | Test Condition                                  | Min | Typ. | Max      | Unit             |
|---|---------------|---|-----|------|----------|------------------|
| Gate leakage current                    | $I_{GSS}$     | $V_{GS} = \pm 16\text{ V}, V_{DS} = 0\text{ V}$ | —   | —    | $\pm 10$ | $\mu\text{A}$    |
| Drain cut-off current                   | $I_{DSS}$     | $V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$    | —   | —    | 10       |                  |
| Drain-source breakdown voltage          | $V_{(BR)DSS}$ | $I_D = 10\text{ mA}, V_{GS} = 0\text{ V}$       | 100 | —    | —        | V                |
| Drain-source breakdown voltage (Note 6) | $V_{(BR)DSX}$ | $I_D = 10\text{ mA}, V_{GS} = -20\text{ V}$     | 65  | —    | —        |                  |
| Gate threshold voltage                  | $V_{th}$      | $V_{DS} = 10\text{ V}, I_D = 0.5\text{ mA}$     | 1.5 | —    | 2.5      |                  |
| Drain-source on-resistance              | $R_{DS(ON)}$  | $V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$      | —   | 6.4  | 10.3     | $\text{m}\Omega$ |
|   |               | $V_{GS} = 10\text{ V}, I_D = 22.5\text{ A}$     | —   | 5.1  | 6.3      |                  |

Note 6: If a reverse bias is applied between gate and source, this device enters  $V_{(BR)DSX}$  mode. Note that the drain-source breakdown voltage is lowered in this mode.

**6.2. Dynamic Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

| Characteristics                | Symbol    | Test Condition   | Min | Typ. | Max  | Unit        |
|--------------------------------|-----------|--|-----|------|------|-------------|
| Input capacitance              | $C_{iss}$ | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$<br>$f = 1\text{ MHz}$ | —   | 3300 | 4300 | $\text{pF}$ |
| Reverse transfer capacitance   | $C_{rss}$ |  | —   | 27   | 56   |             |
| Output capacitance             | $C_{oss}$ |  | —   | 410  | —    |             |
| Gate resistance                | $r_g$     | —  | —   | 2.1  | 3.2  | $\Omega$    |
| Switching time (rise time)     | $t_r$     | See Figure 6.2.1   | —   | 7    | —    | ns          |
| Switching time (turn-on time)  | $t_{on}$  |  | —   | 18   | —    |             |
| Switching time (fall time)     | $t_f$     |  | —   | 12   | —    |             |
| Switching time (turn-off time) | $t_{off}$ |  | —   | 58   | —    |             |



**Fig. 6.2.1 Switching Time Test Circuit**

**6.3. Gate Charge Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

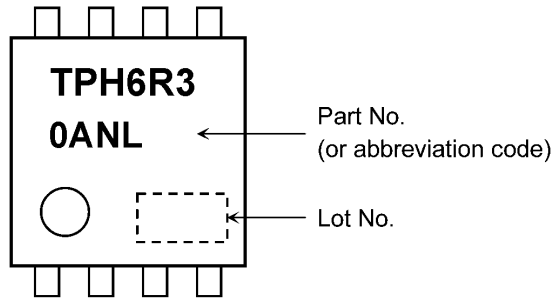
| Characteristics                                 | Symbol    | Test Condition  | Min | Typ. | Max | Unit |
|---|-----------|---|-----|------|-----|------|
| Total gate charge (gate-source plus gate-drain) | $Q_g$     | $V_{DD} \approx 50\text{ V}, V_{GS} = 10\text{ V},$<br>$I_D = 22.5\text{ A}$  | —   | 55   | —   | nC   |
|   |           | $V_{DD} \approx 50\text{ V}, V_{GS} = 4.5\text{ V},$<br>$I_D = 22.5\text{ A}$ | —   | 27   | —   |      |
| Gate-source charge 1                            | $Q_{gs1}$ | $V_{DD} \approx 50\text{ V}, V_{GS} = 10\text{ V},$<br>$I_D = 22.5\text{ A}$  | —   | 16   | —   |      |
| Gate-drain charge                               | $Q_{gd}$  |   | —   | 7    | —   |      |
| Gate switch charge                              | $Q_{SW}$  |   | —   | 14   | —   |      |
| Output charge                                   | $Q_{oss}$ | $V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V},$<br>$f = 1\text{ MHz}$            | —   | 46   | —   |      |

**6.4. Source-Drain Characteristics ( $T_a = 25\text{ }^\circ\text{C}$  unless otherwise specified)**

| Characteristics                         | Symbol    | Test Condition  | Min | Typ. | Max  | Unit |
|---|-----------|---|-----|------|------|------|
| Reverse drain current (pulsed) (Note 7) | $I_{DRP}$ | ( $t = 100\text{ }\mu\text{s}$ )  | —   | —    | 300  | A    |
| Diode forward voltage                   | $V_{DSF}$ | $I_{DR} = 45\text{ A}$ , $V_{GS} = 0\text{ V}$  | —   | —    | -1.2 | V    |
| Reverse recovery time                   | $t_{rr}$  | $V_R = 50\text{ V}$ , $I_{DR} = 11.3\text{ A}$ , $V_{GS} = 0\text{ V}$ , $-di_{DR}/dt = 100\text{ A}/\mu\text{s}$ | —   | 48   | —    | ns   |
| Reverse recovery charge                 | $Q_{rr}$  |   | —   | 61   | —    | nC   |

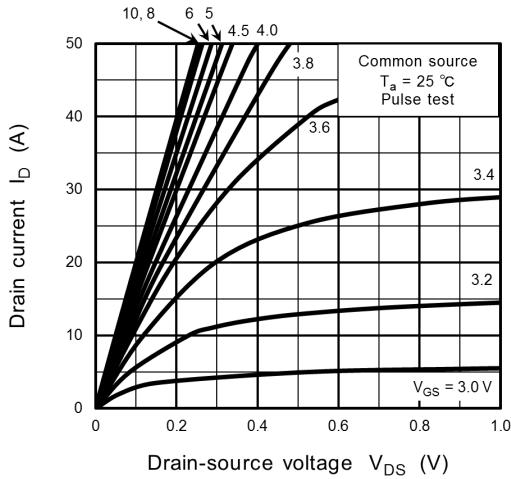
Note 7: Ensure that the channel temperature does not exceed  $150\text{ }^\circ\text{C}$ .

**7. Marking**

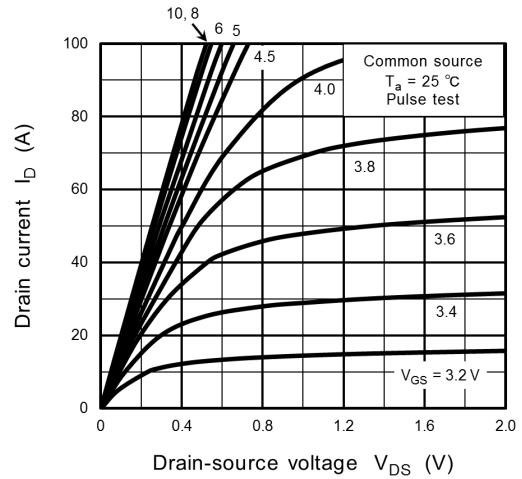


**Fig. 7.1 Marking**

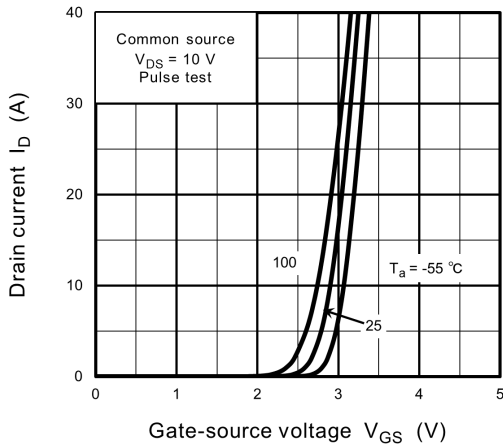
**8. Characteristics Curves (Note)**



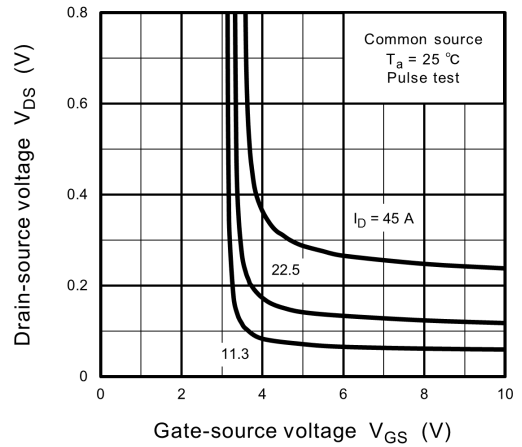
**Fig. 8.1  $I_D - V_{DS}$**



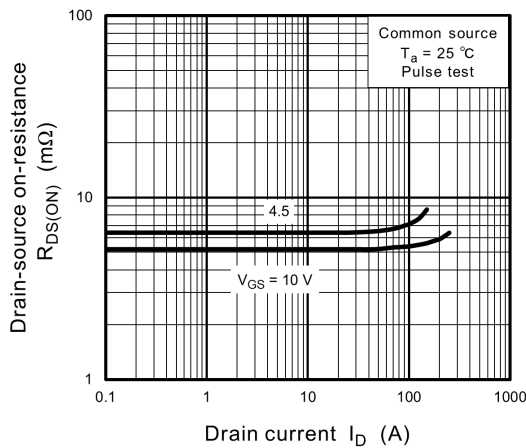
**Fig. 8.2  $I_D - V_{DS}$**



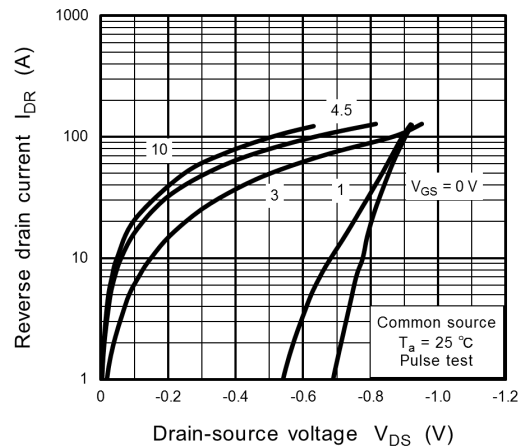
**Fig. 8.3  $I_D - V_{GS}$**



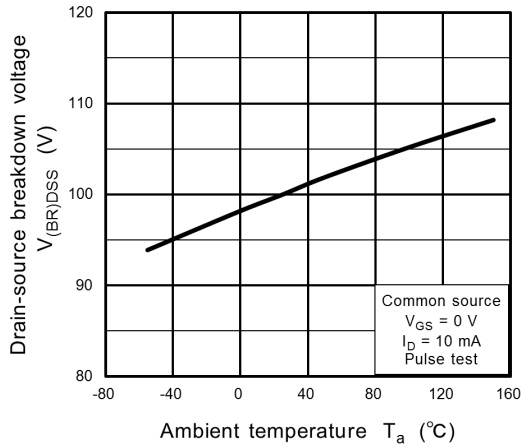
**Fig. 8.4  $V_{DS} - V_{GS}$**



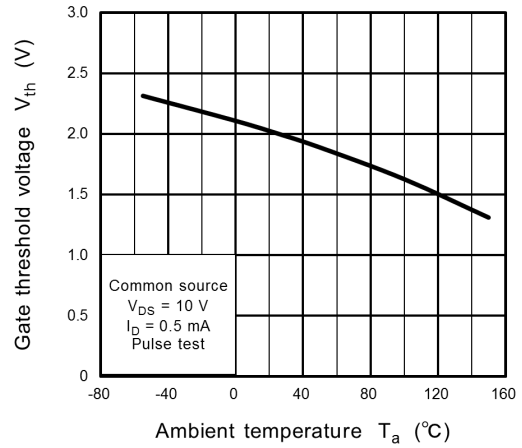
**Fig. 8.5  $R_{DS(ON)} - I_D$**



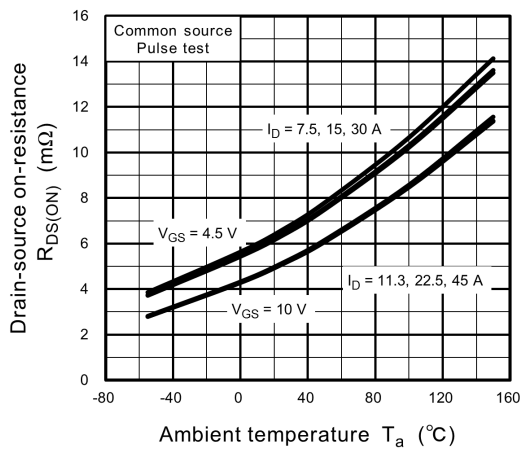
**Fig. 8.6  $I_{DR} - V_{DS}$**



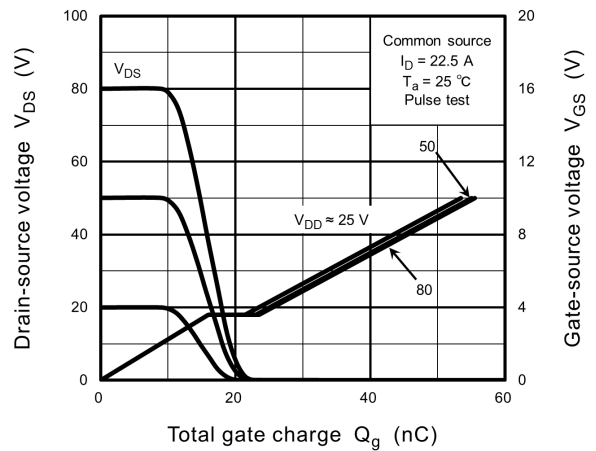
**Fig. 8.7  $V_{(BR)DSS} - T_a$**



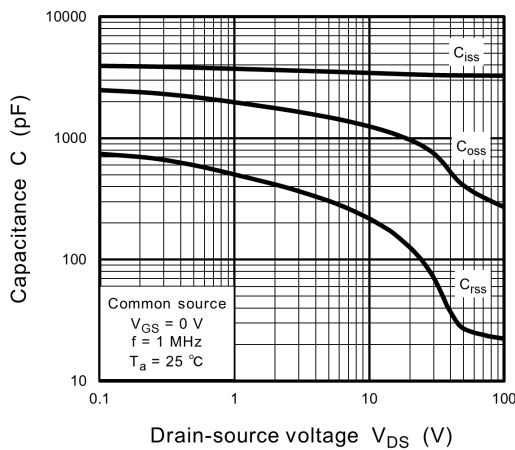
**Fig. 8.8  $V_{th} - T_a$**



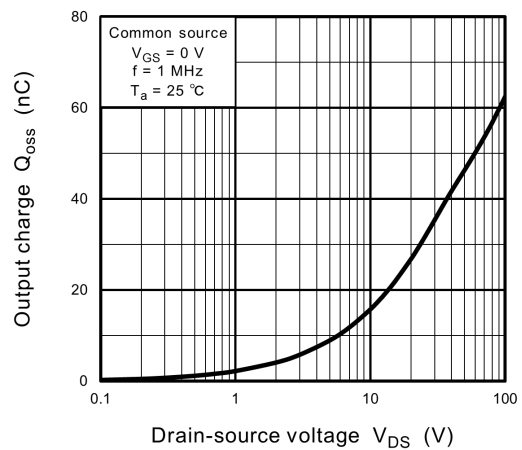
**Fig. 8.9  $R_{DS(ON)} - T_a$**



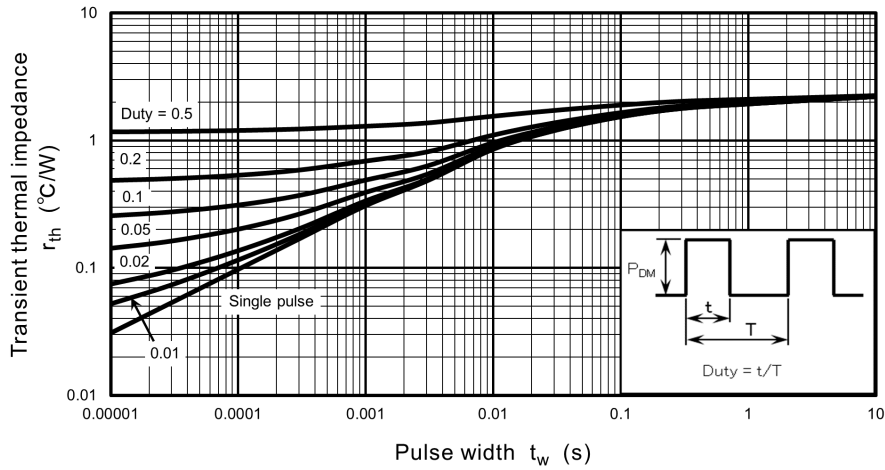
**Fig. 8.10 Dynamic Input/Output Characteristics**



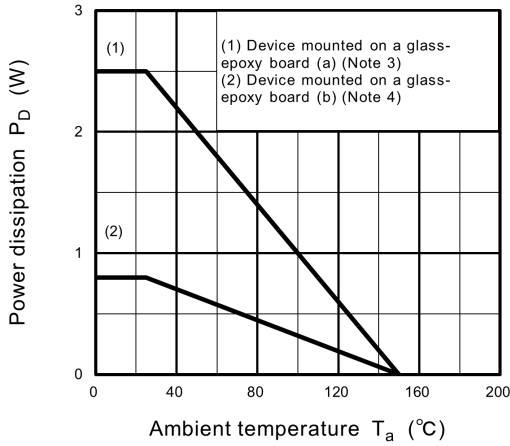
**Fig. 8.11 Capacitance -  $V_{DS}$**



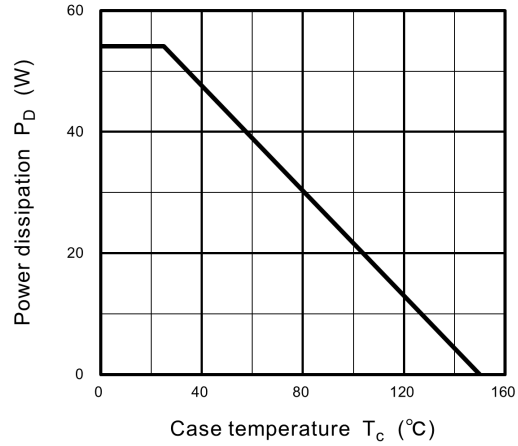
**Fig. 8.12  $Q_{oss} - V_{DS}$**



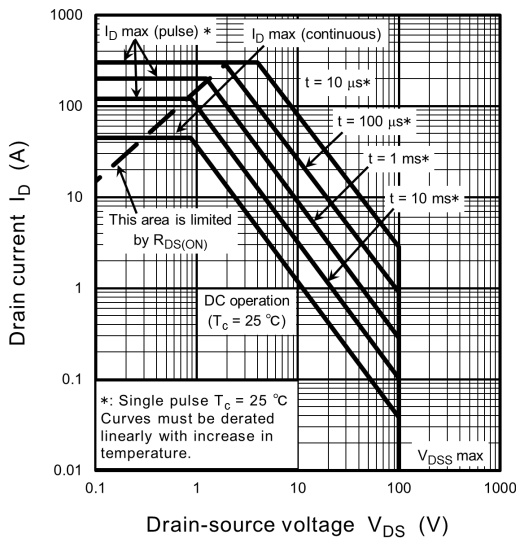
**Fig. 8.13  $r_{th} - t_w$**   
(Guaranteed Maximum)



**Fig. 8.14  $P_D - T_a$**   
(Guaranteed Maximum)



**Fig. 8.15  $P_D - T_c$**   
(Guaranteed Maximum)

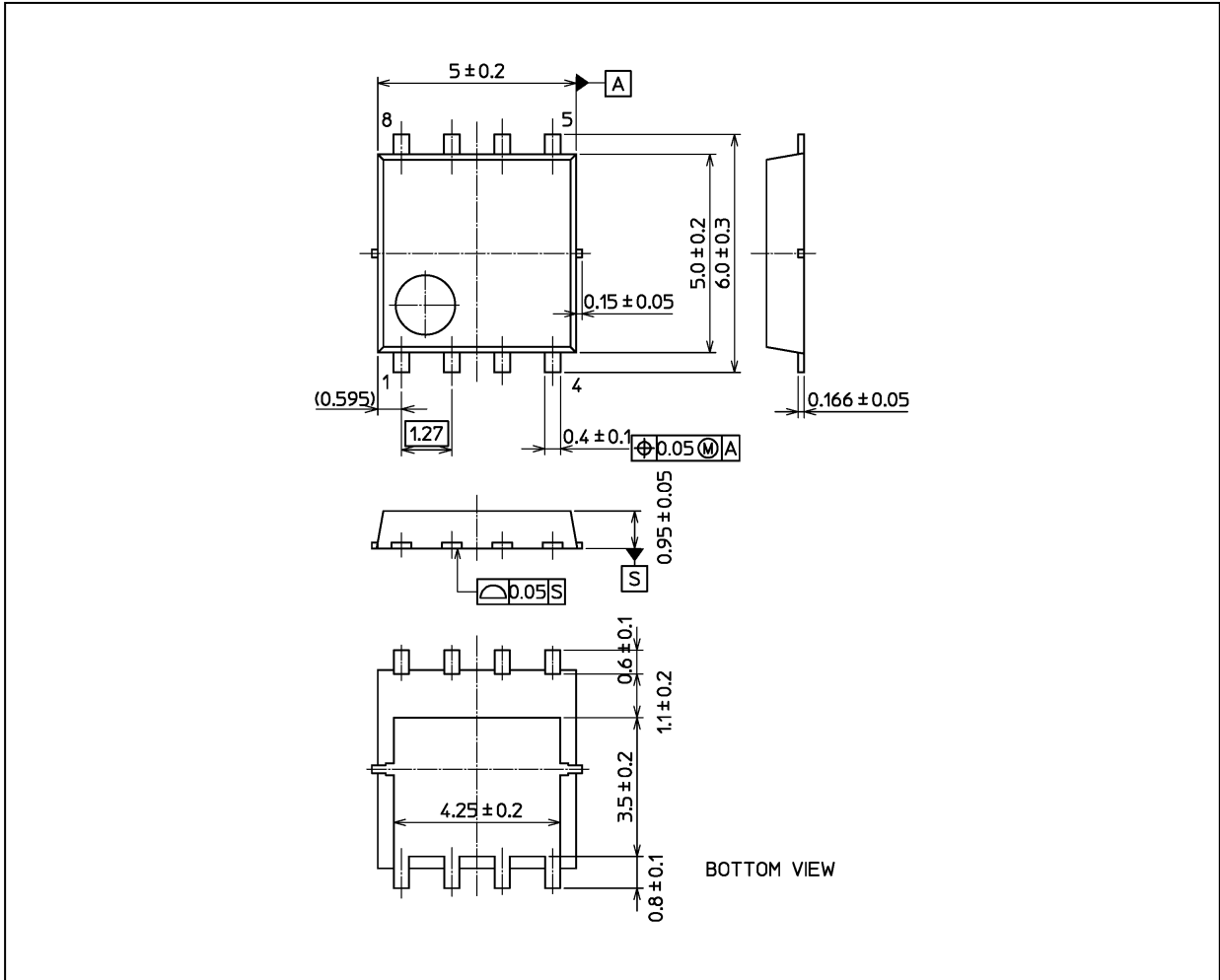


**Fig. 8.16 Safe Operating Area**  
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

Package Dimensions

Unit: mm



Weight: 0.069 g (typ.)

| Package Name(s)       |
|-----------------------|
| TOSHIBA: 2-5Q1S       |
| Nickname: SOP Advance |



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